

SGM330A

Quad, Wide-Bandwidth SPDT Video Analog Switch

GENERAL DESCRIPTION

The SGM330A is a Quad, bidirectional, single-pole/double-throw (SPDT) CMOS Video analog switches (Mux/DeMux) designed to operate at a single +5V supply. This 2-channel multiplexer/demultiplexer is recommended for both RGB and composite video switching applications. The Video Switch can be driven from a current output RAMDAC or voltage output composite video source.

Wide bandwidth (500MHz) , low On-Resistance (6Ω) , and low crosstalk make it suitable for high-frequency and other applications. Also this device has exceptionally high current capability which is far greater than most analog switches offered today.

The SGM330A offers a high-performance, low-cost solution to switch between video sources. It is specified -40°C to $+85^{\circ}\text{C}$ temperature range. The SGM330A has lead (Pb) free SOIC-16, TSSOP-16 and QSOP-16 packages.

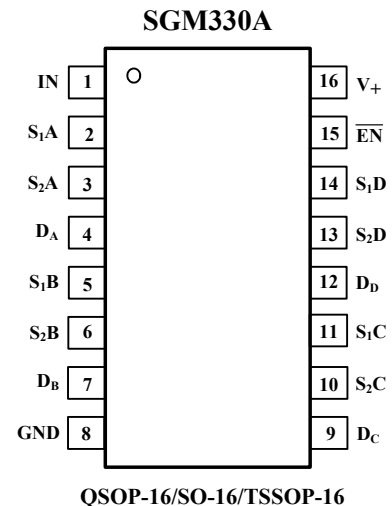
FEATURES

- **Wide Bandwidth:** 500 MHz
- **Low On-Resistance:** 6Ω (TYP)
- **Low Crosstalk:** -60dB @ 10MHz(TYP)
- **Single Power Operation:** +5V
- **Fast Switching Time**
- **Rail-to-Rail Operation**
- **Typical Power Consumption** (0.1 μW)
- **TTL/CMOS Compatible**
- **Micro size Package**
 - SO-16
 - TSSOP-16
 - QSOP-16

APPLICATIONS

Personal Video Recorders
Terrestrial Set-Top Boxes
Hard Disk Recorders
DVD Players
Game Consoles
Digital VCRs
Desktop Video Editors
Audio and Video Switching

PIN CONFIGURATIONS (TOP VIEW)



ORDERING INFORMATION

ORDERING NUMBER	PIN- PACKAGE	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	PACKAGE OPTION
SGM330A-YS/TR	SO-16	- 40°C to +85°C	SGM330A-YS	Tape and Reel, 2500
SGM330A-YTS/TR	TSSOP-16	- 40°C to +85°C	SGM330A-YTS	Tape and Reel, 3000
SGM330A-YQS/TR	QSOP-16	- 40°C to +85°C	SGM330A-YQS	Tape and Reel, 3000

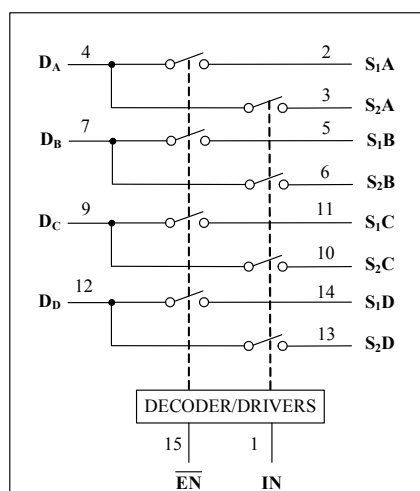
ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground Potential (Inputs & V₊ only)... - 0.5V to +6V
 Supply Voltage to Ground Potential (Outputs & D only) .. - 0.5V to +6V
 DC Input Voltage - 0.5V to +6V
 DC Output Current 200mA
 Operating Temperature Range..... - 40°C to +85°C
 Junction Temperature.....+150°C
 Storage Temperature.....- 65°C to +150°C
 Package Thermal Resistance @ T_A = 25°C

SO-16, θ_{JA} 82°C/W
 TSSOP-16, θ_{JA}100°C/W
 QSOP-16, θ_{JA}103°C/W
 Lead Temperature (soldering, 10s)260°C
 ESD Susceptibility
 HBM.....4000V
 MM.....400V

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM (positive logic)



PIN DESCRIPTION

NAME	FUNCTION
S ₁ A, S ₁ B, S ₁ C, S ₁ D S ₂ A, S ₂ B, S ₂ C, S ₂ D	Analog video I/O
IN	Select input
$\overline{EN}$	Switch-enable input
D _A , D _B , D _C , D _D	Analog video I/O
GND	Ground
V ₊	Power supply

FUNCTION TABLE

$\overline{EN}$	IN	ON Switch
0	0	S ₁ A, S ₁ B, S ₁ C, S ₁ D
0	1	S ₂ A, S ₂ B, S ₂ C, S ₂ D
1	X	Disabled

Notes: S₁ is normally connected when IN is "0".

ELECTRICAL CHARACTERISTICS

(Over the Operating Range, $V_+ = +5\text{ V} \pm 10\%$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNITS
DC CHARACTERISTICS						
Analog Signal Range	V_{ANALOG}		0		2.0	V
On-Resistance	R_{ON}	$V_+ = 4.5\text{V}$, $V_I = 1.0\text{V}$, $R_L = 75\Omega$, $I_{\text{ON}} = 13\text{mA}$		6	9	Ω
		$V_+ = 4.5\text{V}$, $V_I = 2.0\text{V}$, $R_L = 75\Omega$, $I_{\text{ON}} = 26\text{mA}$		7	10	Ω
Input High Voltage	V_{IH}	Guaranteed Logic HIGH Level	2.0			V
Input Low Voltage	V_{IL}	Guaranteed Logic LOW Level	-0.5		0.8	V
Input High Current	I_{IH}	$V_+ = 5.5\text{V}$, $V_{\text{IN}} = V_+$			± 1	μA
Input Low Current	I_{IL}	$V_+ = 5.5\text{V}$, $V_{\text{IN}} = \text{GND}$			± 1	μA
Analog Output Leakage Current	I_{O}	$0 \leq S1, S2$, or $D \leq V_+$, Switch OFF			± 1	μA
Short Circuit Current	I_{OS}			230		mA
Clamp Diode Voltage	V_{IK}	$V_{\text{CC}} = 4.5\text{V}$, $I_{\text{IN}} = -18\text{mA}$	-0.7	-0.9		V
Input Hysteresis at Control Pins	V_{H}			200		mV
DYNAMIC CHARACTERISTICS						
Turn-On Time	T_{ON}	$R_L = 70\Omega$, $C_L = 20\text{pF}$ (Figure 1)		14	17	ns
Turn-Off Time	T_{OFF}	$R_L = 70\Omega$, $C_L = 20\text{pF}$ (Figure 1)		4	7	ns
Off Isolation	O_{IRR}	$R_L = 150\Omega$, $f = 10\text{MHz}$ (Figure 5)		-55		dB
Channel-to-Channel Crosstalk	X_{TALK}	$R_{\text{IN}} = 10\Omega$, $R_L = 150\Omega$, $f = 10\text{MHz}$ (Figure 4)		-60		dB
Bandwidth -3 dB	BW	$R_L = 150\Omega$ (Figure 3)			500	MHz
Input/Enable Capacitance	C_{IN}	$V_{\text{IN}} = 0\text{V}$, $f = 1\text{MHz}$			5	pF
Switch OFF Capacitance	C_{OFF}	$V_{\text{IN}} = 0\text{V}$, $f = 1\text{MHz}$			5	pF
Switch ON Capacitance	C_{ON}	$V_{\text{IN}} = 0\text{V}$, $f = 1\text{MHz}$			8	pF
Differential Gain	D_{G}	$R_L = 150\Omega$, $f = 3.58\text{MHz}$ (Figure 2)		0.51		%
Differential Phase	D_{P}	$R_L = 150\Omega$, $f = 3.58\text{MHz}$ (Figure 2)		0.01		$^\circ$
POWER REQUIREMENTS						
Quiescent Power Supply Current	I_{CC}	$V_+ = +5.5\text{V}$, $\text{IN} = \text{GND}$ or 5V		0.1	20.0	μA
Supply Current per Input @ TTL HIGH	ΔI_{CC}	$V_+ = +5.5\text{V}$, $\text{IN} = 3.4\text{V}$			300	μA
Supply Current per Input per MHz	I_{CCD}	$V_+ = +5.5\text{V}$, $S1, S2$ and D Pins Open $\overline{EN} = \text{GND}$ Control Input Toggling 50% Duty Cycle			0.1	mA/ MHz

Specifications subject to change without notice.

Notes:

1. Typical values are at $V_{\text{CC}} = 5.0\text{V}$, $T_A = 25^\circ\text{C}$ ambient and maximum loading.

PARAMETER DEFINITIONS

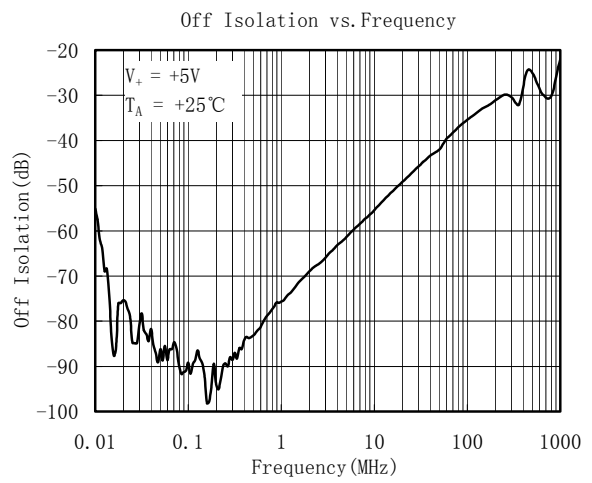
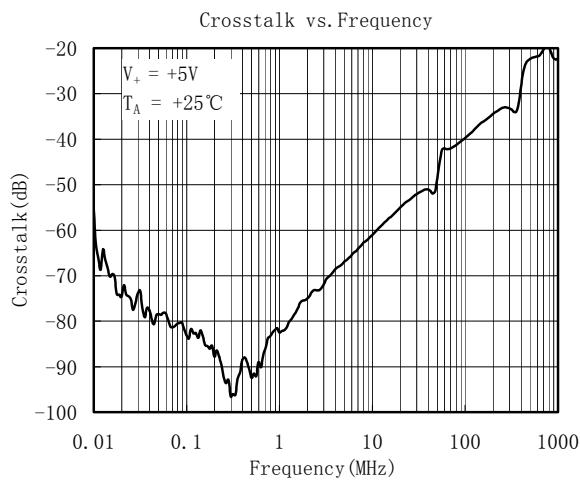
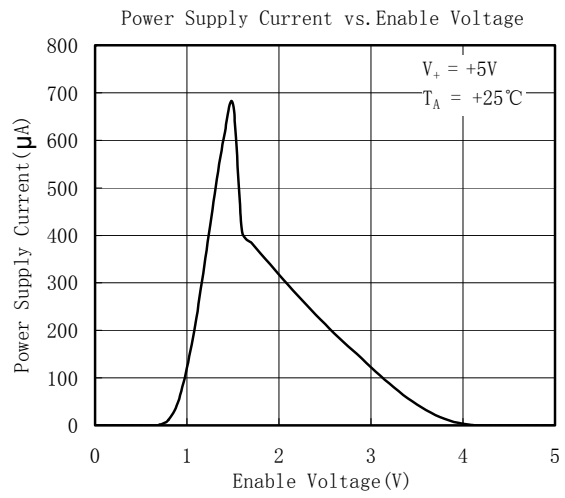
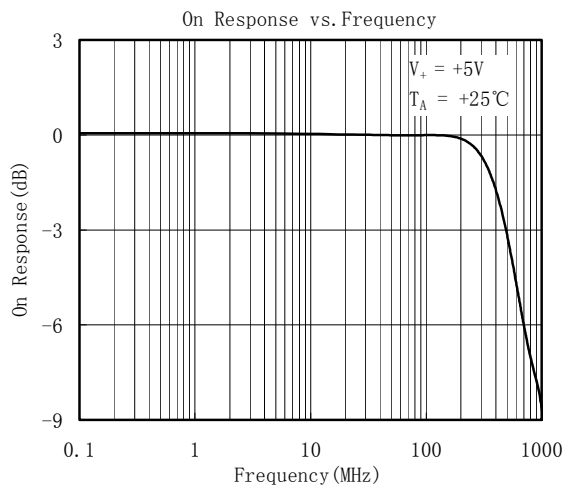
PARAMETER	DESCRIPTION
R_{ON}	Resistance between source and drain with switch in the ON state
I_O	Output leakage current measured at S1, S2, and D with the switch OFF
V_{IN}	Digital voltage at the IN pin that selects between S1 and S2 analog inputs
V_I	Voltage applied to the D or S1, S2 pins when D or S1, S2 is the switch input
V_{EN}	A voltage that ENABLES the chip
C_{IN}	Capacitance at the digital inputs
C_{OFF}	Capacitance at analog I/O (S1, S2, D) with switch OFF
C_{ON}	Capacitance at analog I/O (S1, S2, D) with switch ON
V_{IH}	Minimum input voltage for logic HIGH
V_{IL}	Minimum input voltage for logic LOW
$I_{IH} (I_{IL})$	Input current of the digital input
I_{OS}	Minimum short circuit current for S1, S2 and D
T_{ON}	Propagation delay measured between 50% of the digital input to 90% of the analog output when switch is turned ON. The peak analog voltage is 0.714V
T_{OFF}	Propagation delay measured between 50% of the digital input to 90% of the analog output when switch is turned OFF. The peak analog voltage is 0.714V
BW	response of the switch in the ON state measured at 3dB down
X_{TALK}	Is an unwanted signal coupled from channel to channel. Measured in -dB. $X_{TALK} = 20 \text{ LOG } V_{OUT}/V_{IN}$. This is non-adjacent crosstalk
D_G	Magnitude variation between analog input and output pins when the switch is ON and the dc offset of composite-video signal varies at the analog input pin. In the NTSC standard, the frequency of the video signal is 3.58 MHz, and dc offset is from 0 to 0.714 V.
D_P	Phase variation between analog input and output pins when the switch is ON and the dc offset of composite-video signal varies at the analog input pin. In the NTSC standard, the frequency of the video signal is 3.58 MHz, and dc offset is from 0 to 0.714 V.
O_{IRR}	Off isolation is the resistance (measured in -dB) between the input and output with the switch off (NO)

CAUTION

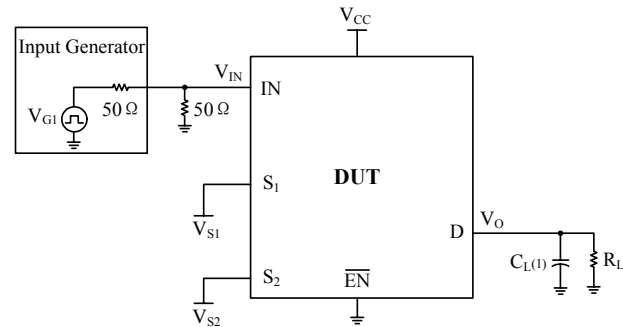
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. Shengbang Micro-electronics recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

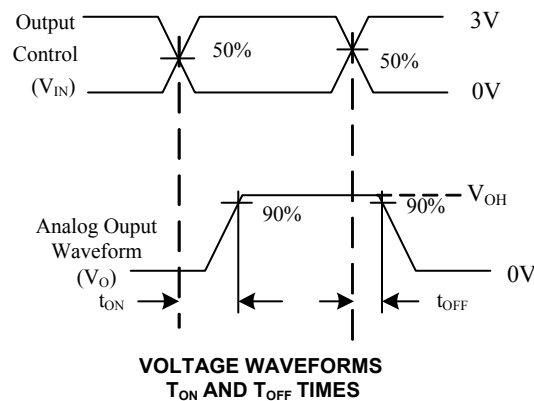
TYPICAL PERFORMANCE CHARACTERISTICS



TEST CIRCUITS



Test	V _{CC}	R _L	C _L	V _{S1}	V _{S2}
T _{ON}	5V±0.5V	75	20	GND	3V
	5V±0.5V	75	20	3V	GND
T _{OFF}	5V±0.5V	75	20	GND	3V
	5V±0.5V	75	20	3V	GND



NOTES:

1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_o = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
3. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Test Circuit for Voltage Waveform and Switch Time

TEST CIRCUITS(continued)

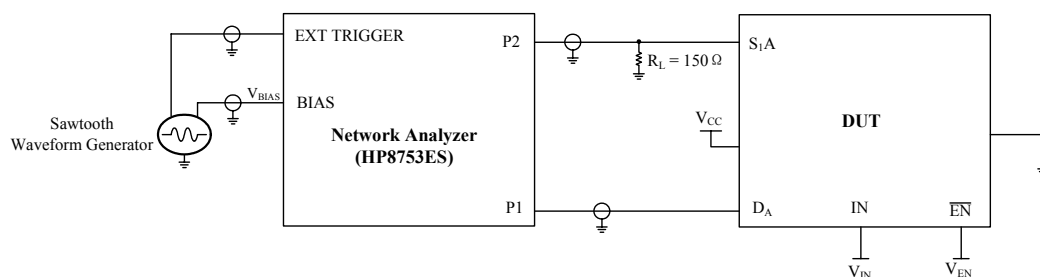


Figure 2. Test Circuit for Differential Gain/Phase Measurement

Differential gain and phase are measured at the output of the ON channel. For example, when $V_{IN} = 0$, $V_{EN} = 0$, and D_A is the input, the output is measured at S_{1A} .

HP8753ES Setup

Average = 20

RBW = 300 Hz

ST = 1.381 s

P1 = -7 dBm

CW frequency = 3.58 MHz

Sawtooth Waveform Generator Setup

$V_{BIAS} = 0$ to 1 V

Frequency = 0.905 Hz

TEST CIRCUITS(continued)

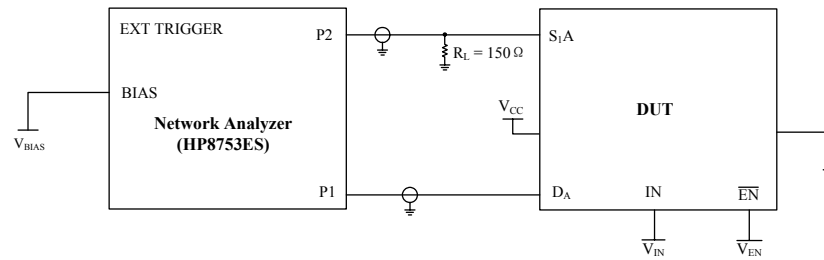


Figure3. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when $V_{IN} = 0$, $V_{EN} = 0$, and D_A is the input, the output is measured at S_{1A} . All unused analog I/O ports are left open.

HP8753ES Setup

Average = 4

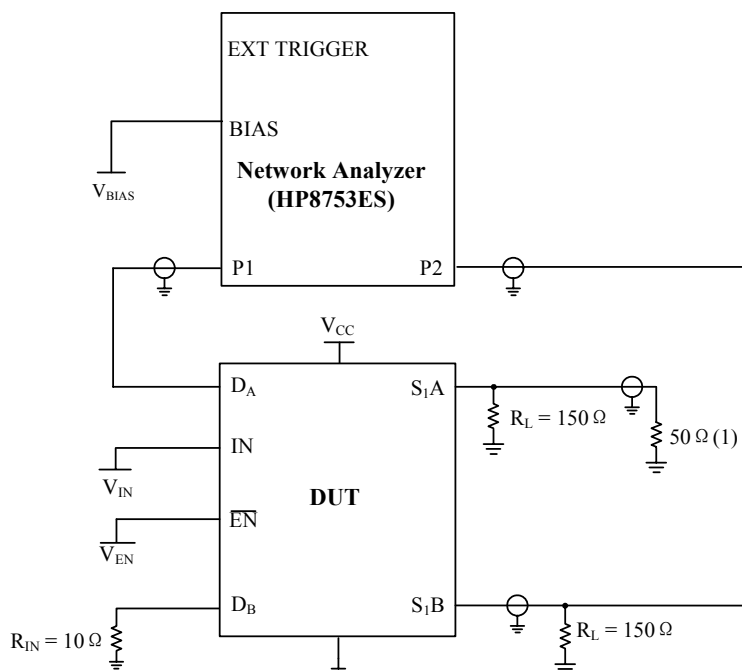
RBW = 3 Hz

$V_{BIAS} = 0.35$ V

ST = 2 s

P1 = 0 dBm

TEST CIRCUITS(continued)



NOTES: (1) A 50Ω termination resistor is needed for the network analyzer.

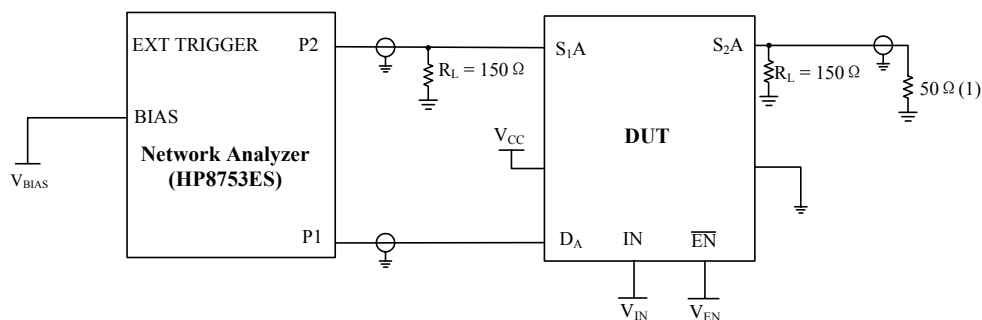
Figure 4. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when V_{IN} = 0, V_{EN} = 0, and D_A is the input, the output is measured at S₁B. All unused analog input (D) ports and output (S) ports are connected to GND through 10Ω and 50Ω pulldown resistors, respectively.

HP8753ES Setup

Average = 4
 RBW = 3 kHz
 V_{BIAS} = 0.35 V
 ST = 2 s
 P1 = 0 dBm

TEST CIRCUITS(continued)



NOTES: (1) A 50Ω termination resistor is needed for the network analyzer.

Figure 5. Test Circuit for Off Isolation (OIRR)

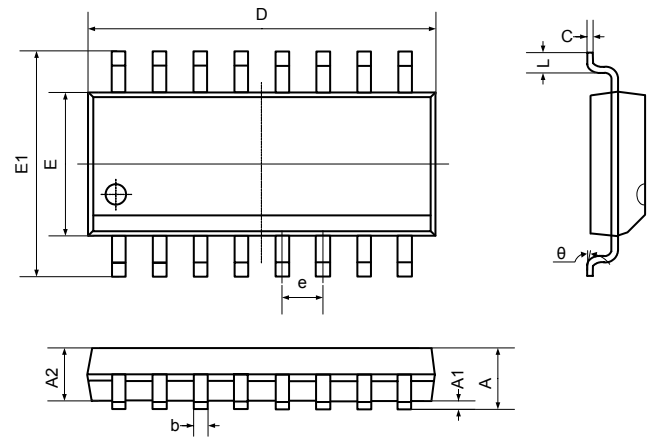
Off isolation is measured at the output of the OFF channel. For example, when $V_{IN} = V_{CC}$, $V_{EN} = 0$, and D_A is the input, the output is measured at S_{1A} . All unused analog input (D) ports are left open, and output (S) ports are connected to GND through 50Ω pulldown resistors.

HP8753ES Setup

Average = 4
 RBW = 3 kHz
 $V_{BIAS} = 0.35\text{ V}$
 ST = 2 s
 P1 = 0 dBm

PACKAGE OUTLINE DIMENSIONS

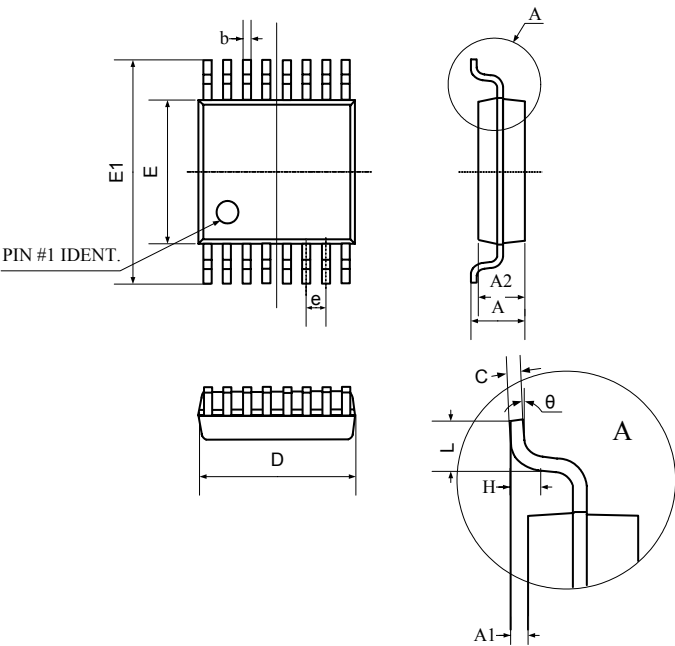
SO-16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.20	0.386	0.402
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

TSSOP-16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

PACKAGE OUTLINE DIMENSIONS

QSOP-16

