

Dual or Quad Selectable Programmable Crystal Oscillator
Output: LV-PECL

SG-8503CA / SG-8504CA

- Dual frequency Selectable: SG-8503CA, 7.0 × 5.0 × 1.5 mm (6 pins)
- Quad frequency Selectable: SG-8504CA, 7.0 × 5.0 × 1.5 mm (8 pins)
- Frequency range: 50 MHz to 800 MHz
- Supply voltage: 2.5 V to 3.3 V

Features

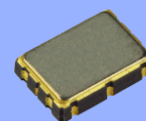
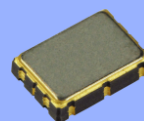
- User-specified two (FSEL) or four (FSEL0, FSEL1) startup frequencies
- High frequency fundamental tone crystal, Low jitter PLL technology
- Available field oscillator programmer "SG-Writer II"

Application

- OTN, BTS, Test Instrument



Product Number (please contact us)
 SG-8503CA : X1G005011xxx00
 SG-8504CA : X1G005021xxx00



Actual size


Specifications (characteristics)

Item	Symbol	Specifications	Conditions / Remarks
Output frequency range	f_o	50 MHz to 800 MHz	-
Supply voltage	V_{CC}	2.5 V - 0.125 V to 3.3 V + 0.33 V	-
Storage temperature	T_{stg}	-55 °C to +125 °C	Store as bare product after packing
Operating temperature	T_{use}	-40 °C to +85 °C	-
Frequency tolerance *1	f_{tol}	K : $\pm 31.5 \times 10^{-6}$	Customized Product (Option)
		L : $\pm 50 \times 10^{-6}$	
Current consumption	I_{CC}	90 mA Max.	OE Active, $L_{ECL} = 50 \Omega$
Disable current	I_{dis}	40 mA Max.	OE Inactive, Output Standby: Hi-Z mode
		70 mA Max.	OE Inactive, Output Standby: Fix mode
Symmetry	SYM	45 % to 55 %	At outputs crossing point
Output voltage	V_{OH}	$V_{CC} - 1.025 \text{ V Min.}$	DC characteristics
	V_{OL}	$V_{CC} - 1.62 \text{ V Max.}$	
Output load condition	L_{ECL}	50 Ω	Termination to $V_{CC} - 2.0 \text{ V}$
Input voltage	V_{IH}	70% V_{CC} Min.	SG-8503CA : OE, FSEL
	V_{IL}	30% V_{CC} Max.	SG-8504CA : OE, FSEL0, FSEL1
Rise time / Fall time	t_r/t_f	400 ps Max.	Between 20% and 80% of ($V_{OH} - V_{OL}$)
Start-up time	t_{str}	10 ms Max.	Time at minimum supply voltage to be 0 s
Setting time for frequency change	t_{SET1}	1.5 ms Max.	SG-8503CA : From setting FSEL pin to output new frequency SG-8504CA : From setting FSEL0 / FSEL1 pin to output new frequency

*1 Frequency tolerance includes initial frequency tolerance, temperature variation, supply voltage change, reflow drift and 10 years aging at +25 °C.

Product Name SG-8503 CA 156MHz 625MHz A P R L Z
 (Standard form) ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨

① Model, ② Package type,

③ Frequency-0 (50 ~ 800 MHz), ④ Frequency-1 (50 ~ 800 MHz), ⑤ Internal crystal frequency, ⑥ Output enable pin Polarity,

⑦ Supply voltage/Output format, ⑧ Frequency tolerance/Operating temperature, ⑨ Output standby type

Product Name SG-8504 CA 156.2MHz nnnn A P R L Z
 (Standard form) ① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨

① Model, ② Package type,

③ Frequency-0 (50 ~ 800 MHz), ④ Parameter identifier, ⑤ Internal crystal frequency, ⑥ Output enable pin Polarity,

⑦ Supply voltage/Output format, ⑧ Frequency tolerance/Operating temperature, ⑨ Output standby type

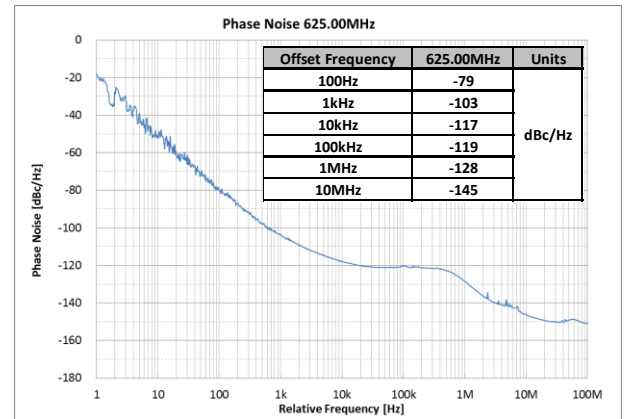
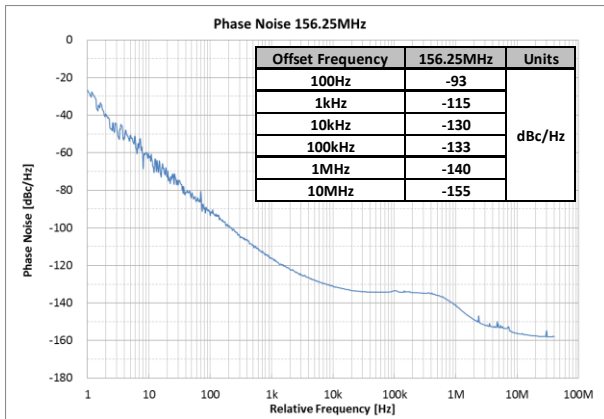
⑤ Internal crystal frequency	⑥ Output enable pin Polarity	⑦ Supply voltage/Output format	⑧ Frequency tolerance/Operating temperature	⑨ Output standby type
A 114.1444 MHz	P Active High Q Active Low	R 2.5 V ~ 3.3 V/LVPECL	K $\pm 31.5 \times 10^{-6}/-40$ to +85 °C L $\pm 50 \times 10^{-6}/-40$ to +85 °C	F Fix (OUT="L", OUTN="H") Z High-Z

Phase Jitter

	Offset Frequency	100.00 MHz	125.00 MHz	156.25 MHz	250.00 MHz	312.50 MHz	500.00 MHz	625.00 MHz
Phase jitter *2 Typ.	12 kHz to 20 MHz	0.31 ps	0.30 ps	0.26 ps	0.26 ps	0.29 ps	0.28 ps	0.29 ps

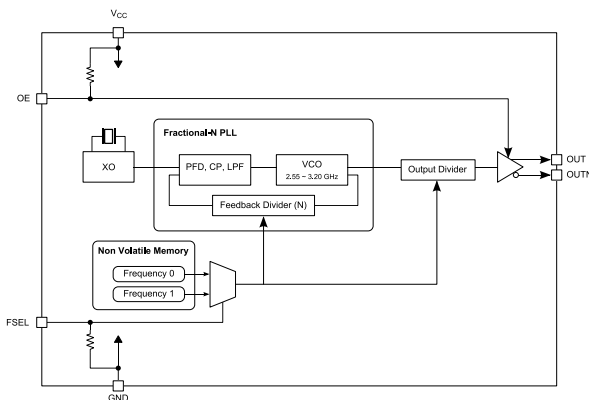
*2 In order to achieve optimum jitter performance, it is recommended that the capacitor (0.1 μF + 10 μF) between V_{CC} and GND pin should be placed as close to the V_{CC} pin as possible.

Phase Noise

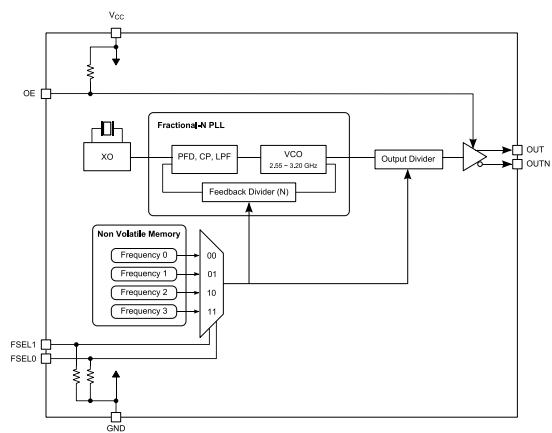


Block diagram

SG-8503CA



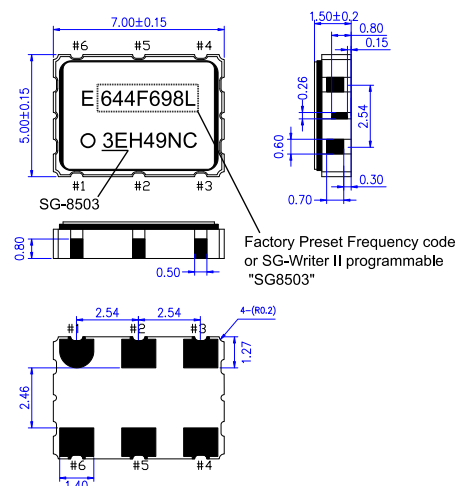
SG-8504CA



External dimensions

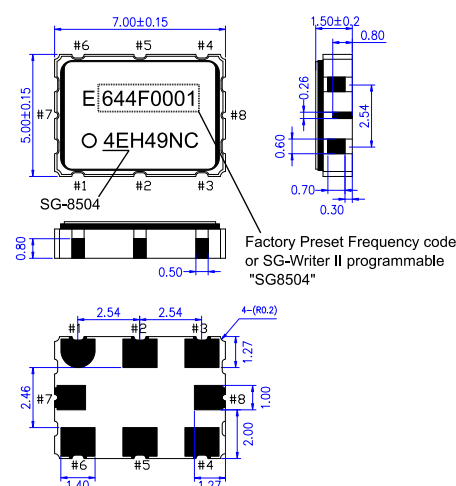
(Unit: mm)

SG-8503CA



Pin	Connection
1	OE
2	FSEL (L = Frequency-0, H = Frequency-1)
3	GND
4	OUT
5	OUTN
6	Vcc

SG-8504CA

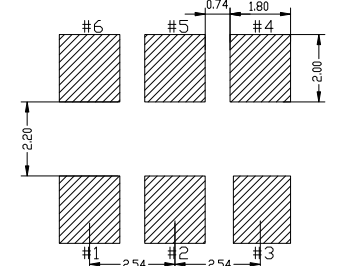


Pin	Connection	Pin	Connection
1	NC	5	OUTN
2	OE	6	Vcc
3	GND	7	FSEL1
4	OUT	8	FSEL0

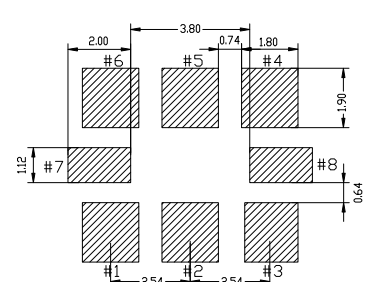
FSEL1, FSEL0	Output Frequency
LL	Frequency-0
LH	Frequency-1
HL	Frequency-2
HH	Frequency-3

Footprint (Recommended)(Unit: mm)

SG-8503CA



SG-8504CA



In order to achieve optimum jitter performance, it is recommended that the capacitor (0.1 μ F + 10 μ F) between V_{CC} and GND pin should be placed as close to the V_{CC} pin as possible.



Simulation Model

- IBIS model is available. Please contact us.

ESD Rating

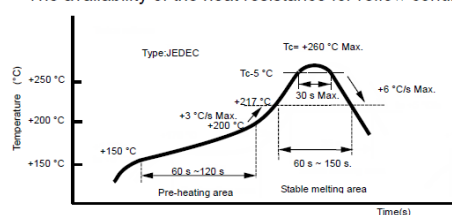
Human Body Model (HBM)	2000 V
Machine Model (MM)	200 V

Device Material & Environmental Information

Model	Package Dimensions	# of Pins	Reference Weight (Typ.)	Terminal Material	Terminal Plating	Complies With EU RoHS	Pb Free	MSL Rating	Peak Temp (Max)
SG-8503CA	7.0 x 5.0 x 1.5 mm	6	167 mg	W	Au	Yes	Yes	1	260 °C
SG-8504CA		8	168 mg						

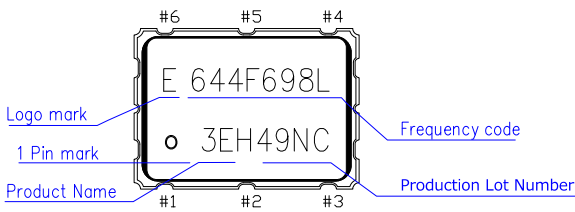
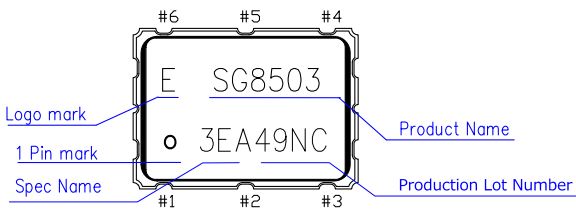
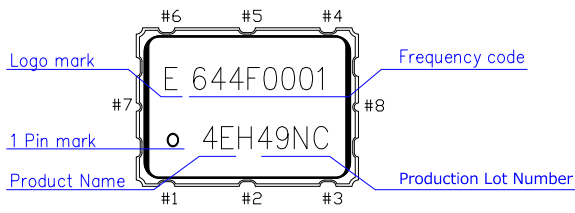
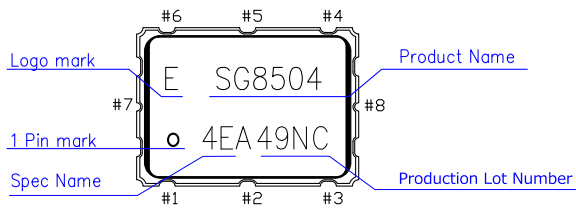
SMD products Reflow profile (example)

The availability of the heat resistance for reflow conditions of JEDEC-STD-020D.01 is judged individually. Please inquire



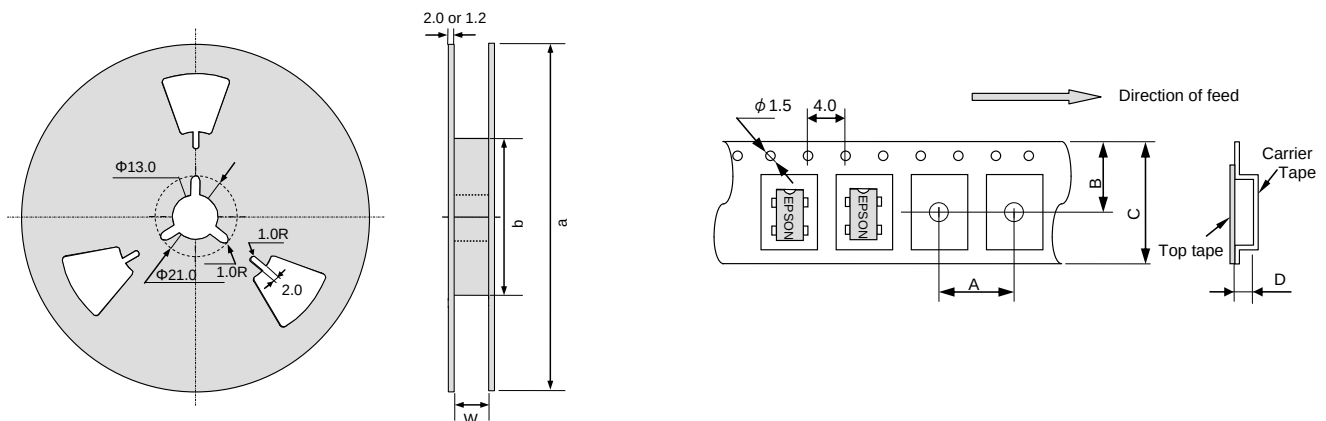
	Pb free.
	- Complies with EU RoHS directive. *About the products without the Pb-free mark. - Contains Pb in products exempted by EU RoHS directive. (Contains Pb in sealing glass, high melting temperature type solder or other.)

Device Marking

Model	Factory Programmed Part Marking	Field Programmable Part Marking (Blank Samples)
SG-8503CA		
SG-8504CA		

Standard Packing Specification

- SMD products are packed in the shipping carton as below table in accordance with taping standards EIA-481 and IEC-60286


Standard Packing Quantity and Dimension (Unit: mm)

Model	Quantity (pcs/Reel)	Reel dimension			Career Tape dimension				Direction of feed (L=left direction)
		a	b	W	A	B	C	D	
SG-8503CA SG-8504CA	1000	Φ180	Φ60	17	8	9.25	16	2.1	L

PROMOTION OF ENVIRONMENTAL MANAGEMENT SYSTEM CONFORMING TO INTERNATIONAL STANDARDS

At Seiko Epson, all environmental initiatives operate under the Plan-Do-Check-Action (PDCA) cycle designed to achieve continuous improvements. The environmental management system (EMS) operates under the ISO 14001 environmental management standard.

All of our major manufacturing and non-manufacturing sites, in Japan and overseas, completed the acquisition of ISO 14001 certification.

ISO 14000 is an international standard for environmental management that was established by the International Standards Organization in 1996 against the background of growing concern regarding global warming, destruction of the ozone layer, and global deforestation.

WORKING FOR HIGH QUALITY

In order provide high quality and reliable products and services than meet customer needs,

Seiko Epson made early efforts towards obtaining ISO9000 series certification and has acquired ISO9001 for all business establishments in Japan and abroad. We have also acquired ISO/TS 16949 certification that is requested strongly by major automotive manufacturers as standard.

ISO/TS16949 is the international standard that added the sector-specific supplemental requirements for automotive industry based on ISO9001.

► Explanation of the mark that are using it for the catalog

	► Pb free.
	► Complies with EU RoHS directive. *About the products without the Pb-free mark. Contains Pb in products exempted by EU RoHS directive. (Contains Pb in sealing glass, high melting temperature type solder or other.)
	► Designed for automotive applications such as Car Multimedia, Body Electronics, Remote Keyless Entry etc.
	► Designed for automotive applications related to driving safety (Engine Control Unit, Air Bag, ESC etc).

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