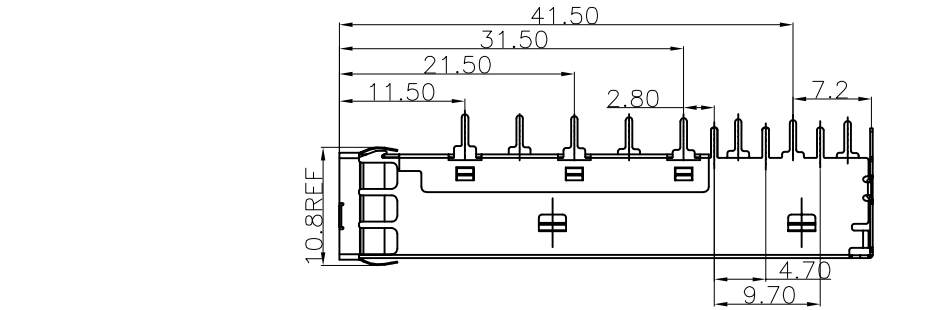
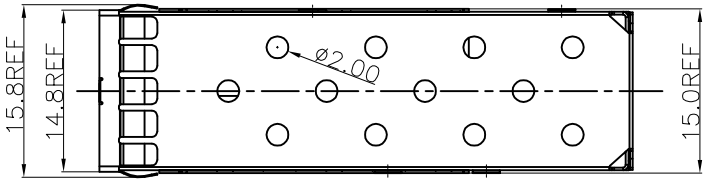
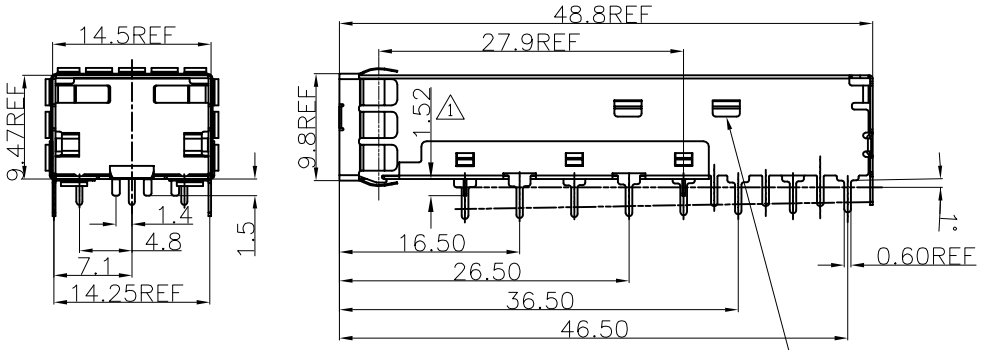
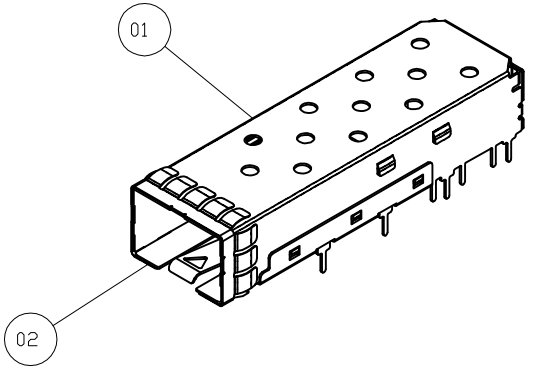
REVISION RECORD		
REV	DESCRIPTION	DRFT
1	UPDATE DIM	Jack 8/05/11'
2	MODIFY NI PLATING SPEC.	Jack 11/11/11'
3	ADD DIMENSION 1.50	Roy 7/03/13'









NOTE:

1.DESCRIPATION

	Q'ty	MATERIAL	PLATING
01 SFP TOP CAGE (Non-Logo)	1PCS	COPPER	MATT NICKLE
02 SFP BOTTOM CAGE (Non-Logo)	1PCS	COPPER	MATT NICKLE

2. PLATED: PLATED NICKEL 50u"-350u" Max

3. TEMPERATURE:
   OPERATION: -40°C~ +85°C
   STORAGE: -40°C~ +85°C

4. RoHS COMPLIANT

PART NUMBER
SFPPCAGE001-02-L

DETACHED LISTS

MM (INCH)

TOLERANCES EXCEPT AS NOTED

MM
.0 ± 0.25 ±
.00 ± 0.20 ±
.000 ± 0.10 ±

ANGLES ± 0.5°

THIRD ANGLE PROJECTION

RoHS Compliant

DFTD PETER	DATE 6/11/08'	
CHKD	DATE	
APPVL	DATE	

SCALE : 1:1

Pulse Electronics FULL RISE ELECTRONIC CO., LTD

TITLE THROUGH HOLE

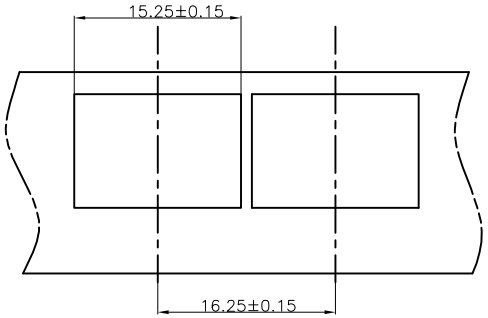
EMI SFP CAGE ENHANCED FOR PCI

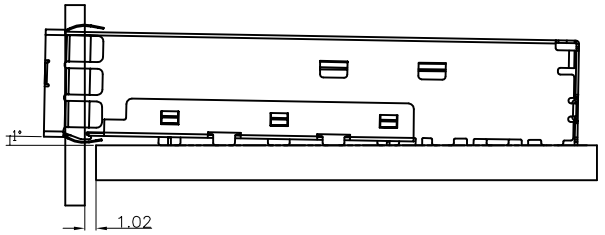
DRAWING NO. CSFPPCAGE001-02-L SIZE A3 REV 3

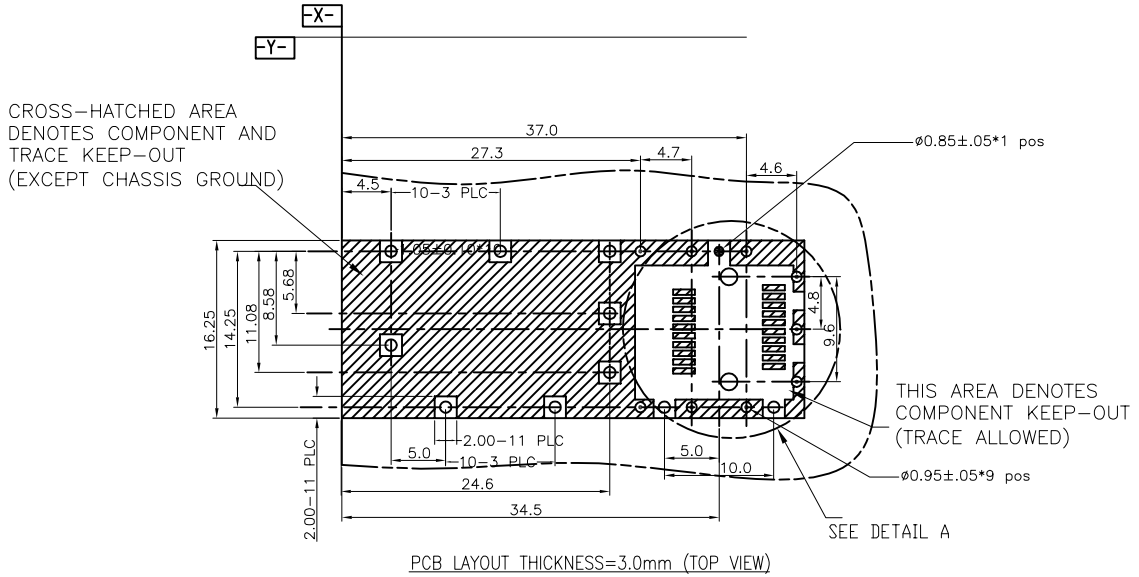
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DO NOT SCALE DRAWING SHEET 1 OF 2

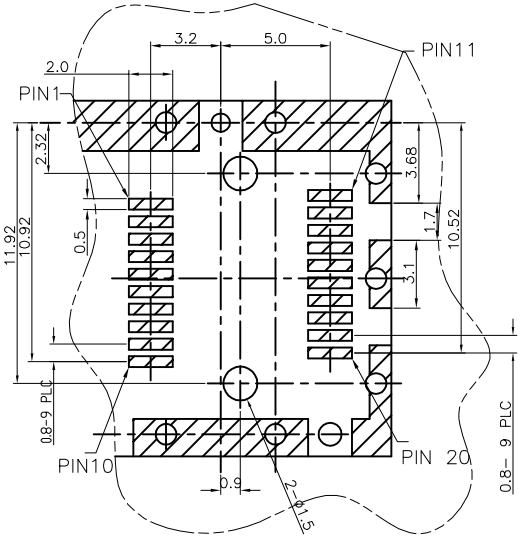
REVISION RECORD		
REV	DESCRIPTION	DRFT
1	UPDATE DIM	Jack 8/05/11'
2	MODIFY NI PLATING SPEC.	Jack 11/11/11'
3	ADD DIMENSION 1.50	Roy 7/03/13'







PCB LAYOUT THICKNESS=3.0mm (TOP VIEW)



DETAIL A
SCALE 2:1

⊡ ø1.05 * 10
⊙ ø0.95 * 9
● ø0.85 * 1

Suggestion: Through hole is ø0.85 +0.05/−0

DETACHED LISTS

MM (INCH)

TOLERANCES EXCEPT AS NOTED

MM	
.0 ± 0.25	±
.00 ± 0.20	±
.000 ± 0.10	±
ANGLES ± 0.5°	

THIRD ANGLE PROJECTION

RoHS Compliant

Pulse Electronics | FULL RISE ELECTRONIC CO., LTD

DFTD	PETER	DATE	6/11/08'
CHKD		DATE	
APPVL		DATE	

SCALE : 1:1

TITLE: THROUGH HOLE

EMI SFP CAGE ENHANCED FOR PCI

DRAWING NO.	CSFPPCAGE001-02-L	SIZE	REV
/PART NO.	SFPPCAGE001-02-L	A3	3

DO NOT SCALE DRAWING | SHEET 2 OF 2