

### Applications

- SONET/SDH-based transmission systems, test equipment and modules
- OC-48 fibre optic modules and line termination
- ATM over SONET/SDH
- Gigabit Ethernet
- Fibre Channel

### Features

- Single +3.3 V power supply
- Power dissipation = 110 mW (typ)
- Input noise current = 360 nA rms when used with a 0.5 pF detector
- Transimpedance gain = 2.3 k $\Omega$  into a 50  $\Omega$  load (differential)
- On-chip automatic gain control gives input current overload of 2.6 mA pk and max output voltage swing of 300 mV pk-pk
- Differential 50  $\Omega$  outputs
- Bandwidth (-3 dB) = 2.4 GHz
- Wide data rate range = 50 Mb/s to 2.5 Gb/s
- Constant photodiode reverse bias voltage = 1.5 V (anode to input, cathode to VCC)
- Minimal external components, supply decoupling only
- Operating junction temperature range = -40°C to +125°C
- Equivalent to Nortel Networks AB89-A4A

### Product Description

SiGe Semiconductor offers a portfolio of optical networking ICs for use in high-performance optical transmitter and receiver functions, from 155 Mb/s up to 12.5 Gb/s.

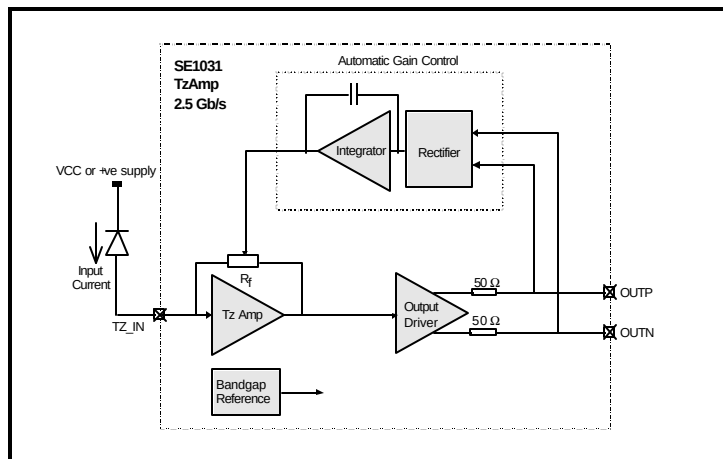
SiGe Semiconductor's SE1031 is a fully integrated, silicon bipolar transimpedance amplifier; providing wideband, low noise preamplification of signal current from a photodetector. It features differential outputs, and incorporates an automatic gain control mechanism to increase dynamic range, allowing input signals up to 2.6 mA peak. A decoupling capacitor on the supply is the only external circuitry required. A system block diagram is shown after the functional description, on page 3.

Noise performance is optimized for 2.5 Gb/s operation, with a calculated rms noise based sensitivity of -26 dBm for 10<sup>-10</sup> bit error rate, achieved using a detector with 0.5 pF capacitance and a responsivity of 0.9 A/W, with an infinite extinction ratio source.

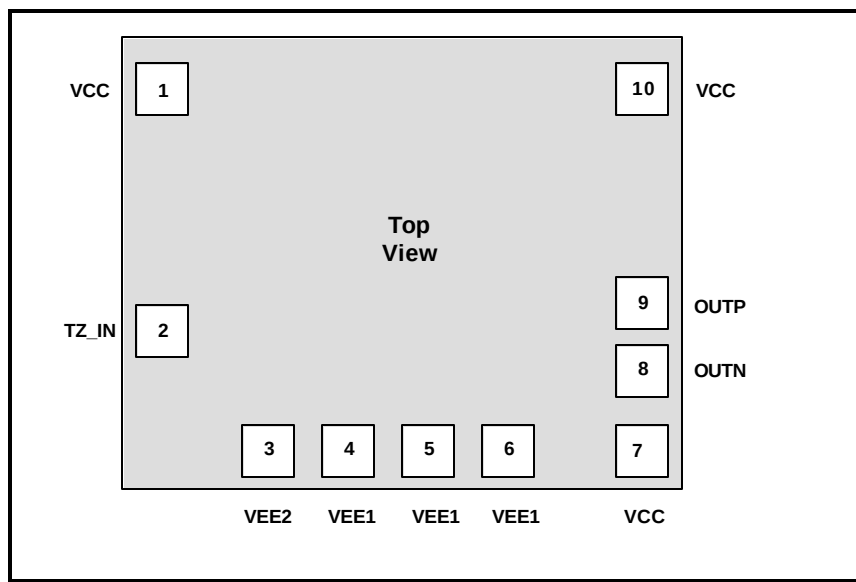
### Ordering Information

| Type    | Package  | Remark |
|---------|----------|--------|
| SE1031W | Bare Die | None   |

### Functional Block Diagram



## Bondpad Diagram



## Bondpad Description

| Pad No. | Name  | Description                                                                                                                                    |
|---------|-------|------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | VCC   | Positive supply (+3.3 V), pads 1, 7 & 10 are connected on chip. Only one pad needs to be bonded.                                               |
| 2       | TZ_IN | Input pad (connect to photodetector anode).                                                                                                    |
| 3       | VEE2  | Negative supply (0V) – Note this is separate ground for the input stage, which is AC coupled on chip. There is no DC current through this pad. |
| 4       | VEE1  | Negative supply (0V), pads 4, 5 & 6 are connected on chip. Only one pad needs to be bonded.                                                    |
| 5       | VEE1  | Negative supply (0V), pads 4, 5 & 6 are connected on chip. Only one pad needs to be bonded.                                                    |
| 6       | VEE1  | Negative supply (0V), pads 4, 5 & 6 are connected on chip. Only one pad needs to be bonded.                                                    |
| 7       | VCC   | Positive supply (+3.3 V), pads 1, 7 & 10 are connected on chip. Only one pad needs to be bonded.                                               |
| 8       | OUTN  | Negative differential voltage output.                                                                                                          |
| 9       | OUTP  | Positive differential voltage output.                                                                                                          |
| 10      | VCC   | Positive supply (+3.3 V), pads 1, 7 & 10 are connected on chip. Only one pad needs to be bonded.                                               |

## Functional Description

### Amplifier front-end

The transimpedance front-end amplifies an input current from a photodetector, at pin TZ\_IN, to produce a differential output voltage with the feedback resistor  $R_f$  determining the level of amplification (see the functional block diagram on page 1). An automatic gain control loop varies this resistor, to ensure that the output from the front-end does not saturate the output driver stage that follows. This gain control allows input signals of up to 2.6 mA peak.

The input pin TZ\_IN is biased at 1.5 V below the supply voltage VCC, allowing a photodetector to have a constant reverse bias by connecting the cathode to 3.3 V. This enables full single rail operation.

The front-end stage has its own supply ground connection (VEE2) to achieve optimum noise performance and maintain integrity of the high-speed signal path. The front-end shares the VCC (+3.3 V)

connection with the remainder of the circuitry, which has a separate ground (VEE1).

### Output driver stage

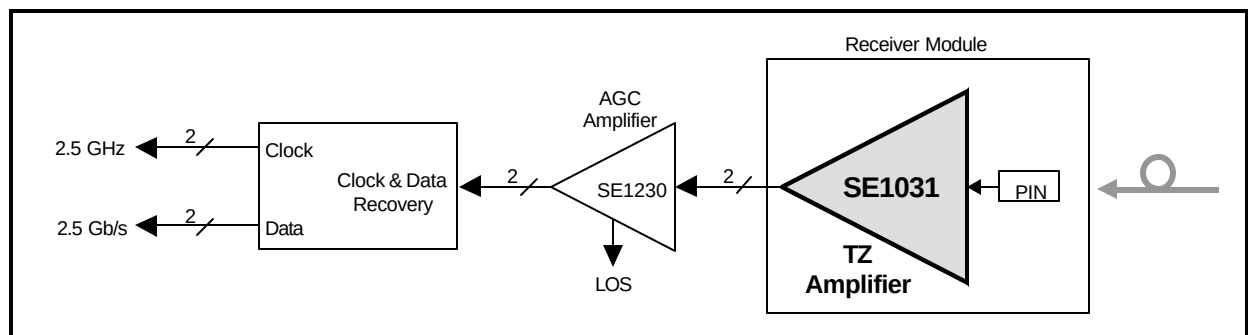
The output driver acts as a buffer stage, capable of swinging up to 300 mVpk-pk differential into a  $100\ \Omega$  load. The small output swings allow ease of use with low voltage post amplifiers (e.g. 3.3 V parts). Increasing optical input level gives a positive-going output signal on the OUTP pin.

### Automatic Gain Control (AGC)

The AGC circuit monitors the voltages from the output driver and compares them to an internal reference level produced via the on-chip bandgap reference circuit. When this level is exceeded, the gain of the front-end is reduced by controlling the feedback resistor  $R_f$ .

A long time-constant integrator is used within the control loop of the AGC with a typical low frequency cut-off of 10 kHz.

## System Block Diagram



## Absolute Maximum Ratings

These are stress ratings only. Exposure to stresses beyond these maximum ratings may cause permanent damage to, or affect the reliability of the device. Avoid operating the device outside the recommended operating conditions defined below.

| Symbol           | Parameter                                             | Min   | Max     | Unit |
|------------------|-------------------------------------------------------|-------|---------|------|
| VCC              | Supply Voltage                                        | −0.7  | 6.0     | V    |
| V <sub>IO</sub>  | Voltage at any input or output                        | −0.5  | VCC+0.5 | V    |
| I <sub>IO</sub>  | Current sourced into any input or output except TZ_IN | −20   | 20      | mA   |
| I <sub>IO</sub>  | Current sourced into pin TZ_IN                        | −5    | 5       | mA   |
| V <sub>ESD</sub> | Electrostatic Discharge (100 pF, 1.5 kΩ) except TZ_IN | −2    | 2       | kV   |
| V <sub>ESD</sub> | Electrostatic Discharge (100 pF, 1.5 kΩ) pin TZ_IN    | −0.25 | 0.25    | kV   |
| Tstg             | Storage Temperature                                   | −65   | 150     | °C   |

## Recommended Operating Conditions

| Symbol         | Parameter                      | Min | Typ | Max | Unit |
|----------------|--------------------------------|-----|-----|-----|------|
| VCC            | Supply Voltage                 | 3.1 | 3.3 | 3.5 | V    |
| T <sub>J</sub> | Operating Junction Temperature | −40 |     | 125 | °C   |

## DC Electrical Characteristics

| Symbol           | Parameter                           | Min      | Typ      | Max      | Unit     |
|------------------|-------------------------------------|----------|----------|----------|----------|
| ICC max          | Supply Current (max input current)  |          | 41       | 65       | mA       |
| ICC zero         | Supply Current (zero input current) |          | 33       | 52       | mA       |
| I <sub>agc</sub> | AGC Threshold                       | 42       |          |          | μA pk-pk |
| V <sub>in</sub>  | Input Bias Voltage                  | VCC−1.57 | VCC−1.52 | VCC−1.47 | V        |
| V <sub>out</sub> | Output Bias Voltage                 |          | VCC−0.15 |          | V        |
| R <sub>out</sub> | Output Resistance                   | 35       | 50       | 65       | Ω        |

## AC Electrical Characteristics

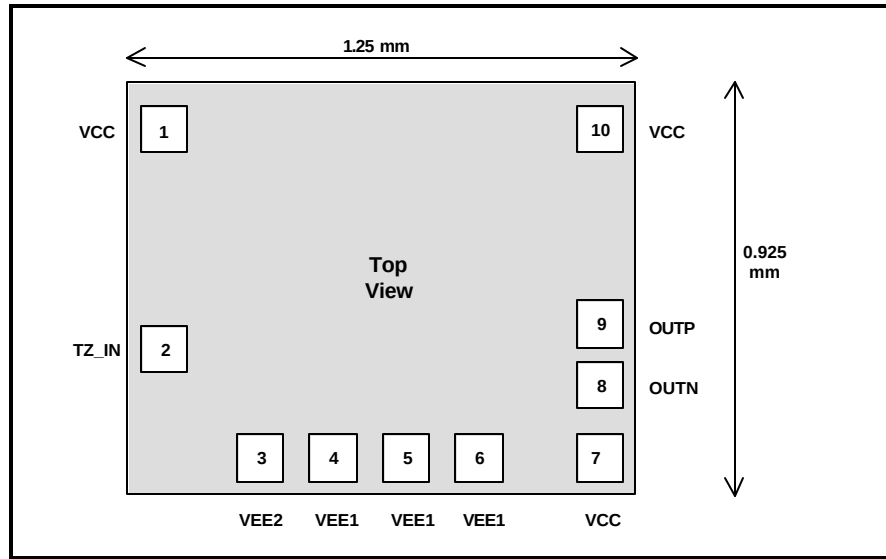
| Symbol          | Parameter                                                                                          | Min  | Typ | Max  | Unit          |
|-----------------|----------------------------------------------------------------------------------------------------|------|-----|------|---------------|
| BW (3dB)        | Small Signal Bandwidth at –3dB point                                                               | 1.8  | 2.4 |      | GHz           |
| Tz              | Differential Transimpedance (50 $\Omega$ on each output, f = 100 MHz)                              | 1.6  | 2.3 | 3.1  | k $\Omega$    |
| Dri             | Input Data Rate                                                                                    | 50   |     | 2500 | Mb/s          |
| Voutmax         | Maximum Differential Output Voltage                                                                |      |     | 300  | mV pk-pk      |
| Flf             | Low Frequency Cut-off                                                                              |      | 10  | 20   | kHz           |
| I <sub>OL</sub> | Input Current before overload (2.5 Gb/s NRZ data)                                                  | 2600 |     |      | $\mu$ A pk-pk |
| Pol             | Optical Overload                                                                                   | +1.6 |     |      | dBm           |
| Nrms            | Input Noise Current (in 2 GHz)                                                                     |      | 360 | 500  | nA rms        |
| Sens            | Optical Sensitivity [ calculated from input noise spectral density only, (10 <sup>-10</sup> BER) ] |      | –26 |      | dBm           |

DC and AC electrical characteristics are specified under the following conditions:

Supply Voltage (VCC).....3.1 V to 3.5 V  
Junction Temperature (Tj).....–40°C to 125°C  
Load Resistor (R<sub>L</sub>).....50  $\Omega$  AC coupled via 220 nF, for each output  
Photodetector Capacitance (Cd).....0.5 pF  
Input bond wire inductance .....1 nH  
Photodetector responsivity.....0.9 A/W  
Transimpedance (Tz) measured with 4  $\mu$ A mean photocurrent

## Bondpad Configuration

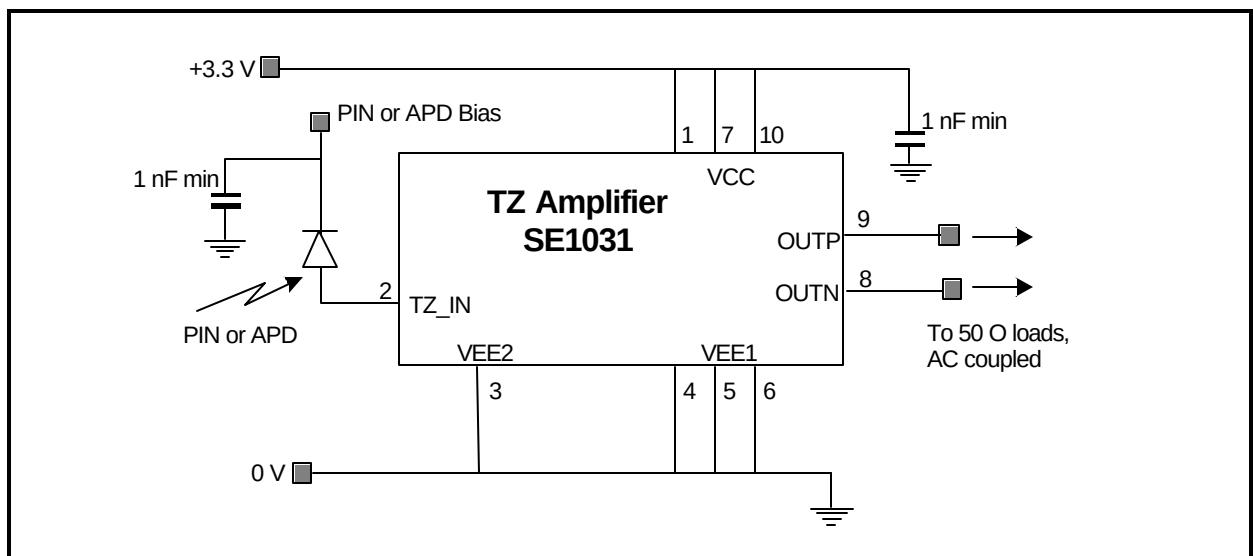
The diagram below shows the bondpad configuration of the SE1031 Transimpedance Amplifier: Note that the diagram is not to scale. Bondpad openings are  $82\ \mu\text{m} \times 82\ \mu\text{m}$ . There are three VCC and three VEE1 pads for ease of wire bonding – the VCC and VEE1 pads respectively are connected on-chip and only one pad of each type is required to be bonded out.



## Applications Information

For optimum performance it is recommended that the device be used in differential mode with the circuit shown in the diagram below.

Note that all VCC pads (1, 7, 10) are connected on-chip, as are the VEE1 pads (4, 5, 6), and only one pad of each type is required to be bonded out. However, in order to minimize inductance for optimum high speed performance, it is recommended that all power pads are wire bonded. The VEE2 pad is not connected on chip to VEE1 and must be bonded out separately.



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Product Preview

The datasheet contains information from the product concept specification. SiGe Semiconductor reserves the right to change information at any time without notification.

Preliminary

The datasheet contains information from the design target specification. SiGe Semiconductor reserves the right to change information at any time without notification.

Final

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