LPC IO with 8042 KBC, Reset Generation, HWM and Multiple Serial Ports

Product Features

- General Features
  - 3.3 Volt Operation (SIO Block is 5 Volt Tolerant)
  - Programmable Wake-up Event (PME) Interface
  - PC99, PC2001 Compliant
  - ACPI 2.0 Compliant
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - ISA Plug-and-Play Compatible Register Set
  - Four Address Options for Power On Configuration Port
  - System Management Interrupt (SMI)
  - General Purpose I/O pins: see Table 1-1
  - GPIOs with VID compatible inputs: see Table 1-1
  - Support for power button on PS/2 Keyboard
  - Security Key Register (32 byte) for Device Authentication
- Low Pin Count Bus (LPC) Interface
  - Supports Bus frequencies of 19MHz to 33MHz
- Watchdog Timer
- Resume and Main Power Good Generator
- Programmable Clock Output to 16 Hz
- Keyboard Controller
  - 8042 Software Compatible
  - 8 Bit Microcomputer
  - 2k Bytes of Program ROM
  - 256 Bytes of Data RAM
  - Four Open Drain Outputs Dedicated for Keyboard/Mouse Interface
  - Asynchronous Access to Two Data Registers and One Status Register
  - Supports Interrupt and Polling Access
  - 8 Bit Counter Timer
  - Port 92 Support
  - Fast Gate A20 and KRESET Outputs
  - Phoenix Keyboard BIOS ROM
- Multiple Serial Ports
  - 4 Full Function Serial Ports (SCH3227, SCH3226, SCH3222)
  - 2 Full Function Serial Ports (SCH3224)
  - Two additional 4-pin Serial Ports available by strap option (SCH3227, SCH3226)
  - Two additional 4-pin Serial Ports available always (SCH3224, SCH3222)
  - High Speed NS16C550A Compatible UARTs with Send/Receive 16-Byte FIFOs
  - Supports 230k, 460k, 921k and 1.5M Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
  - 480 Address and 15 IRQ Options
  - Support IRQ Sharing among serial ports
  - RS485 Auto Direction Control Mode
- Infrared Port
  - Multiprotocol Infrared Interface
  - IrDA 1.0 Compliant
  - SHARP ASK IR
  - 480 Addresses, Up to 15 IRQ
- Multi-Mode™ Parallel Port with ChiProtect™
  - Available in SCH3227, SCH3224
  - Standard Mode IBM PC/XT®, PC/AT®, and PS/2™ Compatible Bi-directional ParallelPort
  - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - ChiProtect Circuitry for Protection
  - 960 Address, Up to 15 IRQ and Four DMA Options
- Hardware Monitor
  - Available in SCH3227, SCH3226, SCH3224
  - Monitor Power supplies (+2.5V, +5V, +12V, Vccp (processor voltage), VCC, Vbat and Vtr.
  - Remote Thermal Diode Sensing for Two External Temperature Measurements accurate to 1.5°C
  - Internal Ambient Temperature Measurement
  - Limit Comparison of all Monitored Values
  - Programmable Automatic FAN control based on temperature
  - nHWM_INT Pin for out-of-limit Temperature or Voltage Indication
  - Thermtrip signal for over temperature indication
- IDE Reset Output and 3 PCI Reset Buffers with Software Control Capability (SCH3227 and SCH3226 by strap option)
- Power Button Control and AC Power Failure Recovery (SCH3227 and SCH3226 by strap option)
- Temperature Ranges Available
  - Industrial (+85°C to -40°C)
  - Commercial (+70°C to 0°C)
- WFBGA RoHS Compliant Packages
  - 144-ball (SCH3227)
  - 100-ball (SCH3226, SCH3224)
  - 84-ball (SCH3222)

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1.0 INTRODUCTION

1.1 General Description

The SCH3227/SCH3226/SCH3224/SCH3222 Product Family is a 3.3V (Super I/O Block is 5V tolerant) PC99/PC2001 compliant Super I/O controller with an LPC interface. The Product Family also includes Hardware Monitoring capabilities, enhanced Security features, Power Control logic and Motherboard Glue logic.

See Table 1-1 on page 4 for features available per family member.

The Product Family is ACPI 1.0/2.0 compatible and therefore supports multiple low power-down modes. It incorporates sophisticated power control circuitry (PCC), which includes support for keyboard.

The Product Family supports the ISA Plug-and-Play Standard register set (Version 1.0a). The I/O Address, hardware IRQ and DMA Channel of each Logical Device may be reprogrammed through the internal configuration registers. There are up to 480 I/O address location options (960 for the Parallel Port), a Serialized IRQ interface, and a choice of three Legacy DMA channel assignments.

Super I/O functionality includes an 8042 based keyboard and mouse controller, one IrDA 1.0 infrared port and multiple serial ports. Some family members (Table 1-1) also provide an IEEE 1284 EPP/ECP compatible parallel port.

The serial ports are fully functional NS16550 compatible UARTs that support data rates up to 1.5 Mbps. There are both 8-pin Serial Ports and 4-pin Serial Ports. The reduced-pin serial ports have selectable input and output controls. The Serial Ports contain programmable direction control, which will automatically drive nRTS when the Output Buffer is loaded, then drive nRTS when the Output Buffer is empty.

Hardware Monitoring capability has programmable, automatic fan control. Three fan tachometer inputs and three pulse width modulator (PWM) fan control outputs are available.

Hardware Monitoring capability also includes temperature, voltage and fan speed monitoring. It has the ability to alert the system to out-of-limit conditions and automatically control the speeds of multiple fans in response. There are four analog inputs for monitoring external voltages of +5V, +2.5V, +12V and Vccp (core processor voltage), as well as internal monitoring of the device's internal VCC, VTR, and VBAT power supplies. Hardware Monitoring includes support for monitoring two external temperatures via thermal diode inputs and an internal sensor for measuring local ambient temperature. The nHWM_INT pin is implemented to indicate out-of-limit temperature, voltage, and fan speed conditions. Hardware Monitoring features are accessible via the LPC bus, and the same interrupt event reported on the nHWM_INT pin also creates PME wakeup events. A separate THERMTRIP output is available, which generates a pulse output on a programmed over-temperature condition. This can be used to generate a reset or shutdown indication to the system.

The Motherboard Glue logic includes various power management and system logic including generation of nRSMRST, a programmable Clock output, and reset generation. The reset generation includes a watchdog timer which can be used to generate a reset pulse. The width of this pulse is selectable via an external strapping option.

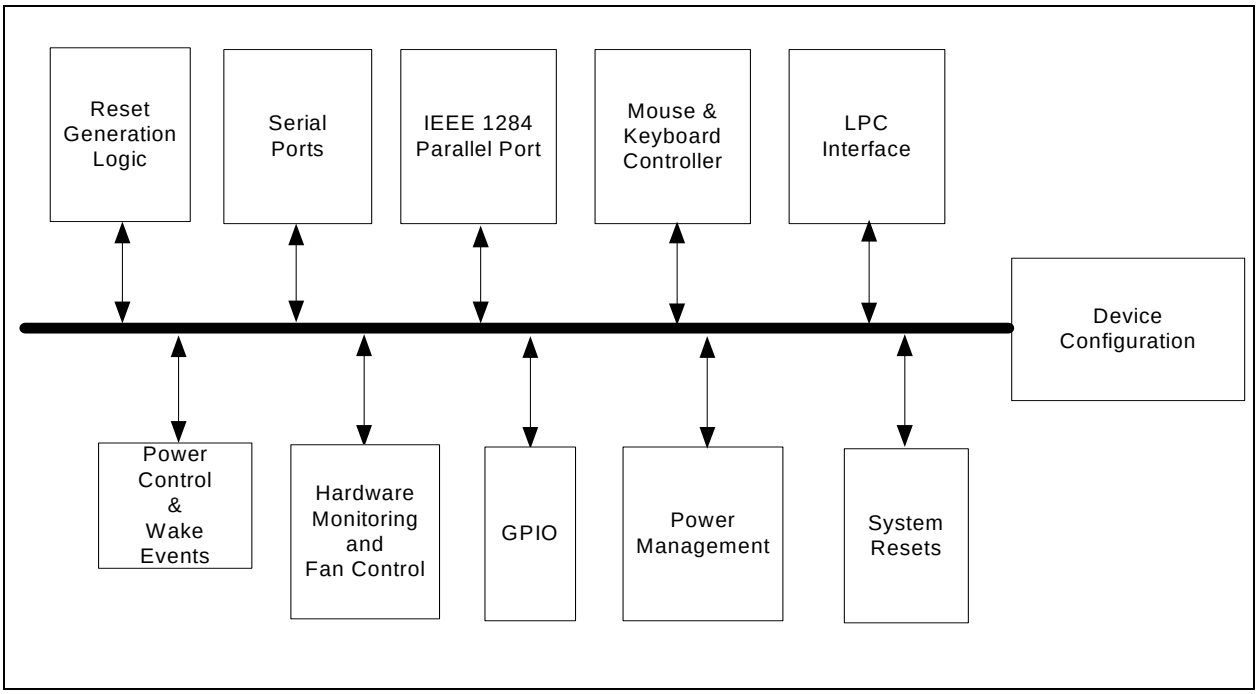
System related functionality, which offers flexibility to the system designer, includes General Purpose I/O control functions, and control of two LED's.

TABLE 1-1: DEVICE SPECIFIC SUMMARY

Function	SCH3227	SCH3226	SCH3224	SCH3222
LPC Bus Interface	YES	YES	YES	YES
PnP Config w/ 4 Port Addresses	YES	YES	YES	YES
Serial IRQ and SMI	YES	YES	YES	YES
Keyboard Controller	YES	YES	YES	YES
Watchdog Timer	YES	YES	YES	YES
Parallel Port	YES	NO	YES	NO
Reset Generator	YES	YES	YES	YES
Serial Ports, Full	4	4	2	4
Additional Serial Ports, 4-Pin	2 avail. (by strap option)	2 avail. (by strap option)	2	2
Infrared Port	YES	YES	YES	YES
Programmable Clock Output	YES	YES	YES	YES
IDE / PCI Reset Outputs	By strap option (vs. 4-pin Serial Ports).	By strap option (vs. 4-pin Serial Ports).	NO	NO
Power Button / AC Fail Support	By strap option (vs. 4-pin Serial Ports).	By strap option (vs. 4-pin Serial Ports).	NO	NO
GPIOs	40	40	24	23
GPIO with VID Compatible Inputs	6	6	0	6
Hardware Monitor	YES	YES	YES	NO
WFBGA Package	144-ball	100-ball	100-ball	84-ball

An internal block diagram of the SCH3227/SCH3226/SCH3224/SCH3222 Product Family is shown in Figure 1-1.

FIGURE 1-1: ARCHITECTURAL OVERVIEW



2.0 PACKAGE OUTLINES

FIGURE 2-1: SCH3227 144 WFBGA Package

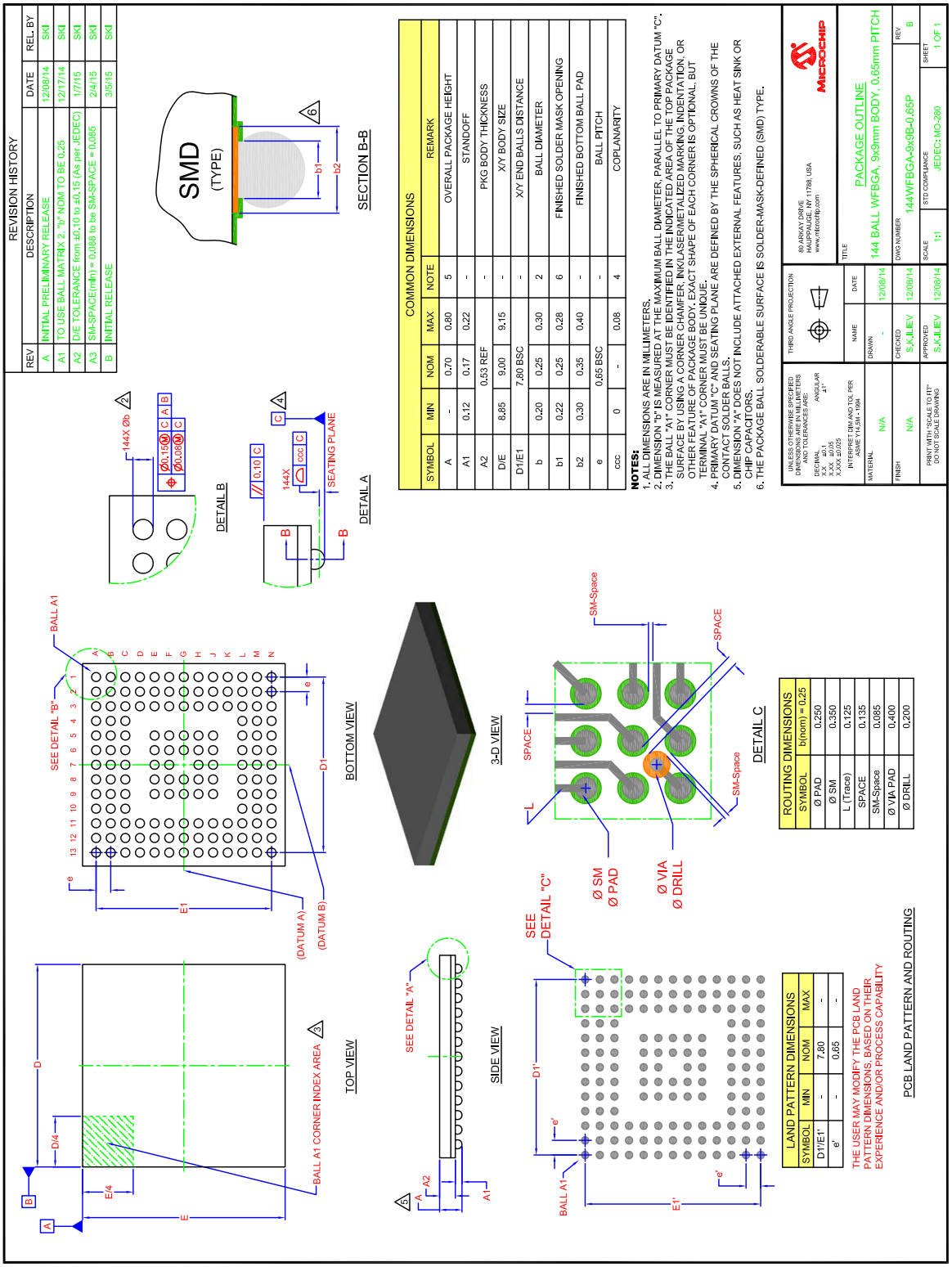


FIGURE 2-2: SCH3226, SCH3224 100 WFBGA Package

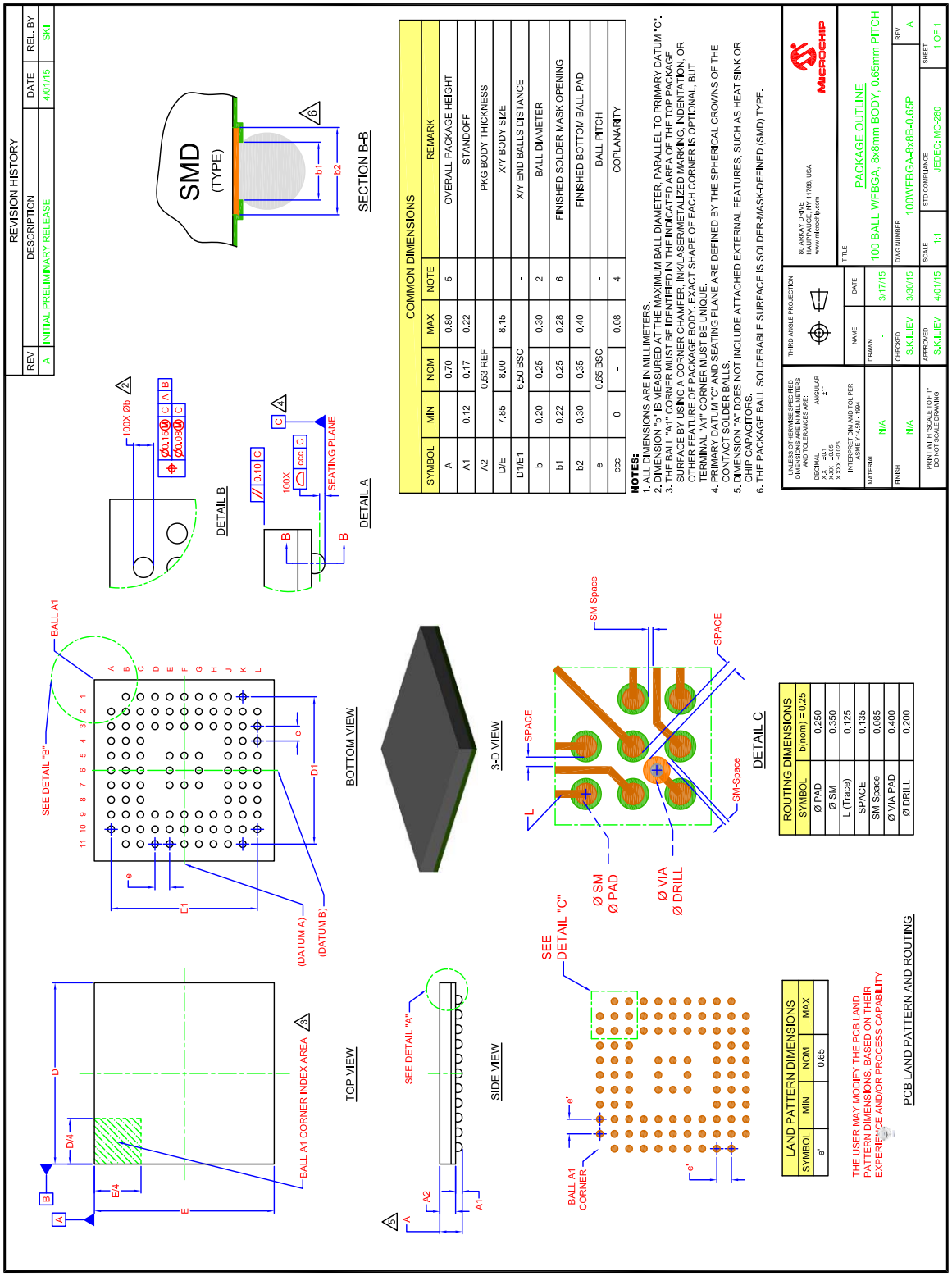
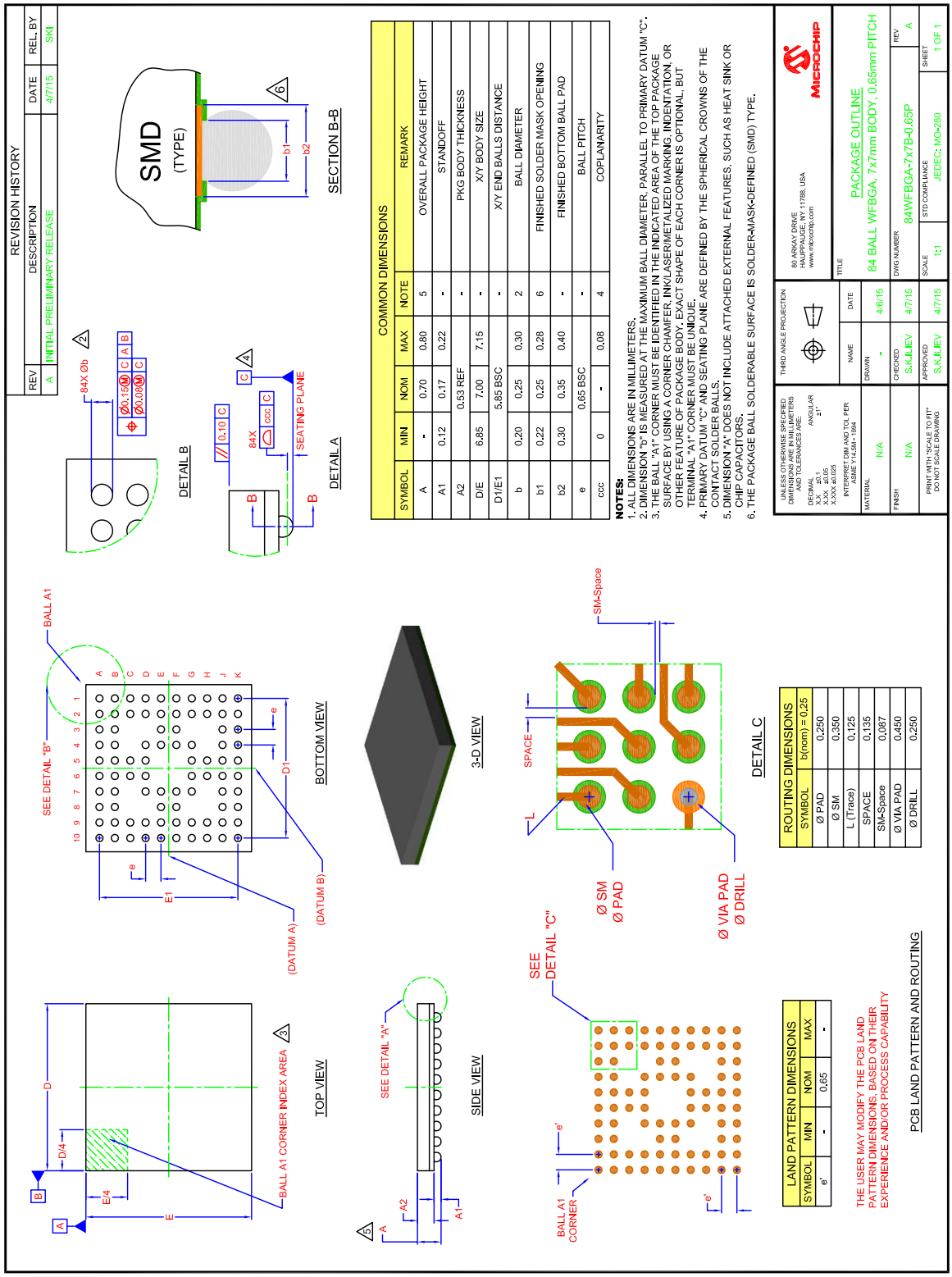


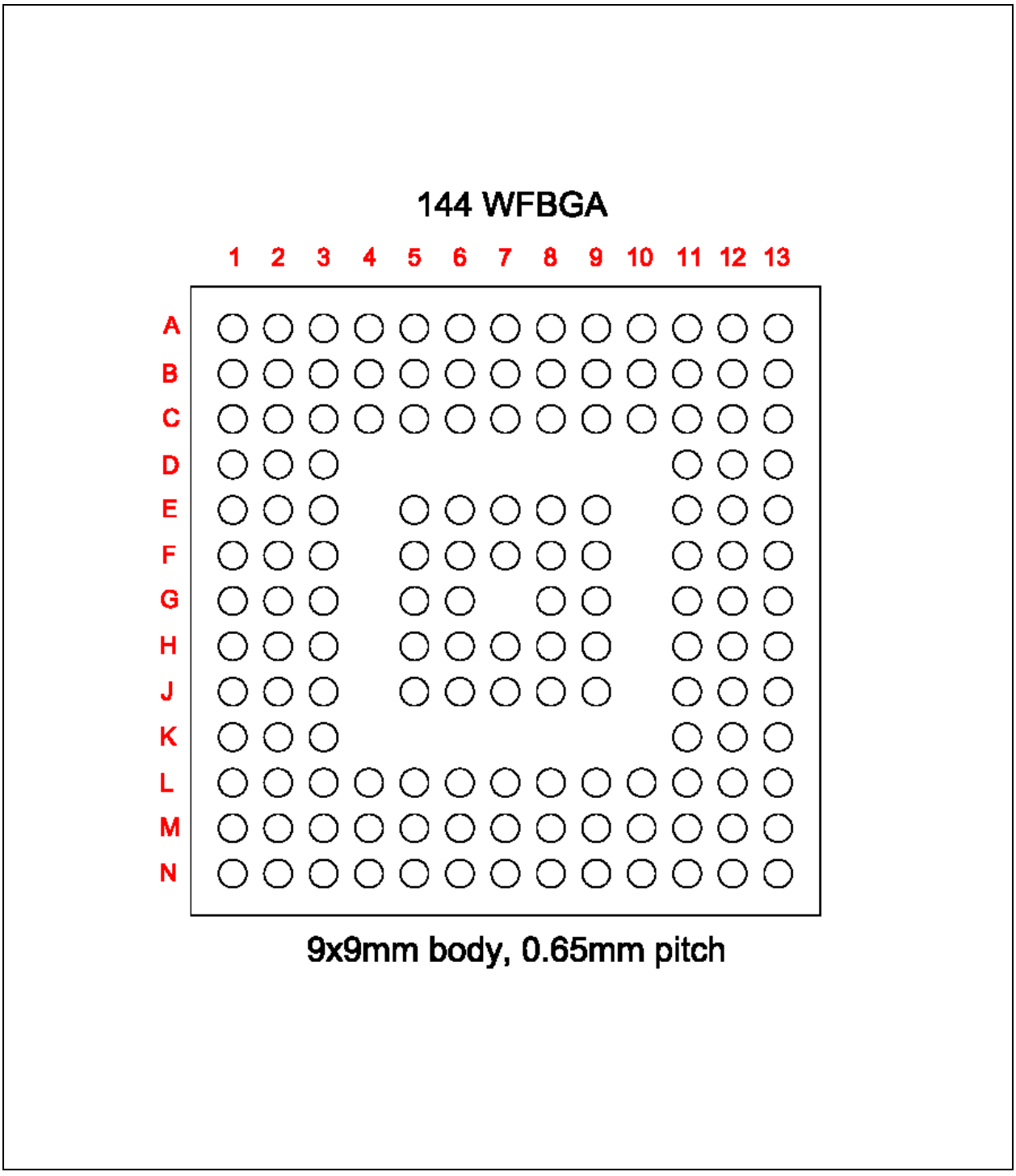
FIGURE 2-3: SCH3222 84 WFBGA Package



3.0 BALL LAYOUTS

3.1 SCH3227 Ball Layout Summary

FIGURE 3-1: SCH3227 FOOTPRINT DIAGRAM, TOP VIEW



Highlighted rows indicate balls whose function depends on the STRAPOPT strap input.

TABLE 3-1: SCH3227 SUMMARIES BY STRAP OPTION

BALL#	FUNCTION: STRAPOPT=1	FUNCTION: STRAPOPT=0
K13	STRAPOPT (=VTR[a])	STRAPOPT (=VSS[a])
M4	RESERVED=VTR[b]	RESERVED=VTR[b]
C3	+12V_IN	+12V_IN
D3	+5V_IN	+5V_IN
E6	GP40	GP40
E3	VTR	VTR
E5	RESERVED=VSS[c]	RESERVED=VSS[c]
F8	TEST=VSS[c]	TEST=VSS[c]
F7	RESERVED=VSS[c]	RESERVED=VSS[c]
F3	VSS	VSS
F6	RESERVED=VSS[c]	RESERVED=VSS[c]
F5	RESERVED=VSS[c]	RESERVED=VSS[c]
G8	RESERVED=VSS[c]	RESERVED=VSS[c]
G6	RESERVED=VSS[c]	RESERVED=VSS[c]
H8	RESERVED=VSS[c]	RESERVED=VSS[c]
G5	RESERVED=VSS[c]	RESERVED=VSS[c]
H7	RESERVED=VSS[c]	RESERVED=VSS[c]
H6	RESERVED=VSS[c]	RESERVED=VSS[c]
H5	RESERVED=VSS[c]	RESERVED=VSS[c]
D2	CLOCKI	CLOCKI
E2	LAD0	LAD0
D1	LAD1	LAD1
E1	LAD2	LAD2
F2	LAD3	LAD3
F1	LFRAME#	LFRAME#
G2	LDRQ#	LDRQ#
H1	PCI_RESET#	PCI_RESET#
G1	PCI_CLK	PCI_CLK
H2	SER_IRQ	SER_IRQ
H3	VSS	VSS
J3	VCC	VCC
J1	GP44 / TXD6	nIDE_RSTDRV / GP44
J2	GP45 / RXD6	nPCIRST1 / GP45
K3	GP46 / nSCIN6	nPCIRST2 / GP46
L3	GP47 / nSCOUT6	nPCIRST3 / GP47
K1	AVSS	AVSS
L1	VBAT	VBAT
K2	GP27 / nIO_SMI / P17	GP27 / nIO_SMI / P17
L2	KDAT / GP21	KDAT / GP21
M1	KCLK / GP22	KCLK / GP22
M2	MDAT / GP32	MDAT / GP32
N1	MCLK / GP33	MCLK / GP33
M3	GP36 / nKBDRST	GP36 / nKBDRST

TABLE 3-1: SCH3227 SUMMARIES BY STRAP OPTION (CONTINUED)

BALL#	FUNCTION: STRAPOPT=1	FUNCTION: STRAPOPT=0
N2	GP37 / A20M	GP37 / A20M
L5	VSS	VSS
N3	VTR	VTR
N4	nINIT	nINIT
M5	nSLCTIN	nSLCTIN
L6	PD0	PD0
N5	PD1	PD1
M6	PD2	PD2
L7	PD3	PD3
N6	PD4	PD4
M7	PD5	PD5
N7	PD6	PD6
L8	PD7	PD7
L9	VSS	VSS
M8	SLCT	SLCT
N8	PE	PE
N9	BUSY	BUSY
M9	nACK	nACK
N10	nERROR	nERROR
M10	nALF	nALF
N11	nSTROBE	nSTROBE
M11	nRI1	nRI1
N12	nDCD1	nDCD1
L11	RXD1	RXD1
M12	TXD1 / SIOXNOROUT	TXD1 / SIOXNOROUT
N13	nDSR1	nDSR1
L12	nRTS1 / SYSOPT0	nRTS1 / SYSOPT0
M13	nCTS1	nCTS1
J12	nDTR1 / SYSOPT1	nDTR1 / SYSOPT1
K12	GP50 / nRI2	GP50 / nRI2
L13	VTR	VTR
J13	VSS	VSS
H11	GP51 / nDCD2	GP51 / nDCD2
H12	GP52 / RXD2(IRRX2)	GP52 / RXD2(IRRX2)
H13	GP53 / TXD2(IRTX2)	GP53 / TXD2(IRTX2)
G13	GP54 / nDSR2	GP54 / nDSR2
G12	GP55 / nRTS2 / RESGEN	GP55 / nRTS2 / RESGEN
G11	GP56 / nCTS2	GP56 / nCTS2
F13	GP57 / nDTR2	GP57 / nDTR2
F12	RXD5	PB_OUT#
F11	TXD5	PS_ON#
E13	nSCOUT5	PB_IN#
E12	nSCIN5	SLP_SX#
D13	GP10 / RXD3	GP10 / RXD3

TABLE 3-1: SCH3227 SUMMARIES BY STRAP OPTION (CONTINUED)

BALL#	FUNCTION: STRAPOPT=1	FUNCTION: STRAPOPT=0
D12	GP11 / TXD3	GP11 / TXD3
E11	GP14 / nDSR3	GP14 / nDSR3
C13	GP17 / nRTS3	GP17 / nRTS3
B13	GP16 / nCTS3	GP16 / nCTS3
C12	GP42 / nIO_PME	GP42 / nIO_PME
D11	VTR	VTR
A13	GP15 / nDTR3	GP15 / nDTR3
B12	GP61 / nLED2 / CLKO	GP61 / nLED2 / CLKO
C11	GP60 / nLED1 / WDT	GP60 / nLED1 / WDT
A12	GP13 / nRI3	GP13 / nRI3
B11	GP12 / nDCD3	GP12 / nDCD3
A11	GP31 / nRI4	GP31 / nRI4
C10	GP63 / nDCD4	GP63 / nDCD4
B10	CLKI32	CLKI32
A10	nRSMRST	nRSMRST
B9	VSS	VSS
C9	GP64 / RXD4	GP64 / RXD4
A9	GP65 / TXD4	GP65 / TXD4
A8	GP66 / nDSR4	GP66 / nDSR4
B8	GP67 / nRTS4	GP67 / nRTS4
C8	GP62 / nCTS4	GP62 / nCTS4
A7	GP34 / nDTR4	GP34 / nDTR4
B7	PWRGD_OUT	PWRGD_OUT
A6	PWRGD_PS	PWRGD_PS
C7	nFPRST / GP30	nFPRST / GP30
E8	VTR	VTR
E7	VSS	VSS
B6	nTHERMTRIP	nTHERMTRIP
A5	nHWM_INT	nHWM_INT
C6	PWM3	PWM3
B5	PWM2	PWM2
A4	PWM1	PWM1
B4	FANTACH3	FANTACH3
C5	FANTACH2	FANTACH2
C4	FANTACH1	FANTACH1
A3	HVSS	HVSS
B3	HVTR	HVTR
A2	REMOTE2-	REMOTE2-
A1	REMOTE2+	REMOTE2+
B1	REMOTE1-	REMOTE1-
C1	REMOTE1+	REMOTE1+
C2	VCCP_IN	VCCP_IN
B2	+2.5V_IN	+2.5V_IN
--	RESERVED=N/C[d]: E9, F9, G9, H9, J5, J6, J7, J8, J9, G3, J11, K11, L4, L10	

a. The STRAPOPT connection defines pin functions for this package, and also the contents of the Device ID register at Plug&Play Index 0x20:
   When connected to VTR, the table column STRAPOPT=1 applies,
   and Device ID = 0x7F.
   When connected to VSS, the table column STRAPOPT=0 applies,
   and Device ID = 0x7D.

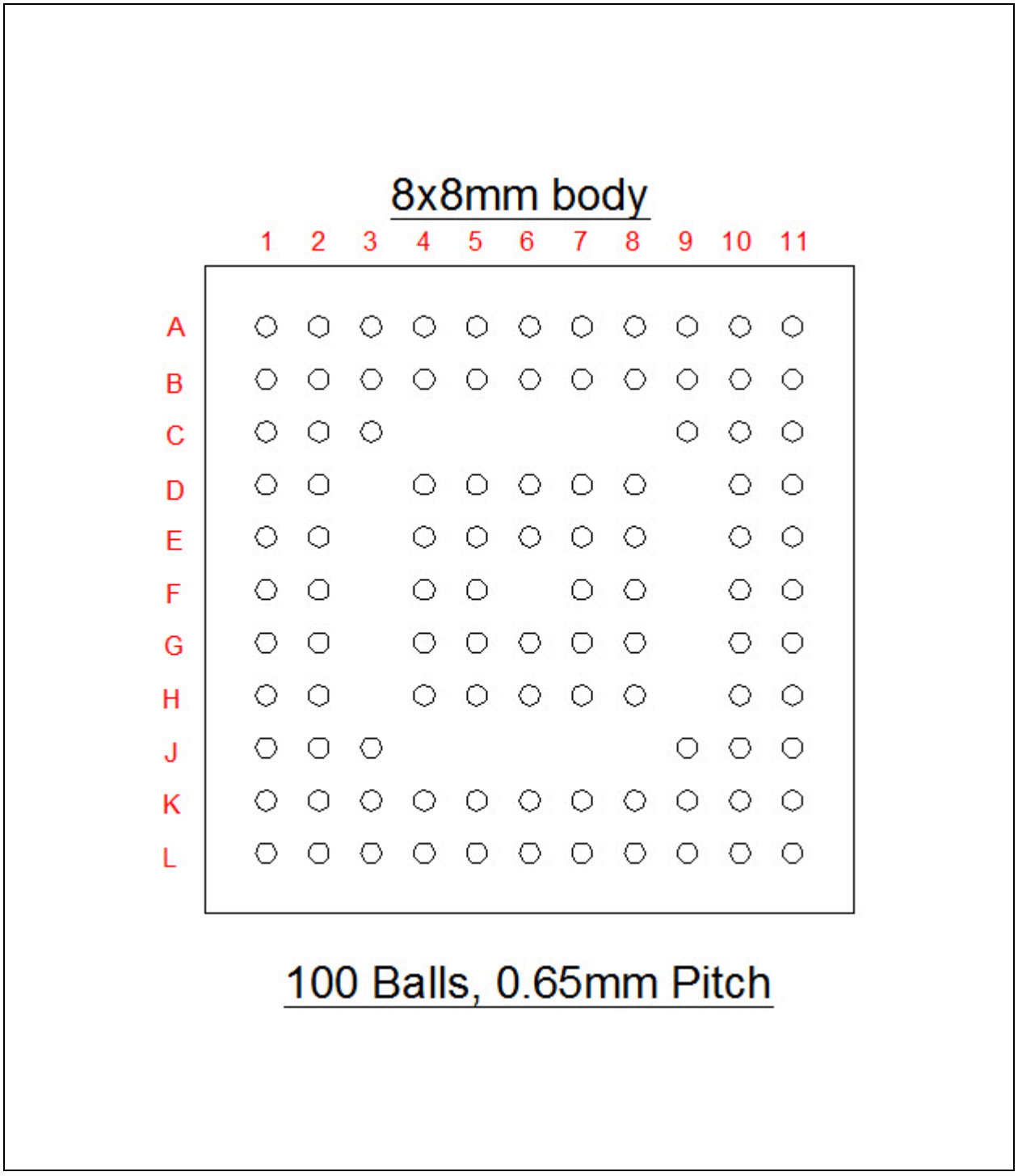
b. For correct operation, this lead must always be connected to VTR.

c. For correct operation and minimal current consumption, this lead must always be connected to VSS.

d. Make No Connection to these leads.

3.2 SCH3226 Ball Layout Summary

FIGURE 3-2: SCH3226 FOOTPRINT DIAGRAM, TOP VIEW



Highlighted rows indicate balls whose function depends on the STRAPOPT strap input.

TABLE 3-2: SCH3226 SUMMARIES BY STRAP OPTION

BALL#	FUNCTION: STRAPOPT=1	FUNCTION: STRAPOPT=0
L8	STRAPOPT (=VTR[a])	STRAPOPT (=VSS[a])
C2	+12V_IN	+12V_IN
C1	+5V_IN	+5V_IN
C3	GP40 / DRVDEN0(out)	GP40 / DRVDEN0(out)
D3	VTR	VTR
G5	TEST	TEST
D2	VSS	VSS
E3	CLOCKI	CLOCKI
F3	LAD0	LAD0
E2	LAD1	LAD1
D1	LAD2	LAD2
F2	LAD3	LAD3
E1	LFRAME#	LFRAME#
G3	LDRQ#	LDRQ#
F1	PCI_RESET#	PCI_RESET#
G1	PCI_CLK	PCI_CLK
G2	SER_IRQ	SER_IRQ
H1	VSS	VSS
H2	VCC	VCC
H3	GP44 / TXD6	nIDE_RSTDRV / GP44
J2	GP45 / RXD6	nPCIRST1 / GP45
K2	GP46 / nSCIN6	nPCIRST2 / GP46
J3	GP47 / nSCOUT6	nPCIRST3 / GP47
J1	AVSS	AVSS
K1	VBAT	VBAT
K3	GP27 / nIO_SMI / P17	GP27 / nIO_SMI / P17
J4	KDAT / GP21	KDAT / GP21
L2	KCLK / GP22	KCLK / GP22
L3	MDAT / GP32	MDAT / GP32
K4	MCLK / GP33	MCLK / GP33
L4	GP36 / nKBDRST	GP36 / nKBDRST
L5	GP37 / A20M	GP37 / A20M
G7	VSS	VSS
G6	VTR	VTR
K7	nRI1	nRI1
L6	nDCD1	nDCD1
K8	RXD1	RXD1
J8	TXD1 / SIOXNOROUT	TXD1 / SIOXNOROUT
K6	nDSR1	nDSR1
K5	nRTS1 / SYSOPT0	nRTS1 / SYSOPT0
J7	nCTS1	nCTS1
J6	nDTR1 / SYSOPT1	nDTR1 / SYSOPT1
J5	GP50 / nRI2	GP50 / nRI2

TABLE 3-2: SCH3226 SUMMARIES BY STRAP OPTION

BALL#	FUNCTION: STRAPOPT=1	FUNCTION: STRAPOPT=0
L9	VTR	VTR
L7	VSS	VSS
K9	GP51 / nDCD2	GP51 / nDCD2
J9	GP52 / RXD2(IRRX2)	GP52 / RXD2(IRRX2)
H9	GP53 / TXD2(IRTX2)	GP53 / TXD2(IRTX2)
G9	GP54 / nDSR2	GP54 / nDSR2
L10	GP55 / nRTS2 / RESGEN	GP55 / nRTS2 / RESGEN
K10	GP56 / nCTS2	GP56 / nCTS2
J10	GP57 / nDTR2	GP57 / nDTR2
H10	RXD5	PB_OUT#
K11	TXD5	PS_ON#
J11	nSCOUT5	PB_IN#
H11	nSCIN5	SLP_SX#
F9	GP10 / RXD3	GP10 / RXD3
G10	GP11 / TXD3	GP11 / TXD3
E9	GP14 / nDSR3	GP14 / nDSR3
F10	GP17 / nRTS3	GP17 / nRTS3
G11	GP16 / nCTS3	GP16 / nCTS3
F11	GP42 / nIO_PME	GP42 / nIO_PME
E10	VTR	VTR
E11	GP15 / nDTR3	GP15 / nDTR3
D9	GP61 / nLED2 / CLKO	GP61 / nLED2 / CLKO
D10	GP60 / nLED1 / WDT	GP60 / nLED1 / WDT
D11	GP13 / nRI3	GP13 / nRI3
C11	GP12 / nDCD3	GP12 / nDCD3
C10	GP31 / nRI4	GP31 / nRI4
C9	GP63 / nDCD4	GP63 / nDCD4
B11	CLKI32	CLKI32
B10	nRSMRST	nRSMRST
A10	VSS	VSS
C8	GP64 / RXD4	GP64 / RXD4
B9	GP65 / TXD4	GP65 / TXD4
A9	GP66 / nDSR4	GP66 / nDSR4
B8	GP67 / nRTS4	GP67 / nRTS4
A8	GP62 / nCTS4	GP62 / nCTS4
C7	GP34 / nDTR4	GP34 / nDTR4
A7	PWRGD_OUT	PWRGD_OUT
B7	PWRGD_PS	PWRGD_PS
E7	nFPRST / GP30	nFPRST / GP30
F7	VTR	VTR
C6	VSS	VSS
B6	nTHERMTRIP	nTHERMTRIP
E6	nHWM_INT	nHWM_INT
A6	PWM3	PWM3

TABLE 3-2: SCH3226 SUMMARIES BY STRAP OPTION

BALL#	FUNCTION: STRAPOPT=1	FUNCTION: STRAPOPT=0
F5	PWM2	PWM2
A5	PWM1	PWM1
E5	FANTACH3	FANTACH3
B5	FANTACH2	FANTACH2
C5	FANTACH1	FANTACH1
B4	HVSS	HVSS
C4	HVTR	HVTR
A4	REMOTE2-	REMOTE2-
A3	REMOTE2+	REMOTE2+
A2	REMOTE1-	REMOTE1-
B1	REMOTE1+	REMOTE1+
B3	VCCP_IN	VCCP_IN
B2	+2.5V_IN	+2.5V_IN

a. The STRAPOPT connection defines pin functions for this package, and also the contents of the Device ID register at Plug&Play Index 0x20:
When connected to VTR, the table column STRAPOPT=1 applies, and Device ID = 0x7F.
When connected to VSS, the table column STRAPOPT=0 applies, and Device ID = 0x7D.

3.3 SCH3224 Ball Layout Summary

FIGURE 3-3: SCH3224 FOOTPRINT DIAGRAM, TOP VIEW

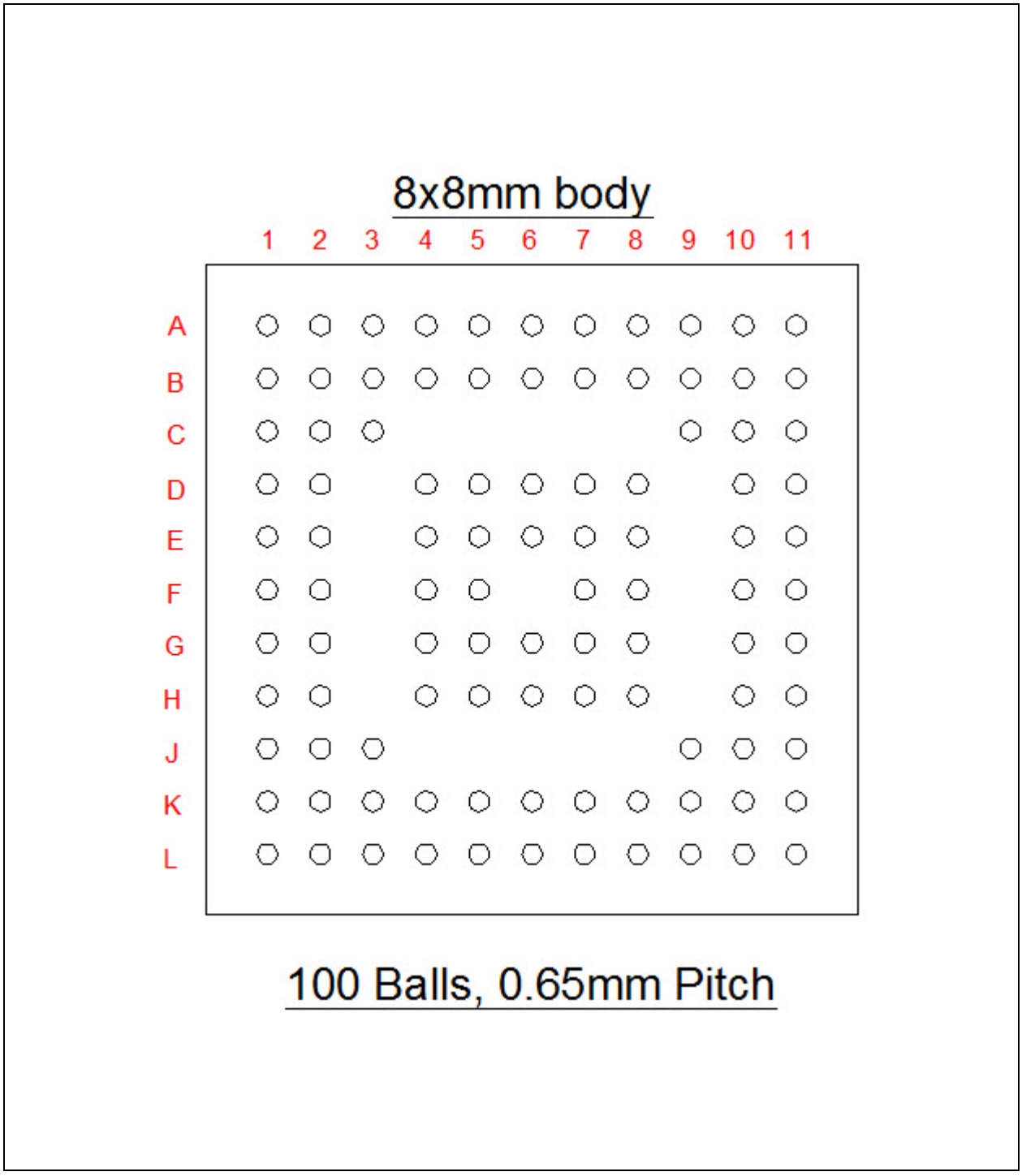


TABLE 3-3: SCH3224 SUMMARY

BALL#	FUNCTION[a]
C3	+12V_IN
C2	+5V_IN
D3	VTR
E6	TEST
D2	VSS
F2	CLOCKI
E2	LAD0
D1	LAD1
E3	LAD2
F3	LAD3
E1	LFRAME#
G3	LDRQ#
F1	PCI_RESET#
G1	PCI_CLK
G2	SER_IRQ
H1	VSS
H2	VCC
H3	GP44 / TXD6
F5	GP45 / RXD6
E5	GP46 / nSCIN6
J2	GP47 / nSCOUT6
J1	AVSS
K1	VBAT
J3	GP27 / nIO_SMI / P17
J4	KDAT / GP21
K3	KCLK / GP22
K2	MDAT / GP32
L2	MCLK / GP33
L3	GP36 / nKBDRST
J5	GP37 / A20M
K4	RESERVED=N/C (Make no connection.)
G6	VTR
K5	nINIT
G5	nSLCTIN
J6	PD0
L5	PD1
K6	PD2
L4	PD3
L6	PD4
C10	PD5
K7	PD6
J7	PD7
G7	VSS

TABLE 3-3: SCH3224 SUMMARY (CONTINUED)

BALL#	FUNCTION[a]
C7	SLCT
E7	PE
L8	BUSY
K8	nACK
J8	nERROR
G11	nALF
K9	nSTROBE
L10	nRI1
J9	nDCD1
K10	RXD1
K11	TXD1 / SIOXNOROUT
J10	nDSR1
J11	nRTS1 / SYSOPT0
H9	nCTS1
H10	nDTR1 / SYSOPT1
H11	GP50 / nRI2
L9	VTR
L7	VSS
G9	GP51 / nDCD2
G10	GP52 / RXD2(IRRX2)
F11	GP53 / TXD2(IRTX2)
F10	GP54 / nDSR2
E11	GP55 / nRTS2 / RESGEN
D11	GP56 / nCTS2
F9	GP57 / nDTR2
D10	RXD5
B11	TXD5
E9	nSCOUT5
D9	nSCIN5
C11	GP42 / nIO_PME
E10	VTR
B10	GP61 / nLED2 / CLKO
C9	GP60 / nLED1 / WDT
C1	CLKI32
B9	nRSMRST
A10	VSS
C8	PWRGD_OUT
A9	PWRGD_PS
B8	nFPRST / GP30
F7	VTR
C6	VSS
B7	nTHERMTRIP
A8	nHWM_INT
A7	PWM3

TABLE 3-3: SCH3224 SUMMARY (CONTINUED)

BALL#	FUNCTION[a]
B6	PWM2
A6	PWM1
A5	FANTACH3
B5	FANTACH2
C5	FANTACH1
B4	HVSS
C4	HVTR
A4	REMOTE2-
A3	REMOTE2+
A2	REMOTE1-
B1	REMOTE1+
B3	VCCP_IN
B2	+2.5V_IN

a. Device ID register at Plug&Play Index 0x20 holds 0x7F.

3.4 SCH3222 Ball Layout Summary

FIGURE 3-4: SCH3222 FOOTPRINT DIAGRAM, TOP VIEW

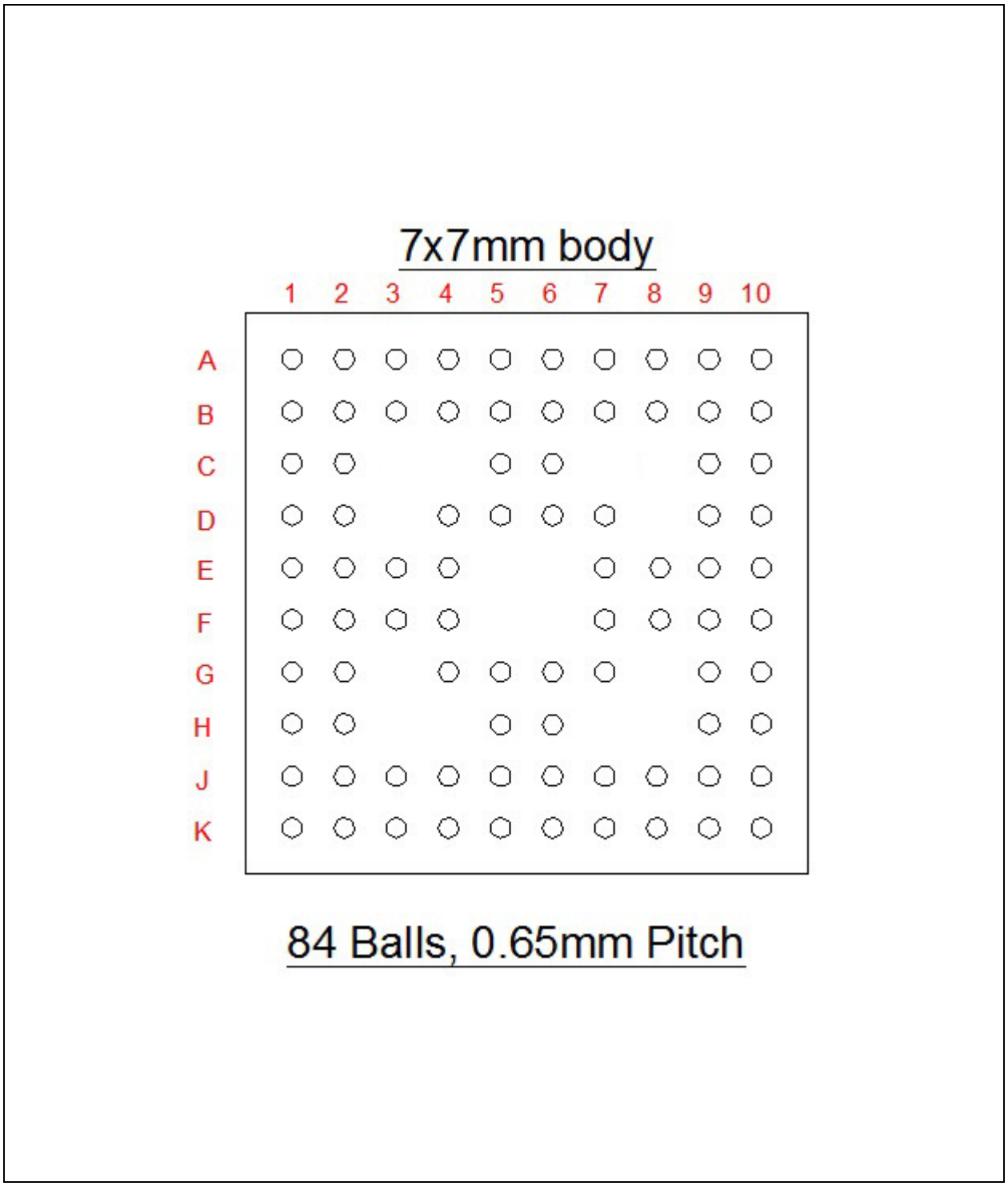


TABLE 3-4: SCH3222 SUMMARY

BALL#	FUNCTION[a]
B1	+5V_IN
A1	GP40
C1	VTR
A2	TEST
D1	VSS
E1	CLOCKI
B2	LAD0
C2	LAD1
B3	LAD2
D2	LAD3
F1	LFRAME#
F2	PCI_RESET#
F3	PCI_CLK
E3	SER_IRQ
G2	VSS
G1	VCC
H1	GP44 / TXD6
J1	GP45 / RXD6
J2	GP46 / nSCIN6
K1	GP47 / nSCOUT6
K2	AVSS
H2	VBAT
K3	GP27 / nIO_SMI / P17
J3	KDAT / GP21
J4	KCLK / GP22
F4	MDAT / GP32
E4	MCLK / GP33
J5	GP36 / nKBDRST
K4	GP37 / A20M
K6	VSS
K5	VTR
K7	VSS
K8	nRI1
H5	nDCD1
K10	RXD1
J10	TXD1 / SIOXNOROUT
K9	nDSR1
J9	nRTS1 / SYSOPT0
H10	nCTS1
H9	nDTR1 / SYSOPT1
J8	GP50 / nRI2
G9	VTR
J7	VSS
G5	GP51 / nDCD2

TABLE 3-4: SCH3222 SUMMARY (CONTINUED)

BALL#	FUNCTION[a]
G10	GP52 / RXD2(IRRX2)
F10	GP53 / TXD2(IRTX2)
G7	GP54 / nDSR2
J6	GP55 / nRTS2 / RESGEN
H6	GP56 / nCTS2
F9	GP57 / nDTR2
F8	RXD5
F7	TXD5
G6	nSCOUT5
E9	nSCIN5
E10	GP10 / RXD3
D10	GP11 / TXD3
G4	GP14 / nDSR3
E8	GP17 / nRTS3
E7	GP16 / nCTS3
D7	GP42 / nIO_PME
D4	VTR
C10	GP15 / nDTR3
D9	GP61 / nLED2 / CLKO
C9	GP60 / nLED1 / WDT
B9	GP13 / nRI3
B10	GP12 / nDCD3
A10	GP31 / nRI4
A9	GP63 / nDCD4
D6	CLKI32
B8	nRSMRST
A4	VSS
A8	GP64 / RXD4
A7	GP65 / TXD4
C6	GP66 / nDSR4
B7	GP67 / nRTS4
C5	GP62 / nCTS4
B6	GP34 / nDTR4
B5	PWRGD_OUT
B4	PWRGD_PS
A6	nFPRST / GP30
A3	VTR
D5	VSS
A5	VSS
E2	VSS

a. Device ID register at Plug&Play Index 0x20 holds 0x7F.

4.0 REVISION HISTORY

TABLE 4-1: REVISION HISTORY

Revision Level & Date	Section/Figure/Entry	Correction
DS00002108A (02-16-16)	Document Release	

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PART NO.	[X]	-	XX	-	[XX]
Device	Temperature Range		Package		Tape and Reel Option

Device:	SCH3227/SCH3226/SCH3224/SCH3222	
Temperature Range:	Blank = 0°C to +70°C (Commercial) I = -40°C to +85°C (Industrial)	
Package:	SZ = 144-pin WFBGA (SCH3227) SY = 100-pin WFBGA (SCH3226. SCH3224) SX = 84-pin WFBGA (SCH3222)	
Tape and Reel Option:	Blank = Standard packaging (tray) TR = Tape and Reel (Note 1)	

Examples:

a) SCH3227-SZ
Commercial temperature, 144-pin WFBGA, Tray

b) SCH3227I-SZ-TR
Industrial temperature, 144-pin WFBGA, Tape & Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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ISBN: 9781522402992

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