

SCH3221 Silicon Errata and Data Sheet Clarification

TABLE 1: SILICON DEV/REV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾
		A
SCH3221	5Bh	00h
Note 1: The Device ID is visible as an 8-bit number at Plug and Play Configuration Index 20h.		
2: The HW Revision Number is visible as an 8-bit number at Plug and Play Configuration Index 21h.		

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾
				A
Runtime Registers	PME	1.	GP50 Generates PME on Negative Edge Only	X
Note 1: Only those issues indicated in the last column apply to the current silicon revision.				

Silicon Errata Issues

1. Module: Runtime Registers

DESCRIPTION

Only a high-to-low signal on the GP50 pin will set the associated PME status bit and generate a PME event (if enabled). This operates the same way regardless of how the polarity bit is set (i.e., non-inverted or inverted).

END USER IMPLICATIONS

Cannot use GP50 to generate a PME event on a transition from low-to-high.

Work Around

None.

SCH3221

Data Sheet Clarifications

The following typographic corrections and clarifications apply only to the SCH3221 Data Sheet, which is currently Document #00002120A. Other members of the SCH322x family have separate data sheets, and separate errata sheets.

Note: Where appropriate, corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

TABLE 3: DATA SHEET CLARIFICATION SUMMARY

Module	Item Number	Issue Summary
Runtime Registers	1.	GP30 Has Two PME Status Bits
Timing Diagrams	2.	Minimum LPC Clock Frequency

1. Module: Runtime Registers

GP30 has two sets of PME status and enable bits associated with it.

1. Bit[0] of the PME_STS3 register at offset 04h is only set on a low-to-high transition of the GP30 pin. If the corresponding enable bit, located in the PME_EN3 register at offset 07h, is set then the IO_PME# signal will be asserted.
2. Bit[0] of the PME_STS4 register at offset 1Ah is only set on a high-to-low transition of the GP30 pin. If the corresponding enable bit, located in the PME_EN4 register at offset 1Bh, is set then the IO_PME# signal will be asserted.

2. Module: Timing Diagrams

The maximum period for the PCI Clock is 55.5nS. This permits an LPC clock of 18MHz.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level and Date	Description
DS80000695A (04-11-16)	Initial Draft Version

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