Data Sheet



SCC1300-D04
Combined Gyroscope and 3-axis Accelerometer with digital SPI interfaces

Features

- ±300 º/s angular rate measurement range
- ±6 g 3-axis acceleration measurement range
- Angular rate measurement around X axis
- Angular rate sensor exceptionally insensitive to mechanical vibrations and shocks
- Superior bias stability for MEMS gyroscopes
- Digital SPI interfacing
- Enhanced self diagnostics features
- Small size: 8.5 x 18.7 x 4.5 mm (w x l x h)
- RoHS compliant robust packaging suitable for lead-free soldering process and SMD mounting
- Proven capacitive 3D-MEMS technology
- Temperature range -40 °C...+125 °C

Applications

The SCC1300-D04 is targeted at applications demanding high stability with tough environmental requirements. Typical applications include:

- Inertial Measurement Units (IMUs) for highly demanding environments
- Platform stabilization and control
- Motion analysis and control
- Roll over detection
- Robotic control systems
- Guidance systems
- Navigation systems

Overview

The SCC1300-D04 is a combined high performance gyroscope and accelerometer component. The sensor is based on Murata's proven capacitive 3D-MEMS technology. The component integrates angular rate and acceleration sensing together with flexible separate digital SPI interfaces. The small robust packaging guarantees reliable operation over the product's lifetime. The housing is suitable for SMD mounting. The component is compatible with RoHS and ELV directives.

The SCC1300-D04 is designed, manufactured and tested for high stability, reliability and quality requirements. The angular rate and acceleration sensors provide highly stable output over wide ranges of temperature and mechanical noise. The angular rate sensor bias stability is in the elite of MEMS gyros. It is also exceptionally insensitive to all mechanical vibrations and shocks. The component has several advanced self diagnostics features.

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1 Introduction

This document contains essential technical information about the SCC1300 sensor, including specifications, SPI interface descriptions, user accessible register details, electrical properties and application information. This document should be used as a reference when designing in SCC1300 component.

2 Specifications

2.1 Performance Specifications for Gyroscope

Table 1. Gyroscope performance specifications (Avdd = 5 V, Dvdd = 3.3 V and ambient temperature unless otherwise specified).

Parameter	Condition	Min [A]	Typ	Max [A]	Unit
Analog supply voltage		4.75	5	5.25	V
Analog supply current	Temperature range -40 ... +125 °C	24	26	29.5	mA
Digital supply voltage		3.0	3.3	3.6	V
Digital supply current	Temperature range -40 ... +125 °C	16	20	24	mA
Operating range	Measurement axis X	-300		300	°/s
Offset error [B]		-1.5		1.5	°/s
Offset over temperature	Temperature range -40 ... +125 °C	-0.9		0.9	°/s
	Temperature range -10 … +60 °C	-0.5		0.5	°/s
Offset drift velocity	Temperature gradient ≤ 2.5 K/min	-0.6		0.6	(°/s)/min
Offset short term instability [C]			<2.1		°/h
Angular random walk (ARW) [C]			0.86		°/√h
Sensitivity			18		LSB/(°/s)
Sensitivity over temperature	Temperature range -40 ... +125 °C	-1		1	%
Total sensitivity error [B]		-2		2	%
Nonlinearity	Temperature range -40 ... +125 °C	-1		1	°/s
Noise (RMS)			0.14	0.23	°/s
Noise Density			0.02		(°/s)/√Hz
Cross-axis sensitivity				1.7	%
G-sensitivity		-0.1		0.1	(°/s)/g
Shock sensitivity	50g, 6ms			2.0	°/s
Shock recovery time				50.0	ms
Amplitude response	-3dB frequency		50		Hz
Power on setup time				0.8	s
Output data rate			2		kHz
Output load				200	pF
SPI clock rate		0.1		8	MHz

A) MIN/MAX values are ±3 sigma variation limits from validation test population.
B) Including calibration error and drift over lifetime.
C) Based on Allan variance measurements (Figure 1b).
D) Cross-axis sensitivity is the maximum sensitivity in the plane perpendicular to the measuring direction relative to the sensitivity in the measuring direction. The specified limit must not be exceeded by either axis.

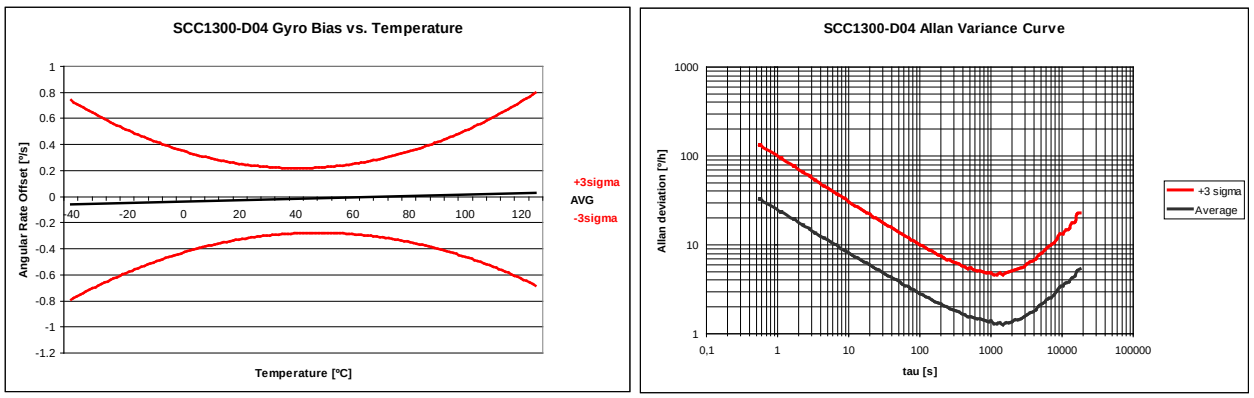

Figure 1 a) SCC1300-D04 Gyroscope offset over full temperature range, b) Allan variance curve

2.2 Performance Specifications for Accelerometer

Table 2. Accelerometer performance specifications (Vdd = 3.3V and ambient temperature unless otherwise specified).

Parameter	Condition	Min [A]	Typ	Max [A]	Unit
Analog and digital supply voltage		3.0	3.3	3.6	V
Current consumption	Active mode		3	5	mA
	Power down mode		0.12		mA
Measurement range	Measurement axes X, Y & Z	-6		6	g
Offset error [B]	@25 °C ±5°C	-70		70	mg
Offset temperature drift [C]	Temperature range -40 ... +125 °C	-40		40	mg
Sensitivity	13 bit output		650		LSB/g
Total sensitivity error	Temperature range -40 ... +125 °C	-4		4	% FS
Sensitivity calibration error	@25 °C ±5°C	-1		1	% FS
Sensitivity temperature drift	Temperature range -40 ... +125 °C	-1		1	% FS
Linearity error	+1g ... -1g range	-40		40	mg
Cross-Axis sensitivity [D]		-2.5		2.5	%
Zero acceleration output	2-complement format		0		LSB
Amplitude response [E]	-3dB frequency	30		55	Hz
Noise			5	7	mg RMS
Power on setup time				0.1	s
Output data rate			2000		Hz
Output load				50	pF
SPI clock rate				8	MHz

A) MIN/MAX values are ±3 sigma variation limits from validation test population.

B) Includes offset deviation from 0g value, including calibration error and drift over lifetime.

C) Biggest change of output from RT value due to temperature.

D) Cross-axis sensitivity is the maximum sensitivity in the plane perpendicular to the measuring direction relative to the sensitivity in the measuring direction. It is calculated as the geometric sum of the sensitivities in two perpendicular directions (Sx and Sy) in this plane.

E) See Figure 2.

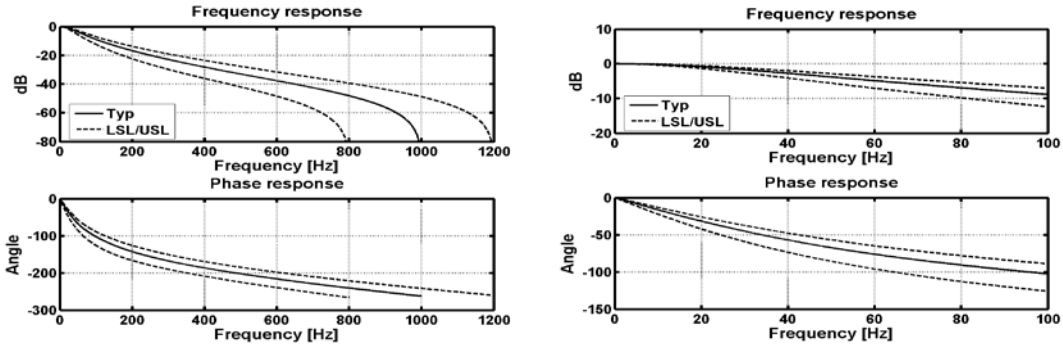

Figure 2. SCC1300-D04 Accelerometer frequency response curves

2.3 Absolute Maximum Ratings

Table 3. Absolute maximum ratings of the SCC1300 sensor.

Parameter	Condition	Min	Typ	Max	Unit
Gyroscope supply voltages					
Analog supply voltage, AVDD_G		-0.5		7	V
Digital supply voltage, DVDD_G		-0.3		3.6	V
Maximum voltage at analog input/output pins		-0.3		AVDD_G + 0.3V	
Maximum voltage at digital input/output pins		-0.3		DVDD_G + 0.3	V
Accelerometer supply voltages					
Digital supply voltage, DVDD_A		-0.3		3.6	V
Analog supply voltage, AVDD_A		-0.5		7.0	V
Maximum voltage at input / output pins		-0.3		DVDD_A + 0.3V	V
General Component Ratings					
Operating temperature		-40		125	°C
Storage temperature		-40		125	°C
	Max 96h	-40		150	°C
Maximum junction temperature during lifetime. Note: device has to be functional, but not in full spec.				155	°C
Mechanical Shock			3000		g
ESD	HBM			2	kV
	CDM			500	V
Ultrasonic agitation (cleaning, welding, etc)	Prohibited				

2.4 Pin Description

The pinout for the SCC1300 is presented below in Figure 3. (See Table 4 for pin description)

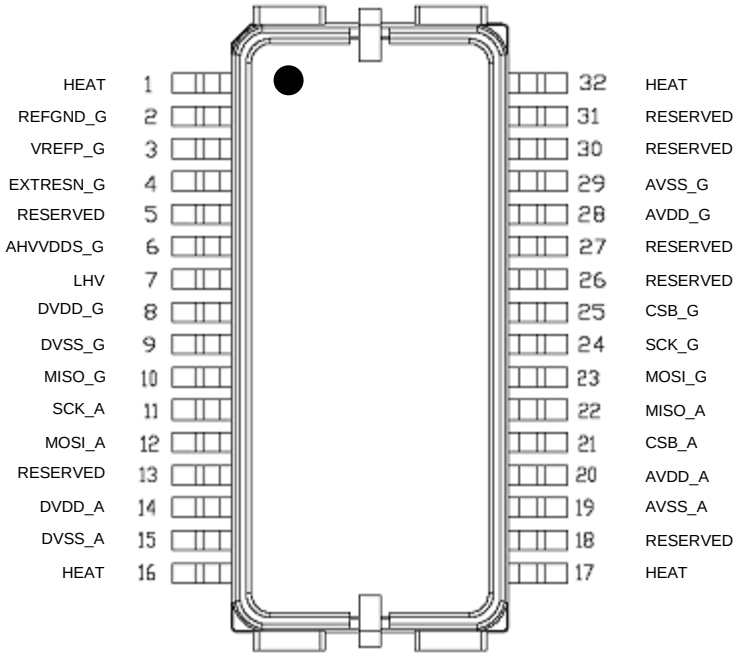

Figure 3. SCC1300 pinout diagram.

Table 4. SCC1300 pin description

pin #	Name	Type 1)	PD/PU/HV 2)	Description
1	HEAT	AI		Heatsink connection, connect to AVSS_G.
2	REFGND_G	AI		Analog reference ground, connect to AVSS_G
3	VREFP_G	AO		Connection for External C for positive reference voltage.
4	EXTRESN_G	DI	PU	External Reset, 3.3V Schmitt-trigger input with internal pull-up, High-low transition causes system restart
5	RESERVED	R		Factory use only, leave floating
6	AHVVDDS_G	AO	HV (~30V)	Connection for External C for high voltage analog supply. High voltage pad ~30V
7	LHV	AI	HV (~30V)	Connection for inductor for high voltage generation, high voltage pad ~30V
8	DVDD_G	AI		Digital Supply Voltage
9	DVSS_G	AI		Digital Supply Return
10	MISO_G	DOZ		Data Out of SPI Interface, 3.3V level.
11	SCK_A	DI	PD	Clk Signal of SPI Interface, 3.3V Schmitt-trigger input
12	MOSI_A	DI	PD	Data In of SPI Interface, 3.3V Schmitt-trigger input
13	RESERVED	R		Factory use only, leave floating
14	DVDD_A	AI		Digital Supply Voltage
15	DVSS_A	AI		Digital Supply Return
16	HEAT	AI		Heatsink connection, connect to AVSS_G.
17	HEAT	AI		Heatsink connection, connect to AVSS_G.
18	RESERVED	R		Factory use only, leave floating
19	AVSS_A	AI		Analog Supply Return
20	AVDD_A	AI		Analog Supply Voltage
21	CSB_A	DI	PU	Chip Select of SPI Interface, 3.3V Schmitt-trigger input
22	MISO_A	DOZ		Data Out of SPI Interface, 3.3V level
23	MOSI_G	DI	PD	Data In of SPI Interface, 3.3V Schmitt-trigger input
24	SCK_G	DI	PD	Clk Signal of SPI Interface, 3.3V Schmitt-trigger input
25	CSB_G	DI	PU	Chip Select of SPI Interface, 3.3V Schmitt-trigger input
26	RESERVED	R		Factory use only, leave floating
27	RESERVED	R		Factory use only, leave floating
28	AVDD_G	AI		Analog Supply Voltage
29	AVSS_G	AI		Analog Supply Return
30	RESERVED	R		Factory use only, leave floating
31	RESERVED	R		Factory use only, leave floating
32	HEAT	AI		Heat sink connection, connect to AVSS_G.

Notes:
1) A = Analog, D = Digital, I = Input, O = Output, Z = Tristate Output, R = Reserved
2) PU = internal pull up, PD = internal pull down, HV = high voltage

2.5 Digital I/O Specification

Table 5 (gyroscope interface) and Table 6 (accelerometer interface) below describe the DC characteristics of the SCC1300 sensor's digital I/O pins. The digital supply voltage is 3.3V unless otherwise specified. Current flowing into the circuit has a positive value.

Table 5. SCC1300 gyroscope SPI interface DC characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Input terminal CSB_G						
Pull up current	V_{IN} = 0V	I_{PU}	10		50	µA
Input high voltage	DVDD_G = 3.3V	V_{IH}	2		DVDD_G	V
Input low voltage	DVDD_G = 3.3V	V_{IL}			0.8	V
Hysteresis	DVDD_G = 3.3V	V_{HYST}	0.3			V
Input terminal SCK_G						
Input high voltage	DVDD_G = 3.3V	V_{IH}	2		DVDD_G	V
Input low voltage	DVDD_G = 3.3V	V_{IL}			0.8	V
Hysteresis	DVDD_G = 3.3V	V_{HYST}	0.3			V
Input leakage current	0 < V_{MISO} < 3.3V	I_{LEAK}	-1		1	uA
Output terminal MOSI_G						
Input high voltage	DVDD_G = 3.3V	V_{IH}	2		DVDD_G	V
Input low voltage	DVDD_G = 3.3V	V_{IL}			0.8	V
Hysteresis	DVDD_G = 3.3V	V_{HYST}	0.3			V
Pull down current	V_{IN} = V_{DVDD_G}	I_{LEAK}	10		50	uA
Output terminal MISO_G (Tri-state)						
Output high voltage	I_{OUT} = -1mA	V_{OH}	DVDD_G -0.5V			V
	I_{OUT} = -50µA		DVDD_G -0.2V			V
Output low voltage	0 ≤ V_{MISO} ≤ 3.3V	V_{OL}			0.5	V
Capacitive load					200	pF

Table 6. SCC1300 accelerometer SPI interface DC characteristics

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Input terminal CSB_A						
Pull up current	V_{IN} = V	I_{PU}	10		50	µA
Input high voltage	DVDD_A = 3.3V	V_{IH}	2		DVDD_A	V
Input low voltage	DVDD_A = 3.3V	V_{IL}			0.8	V
Hysteresis	DVDD_A = 3.3V	V_{HYST}	0.18			V
Input terminal MOSI_A, SCK_A						
Pull down current	V_{IN} = 3.3V	I_{PD}	10		50	µA
Input high voltage	DVDD_A = 3.3V	V_{IH}	2		DVDD_A	V
Input low voltage	DVDD_A = 3.3V	V_L			0.8	V
Hysteresis	DVDD_A = 3.3V	V_{HYST}	0.18			V
Output terminal MISO_A						
Output high voltage	I > -1mA DVDD_A = 3.3V	V_{OH}	DVDD_A - 0.5V			V
Output low voltage	I < 1 mA	V_{OL}			0.5	V
Capacitive load					50	pF
Tri-state leakage	0 < V_{MISO} < 3.3V	I_{LEAK}	-3		3	uA

2.6 SPI AC Characteristics

The AC characteristics of the SCC1300 are defined in Figure 4 and Table 7.

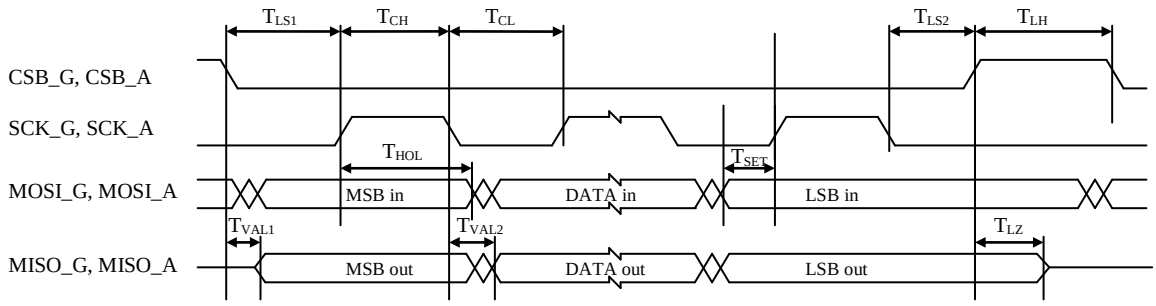

Figure 4. Timing diagram of SPI communication

Table 7. Timing characteristics of SPI communication

Parameter	Condition	Min	Typ	Max	Unit
F_{SPI}		0.1		8	MHz
T_{SPI}			1/ F_{SPI}		
T_{CH}	SCK_G, SCK_A high time	45	T_{SPI} /2		ns
T_{CL}	SCK_G, SCK_A low time	45	T_{SPI} /2		ns
T_{LS1}	CSB_G, CSB_A setup time	45	T_{SPI} /2		ns
T_{VAL1}	Delay CSB_G -> MISO_G Delay CSB_A -> MISO_A			30	ns
T_{SET}	MOSI_G, MOSI_A setup time	30			ns
T_{HOL}	MOSI_G, MOSI_A data hold time	30			ns
T_{VAL2}	Delay SCK_G -> MISO_G Delay SCK_A -> MISO_A			40	ns
T_{LS2}	CSB_G, CSB_A hold time	45	T_{SPI} /2		ns
T_{LZ}	Tri-state delay time			30	ns
T_{RISE}	Rise time of the SCK_G, SCK_A		10		ns
T_{FALL}	Fall time of the SCK_G, SCK_A		10		ns
T_{LH}	Time between SPI cycles	125			ns

2.7 Measurement Axis and Directions

The positive/negative acceleration and angular rate measurement directions of the SCC1300 are shown below in Figure 5.

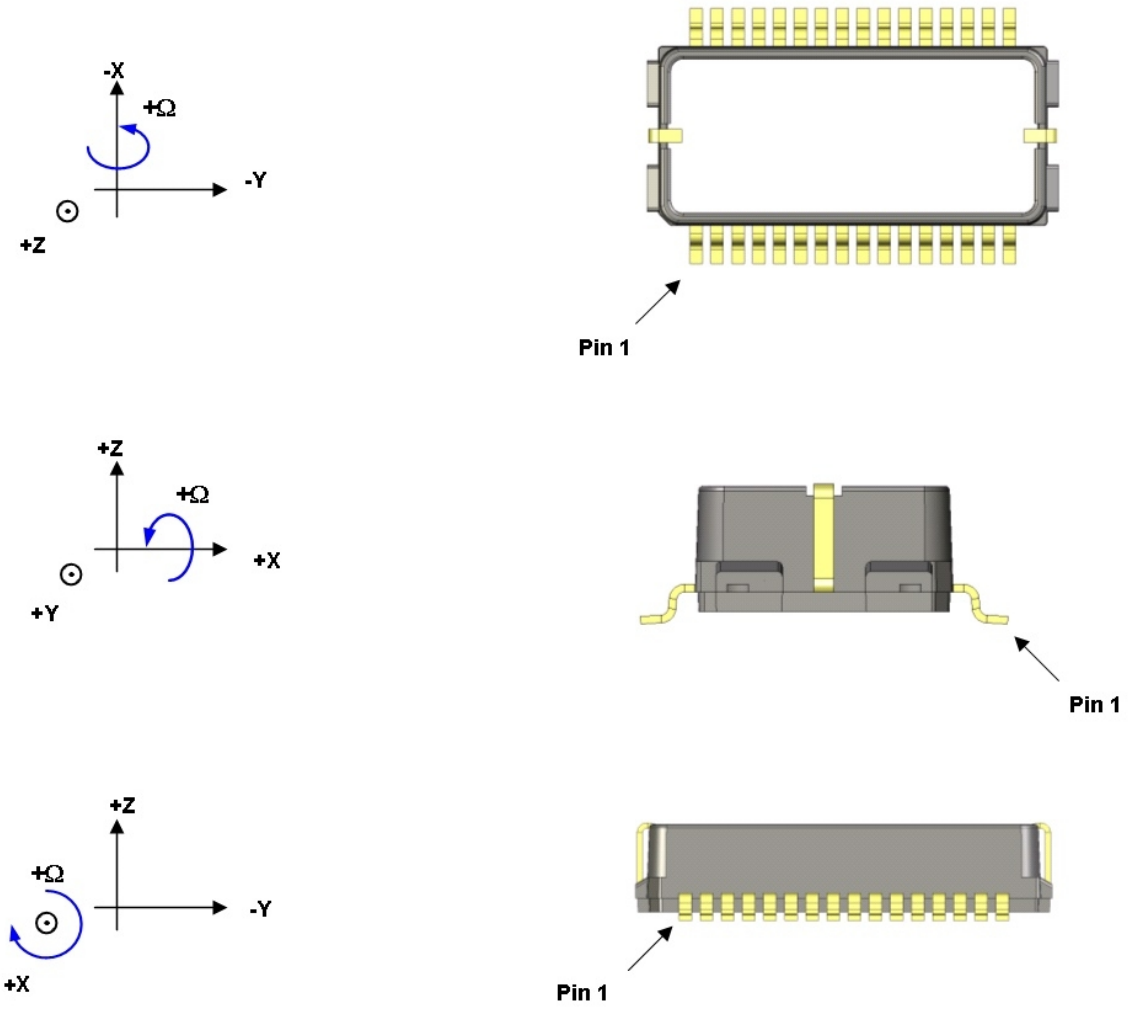

Figure 5. Acceleration and angular rate measurement directions of the SCC1300

2.8 Package Characteristics

2.8.1 Package Outline Drawing

The package outline and dimensions of the SCC1300 are presented in Figure 6 and Table 8.

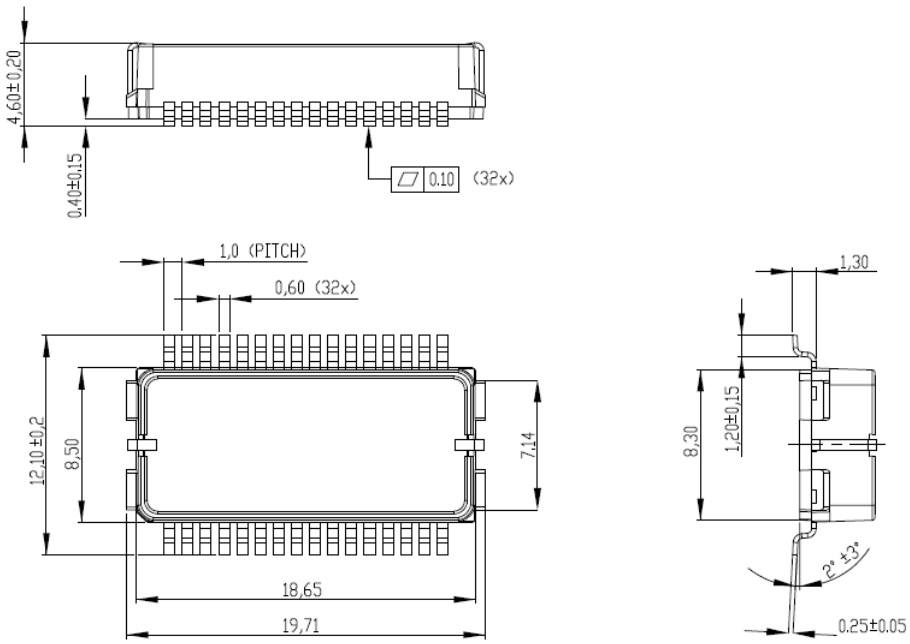

Figure 6. Package outline and dimensions of the SCC1300. All tolerances are according to ISO2768-f (see table below) unless otherwise specified.

Limits for linear measures (ISO2768-f)

Tolerance class	Limits in mm for nominal size in mm			
	0.5 to 3	Above 3 to 6	Above 6 to 30	Above 30 to 120
f (fine)	±0.05	±0.05	±0.1	±0.15

Table 8. Package dimensions of the SCC1300

Component	Parameter	Min	Typ	Max	Unit
Length	Without leads		19.71		mm
Width	Without leads		8.5		mm
Width	With leads		12.1		mm
Height	With leads (including stand-off and EMC lead)		4.60		mm
Lead pitch			1.0		mm

2.8.2 PCB Footprint

The footprint dimensions of the SCC1300 are presented in Figure 7 and Table 9.

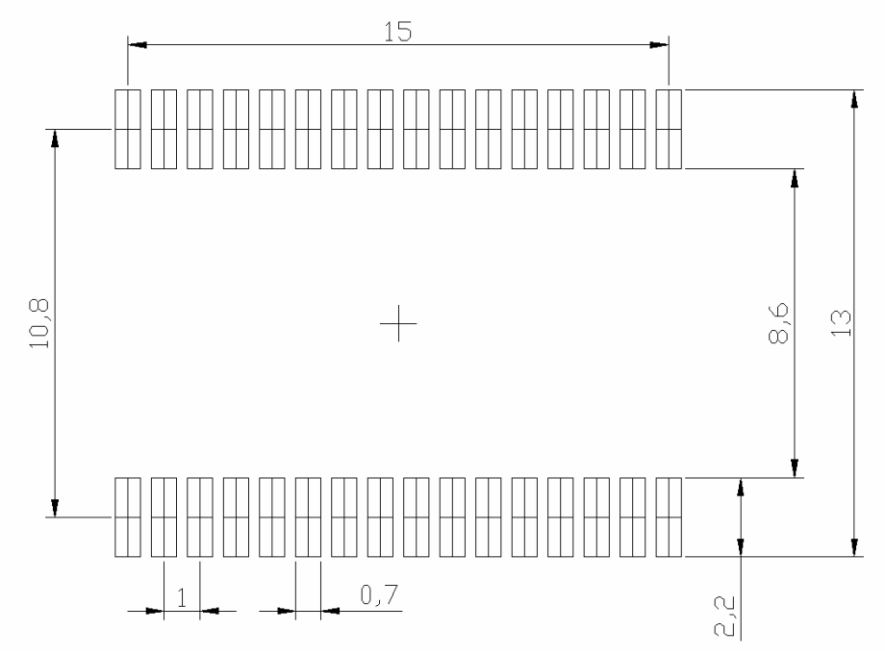

Figure 7. Footprint of the SCC1300

Table 9. Footprint dimensions of the SCC1300

Component	Parameter	Min	Typ	Max	Unit
Footprint length	Without lead footprints		15.7		mm
Footprint width	Without lead footprints		13.0		mm
Footprint lead pitch	Long side leads		1.0		mm
Footprint lead length			2.20		mm
Footprint lead width	Long side leads		0.7		mm

2.9 Abbreviations

ASIC	Application Specific Integrated Circuit
SPI	Serial Peripheral Interface
RT	Room Temperature
STC	Self Test Continuous (continuous self testing of accelerometer element)
STS	Self Test Static (gravitation based self test of accelerometer element)
ARW	Angular random walk
DPS	Degrees per second

3 General Product Description

The SCC1300 sensor consists of independent acceleration and angular rate sensing elements and separate independent Application Specific Integrated Circuits (ASICs) used to sense and control those elements. Figure 8 represents an upper level block diagram of the component. Both ASICs have their own independent digital SPI interfaces used to control and read the accelerometer and the gyroscope.

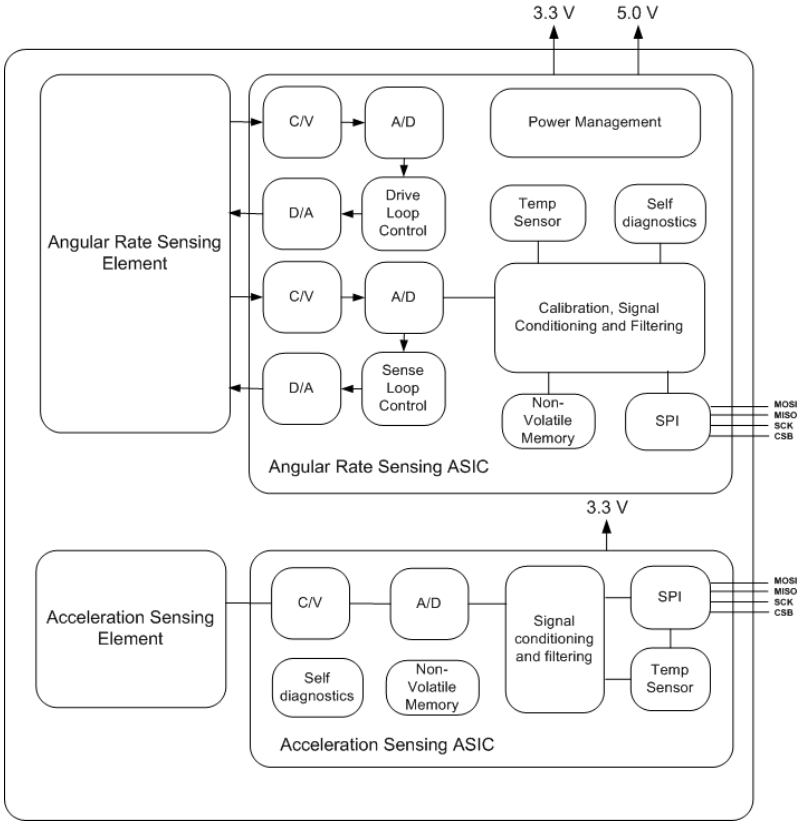

Figure 8. Block diagram of the SCC1300

The angular rate and acceleration sensing elements are manufactured using Murata's proprietary High Aspect Ratio (HAR) 3D-MEMS process, which enables robust, extremely stable and low noise capacitive sensors.

The acceleration sensing element consists of four acceleration-sensitive masses. Acceleration causes a capacitance change that is converted into a voltage change in the signal conditioning ASIC.

The angular rate sensing element consists of moving masses that are purposely exited to in-plane drive motion. Rotation in the sensitive direction causes out-of-plane movement that can be measured as capacitance change with the signal conditioning ASIC.

3.1 Factory Calibration

SCC1300 sensors are factory calibrated. No separate calibration is required in the application. Parameters that are trimmed during production include sensitivities, offsets and frequency responses. Calibration parameters are stored to non-volatile memory during manufacturing. The parameters are read automatically from the internal non-volatile memory during start-up.

It should be noted that assembly can cause minor offset/bias errors to the sensor output. If the best possible offset/bias accuracy is required, system level offset/bias calibration (zeroing) after assembly is recommended.

4 Reset and Power Up

After start-up the angular rate and acceleration data is immediately available through SPI registers. There is no need to initialize the gyroscope or accelerometer before starting to use it. If the application requires operation correctness to be monitored, several self diagnostic features are available. For more details about enabling the self diagnostic features, refer to the gyro and accelerometer power-up sequences (Sections 4.1 and 4.2).

4.1 Gyro Power-up Sequence

After power-up read the Status register (0x08) twice to clear self diagnostic error flags (see Table 12 for more details about gyro self diagnostics). Angular rate data is available immediately after start-up without any additional configuration commands.

Table 10. Gyroscope power-up sequence of the SCC1300

Procedure	Function
Set V_{DVDD_G} V=3.0...3.6V	
Set V_{AVDD_G} V=4.75...5.25V	
Wait 800 ms	
Read Status register (08h) two times	Acknowledge error flags after start up

4.1.1 Gyro Reset

The SCC1300 Gyroscope can be reset by writing 0x04 to the IC Identification register (address 07h) or by using the external active low reset pin (EXTRESN_G). Power supplies should be within the specified range before the reset pin can be released. Please follow the gyro power-up sequence after reset (Table 10).

4.2 Accelerometer Power-up Sequence

No initial configuration is needed before starting to measure acceleration. However, if the device's self diagnostic features are being used, the following operations need to be performed after powering-up the device (see section 5.4.5 for more details about the accelerometer's self diagnostics).

Table 11. Accelerometer power-up sequence of the SCC1300

Procedure	Function	Check
Set Vdd = 3.0...3.6 V	Release part from reset	
Wait 35 ms	Memory reading and self-diagnostic. Settling of signal path	
Read INT_STATUS	Acknowledge for possible saturation (SAT-bit) Check that memory checksum passed	SPI frame fixed bits SPI ST = 0
Write CTRL = 00000000 or CTRL = 00001000 or CTRL = 00001010	Set PORST = 0 Set PORST = 0, Start STC Set PORST = 0, Start STC, Start STS	SPI frame fixed bits SPI FRME = 0 SPI ST = 0 SPI SAT = 0
Wait 10 ms	STS calculation	
Read CTRL	Check that STC is on, if enabled Check that STS is over, if enabled	CTRL.ST = 1 CTRL.ST_CFG = 0 SPI frame fixed bits SPI FRME = 0 SPI PORST = 0 SPI ST = 0 SPI SAT = 0 dPAR, data parity
Read Z_MSB, Z_LSB, Y_MSB, Y_LSB, X_MSB, X_LSB	Read acceleration data	SPI frame fixed bits SPI FRME = 0 SPI PORST = 0 SPI ST = 0 SPI SAT = 0 dPAR, data parity

4.2.1 Accelerometer reset

The accelerometer can be reset by writing 0Ch, 05h, 0Fh (in this order) into the RESET register (address 03h). If the accelerometer's self diagnostic features are being used, the power-up sequence should be executed after reset (Table 11).

5 Component Interfacing

5.1 SPI Interfaces

The SCC1300 sensor has individual SPI interfaces for the accelerometer and angular rate sensor, and they need to be addressed separately. Both interfaces have their own 4-wire interconnection pins in the component package. SPI communication transfers data between the SPI master and registers of the SCC1300's ASICs. The SCC1300's ASICs always operate as slave devices in master-slave operation mode. 3-wire SPI connection cannot be used.

SCC1300 angular rate sensor's ASIC SPI interface:

MOSI_G	master out slave in	µP → ASIC
MISO_G	master in slave out	ASIC → µP
SCK_G	serial clock	µP → ASIC
CSB_G	chip select (active low)	µP → ASIC

SCC1300 accelerometer's ASIC SPI interface:

MOSI_A	master out slave in	µP → ASIC
MISO_A	master in slave out	ASIC → µP
SCK_A	serial clock	µP → ASIC
CSB_A	chip select (active low)	µP → ASIC

PLEASE NOTE THAT EXACTLY THE SAME SPI ROUTINES DO NOT WORK FOR BOTH ASICS! For example, the SCC1300 accelerometer ASIC uses 8-bit addressing, while the SCC1300 angular rate sensor ASIC uses 16-bit addressing.

Both SPI interfaces and instructions for using them are explained separately in the following chapters. For more details, please refer to "Technical Note 92: SPI Communication with SCC1300".

5.2 Gyroscope Interface

This chapter describes the SCC1300 angular rate sensor ASIC interface and how to use it. The angular rate sensor ASIC SPI interface uses 16-bit addressing.

5.2.1 Gyro SPI Communication Overview

The SPI communication is based on 16-bit words. The SPI frames consist of a multiple of these 16-bit words. Figure 9 shows an example of a single SPI data transmission. The gyro captures data on the SCK's rising edge (MOSI line) and data is propagated on the SCK's falling edge (MISO line). This is equal to SPI Mode 0 (CPOL = 0 and CPHA = 0). The SPI transmission is always started with the CSB falling edge and terminated with the CSB rising edge.

The basic read/write data frame consists of two 16-bit words. The first word contains a register address, while the second word contains the register content to be written or read (see timing diagram in Figure 9).

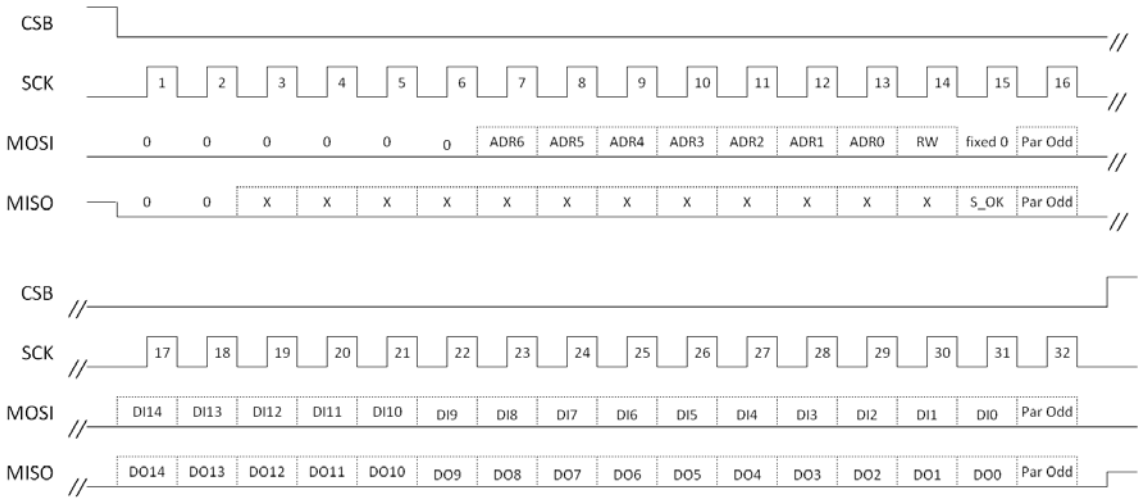

Figure 9. SPI communication timing diagram

After the CSB falling edge the device interprets the first 16-bit word as a 7-bit register address and a read/write operation bit. Remaining bits shall be set to zero. Bit [0] of the 16-bit word is used as an odd parity bit. The 16-bit address word is shown below in detail:

MOSI Address Word:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0	RW	Fixed 0	Par odd

ADR[6:0] : Register address
RW : RW = 1 : Write access
RW = 0 : Read access
Par odd : Odd parity bit.
Par odd = 0 : the number of ones in the address word (D15:D1) is odd.
Par odd = 1 : the number of ones in the address word (D15:D1) is even.

The ADR bits are used to select an internal register of the device; the RW bit selects the access mode for the selected register. The par odd bit has to be calculated and inserted by the master in order to complete the transmission.

5.2.2 Gyro SPI Read Frame

When the address word bit RW is '0', the master performs a read access on the register selected by the register address bits (ADR). After transmission of the address word, the master has to send an additional word (zero vector) to clock the data out from the MOSI. Data is transferred out from the MOSI MSB first.

Example of how to read the rate output

MCU begins the communication by sending the address word (Rate_X register address is 00h, RW='0' and Par odd='1') followed by the zero vector (with correct parity; in this case 'Par odd' bit value will be 1). The zero vector is necessary for the sensor to be able to reply to the MCU during the last 16-bit frame. The sensor replies by sending first the status bits followed by the rate data.

MOSI: 0x0001 0x0001
MISO: 0x3FFE 0xXXXX

The complete read frame transmission length is 32 bits (see Figure 10 below).

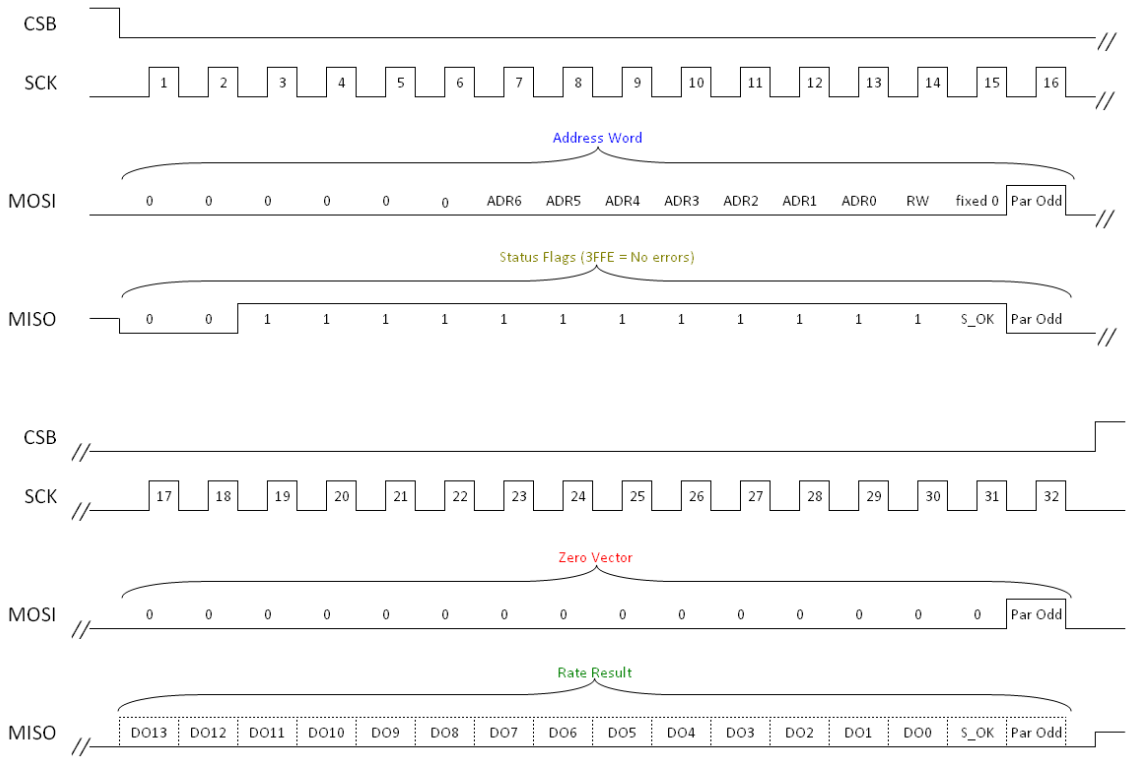

Figure 10. Complete gyroscope read frame

Encoding of the MISO status flags are shown below.

Status flags (1st 16-bit word on the MISO line) in case status flags are cleared after gyro start-up (see Section 4.1):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	1	1	1	1	1	1	1	1	1	s_ok	Par odd

S_OK is generated out of the monitoring flags in the status register (08h).

Data word (2nd 16-bit word on the MISO line):

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DO13	DO12	DO11	DO10	DO9	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0	s_ok	Par odd

DO[13:0] : Value of the angular rate register (14 bits)
S_OK: Sensor OK flag
Par odd : Odd parity bit.
Par odd = 0 : the number of ones in the data word (D15:D1) is odd.
Par odd = 1 : the number of ones in the data word (D15:D1) is even.

See section 5.3.1 for details on angular rate data conversion

5.2.3 Gyro SPI Write Frame

When the address word bit RW is ‘1', the master performs a write access on the register selected by the register address (ADR). The SCC1300 writes the next word transmitted by the master (data word) in the selected register and sends the data that has been previously stored in this register out from the MISO.

If the device is addressed with a non-existent register address, the response from the MISO will be ´0x0000´.

The following table shows data encoding for write access:

Data word:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DI14	DI13	DI12	DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0	Par odd

DI[14:0] : Data value for write access (15 Bits)
Par odd : Odd parity bit
Par odd = 0 : the number of ones in the data word (D15:D1) is odd.
Par odd = 1 : the number of ones in the data word (D15:D1) is even.

An example of a complete write frame transmission is given in Figure 11 (gyroscope soft reset):

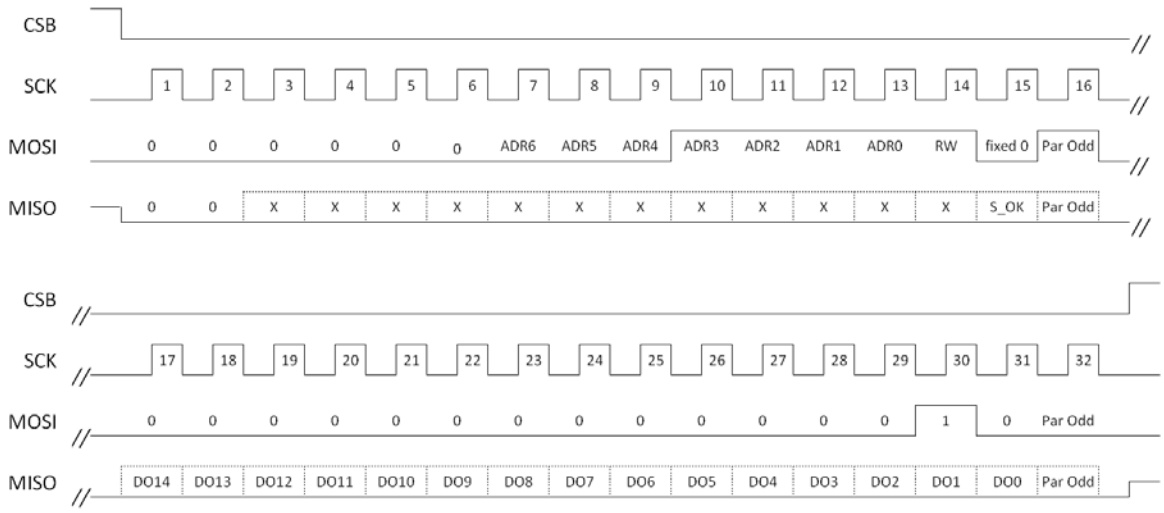

Figure 11. Gyroscope soft reset frame

5.2.4 Gyro SPI Mixed Access Mode

It is possible to mix the write and read access modes during one communication frame. Mixed access mode can be used, for example, to make an interleaved read of both angular rate and temperature data within the same SPI frame.

Figure 12 shows an example of an interleaved read access:

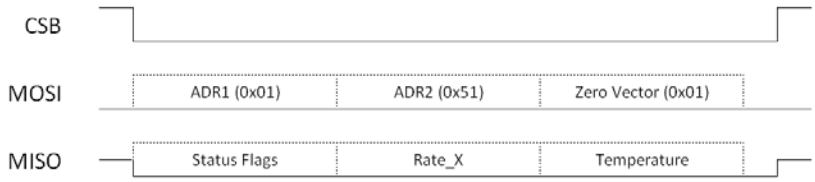

Figure 12. SPI read interleaving

Each communication word in Figure 12 contains 16 SCK cycles.

After the communication start condition (CSB falling edge), the master sends the address word ADR1 with the address of the Rate_X register (0x00), R/W = '0' (read access) and odd parity. All combined, ADR1 = 0x01. In parallel the SCC1300 sends out the status flags.

During transmission of the next address word ADR2, the SCC1300 sends out the register value specified in ADR1 (Rate_X). On ADR2 the master performs another read access, now to the TEMP register (0x0A). The address word ADR2 will be 0x51 (TEMP register address 0x0A shifted to left by 3 bits and added odd parity bit; see Figure 9 for more details). To receive the register value of the second read access (Temperature), the master has to send an additional word to the MOSI (Zero Vector with Odd Parity).

5.3 Gyroscope ASIC Addressing Space

The gyroscope ASIC has multiple register and EEPROM blocks. The EEPROM blocks used for holding calibration data are programmed via SPI during the manufacturing process. The user only needs to access the data register block at addresses 00h, 07h, 08h and 0Ah. The content of this register block is described below.

Table 12. Gyroscope register address space

Address hex	Register Name	Bits	Read/ Write	Description
00h	Rate_X	15:2	R	Rate sensor output in two's complement format
		1	R	S_OK Flag 1 – Rate_X and Temp valid 0 – Rate_X and/or Temp invalid S_OK is generated from internal monitoring flags shown in the status register (08h). If any of the flags in register 08h [15:2] is 0, S_OK will be 0 Only if all flags in register 08h [15:2] are 1, S_OK will be 1
		0	R	Odd Parity bit
07h	IC Identification	15:3	R/W	Reserved, write all to 0
		2	R/W	Soft Reset Setting this bit to 1 to resets the logic core, see section 4.1.1 for more details.
		1	R/W	Reserved, write to 0
		0	R/W	Odd Parity bit
08h	Status/Config	15:10	R	Reserved
		9	R	Parity_OK This bit is set as soon as the SPI logic detects a wrong parity bit received from the µC. The bit is automatically cleared during read access to this register. 1 – Parity check ok 0 – Parity error
		8:1	R	Reserved
		0	R	Odd Parity bit
0Ah	Temp	15:2	R	Temperature sensor output in two's complement format
		1	R	S_OK Flag 1 – Rate_X and Temp valid 0 – Rate_X and/or Temp invalid
		0	R	Odd Parity bit

5.3.1 Angular Rate Output Register

Angular rate data is presented in 14-bit, 2's complement format. Bits [1:0] do not contain angular rate data and they must be discarded. Rate_X bit weights are shown in Table 13 below:

Table 13. Gyroscope rate output bit weights [dps] (sensitivity 18 LSB/dps).

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
s	227.56	113.78	56.89	28.44	14.22	7.111	3.556	1.777	0.888	0.444	0.222	0.111	0.056	s_ok	Par odd

s = sign bit

5.3.1.1 Example of Rate Data Conversion

According to the Gyroscope Register Map (Table 12) the bits 1:0 do not contain rate data and they must be discarded when converting rate register data to angular speed.

For example: the Rate_X register (Address 0x00) data is 0xFF95. The bits 1:0 need to be discarded and as as the rate is presented in 2's complement format, this can be done as an arithmetic shift right by 2 to handle the number sign correctly. So the actual data for rate calculation will be 0xFFE5 which equals -27 decimal. The sensitivity of the SCC1300-D04 is 18 LSB/(°/s) (Table 2) so the rate in degrees per second will be:

Rate_X[dps] = -27[LSB] / 18 LSB/dps = -1.5 dps

5.3.2 Gyro Temperature Output Register

The gyroscope ASIC offers temperature information that has a linear response to temperature change. The temperature sensor reading does not reflect absolute ambient temperature. To use the temperature sensor as an absolute temperature sensor, the offset and sensitivity should be measured and calibrated at system level.

Temperature data is presented in the Temp register (0x0A) in 14-bit, 2's complement format. The bits 1:0 do not contain temperature data and they must be discarded when making temperature calculations.

The temperature register's typical output at +23 °C is -1755 counts, and 1 °C change in temperature typically corresponds to 65 counts. Temperature information is converted from counts to [°C] as follows:

$$Temp[^{o}C] = (Temp[LSB] + 3250) / 65,$$

where Temp[LSB] is the TEMP register content in counts and Temp[°C] is the equivalent temperature in Celsius.

Temperature sensor offset calibration error at 25°C: ≤ ±15 °C
Temperature sensor sensitivity calibration error : ≤ 5%

5.3.2.1 Example of GYRO Temperature Conversion

For example: the Temp register (0x0A) data is 0xEF5A. The bits 1:0 need to be discarded (Table 12) so the actual temperature data will be 0xFBD6m which equals -1066 decimal. Using the conversion formula above the actual temperature in °C will be:

Temp[°C] = (-1066 + 3250) / 65 = 33.6 °C

5.4 Accelerometer Interface

This chapter describes the SCC1300 accelerometer sensor ASIC interface and how to use it. The accelerometer sensor ASIC SPI interface uses 8-bit addressing.

5.4.1 Accelerometer SPI Communication Overview

Each communication frame contains 16 bits (two 8-bit bytes). The SPI frame format and transfer protocol for the accelerometer is presented in Figure 13 below. The accelerometer captures data on the SCK's rising edge (MOSI line) and data is propagated on the SCK's falling edge (MISO line). This is equal to SPI Mode 0 (CPOL = 0 and CPHA = 0). The SPI transmission is always started with the CSB falling edge and terminated with the CSB rising edge.

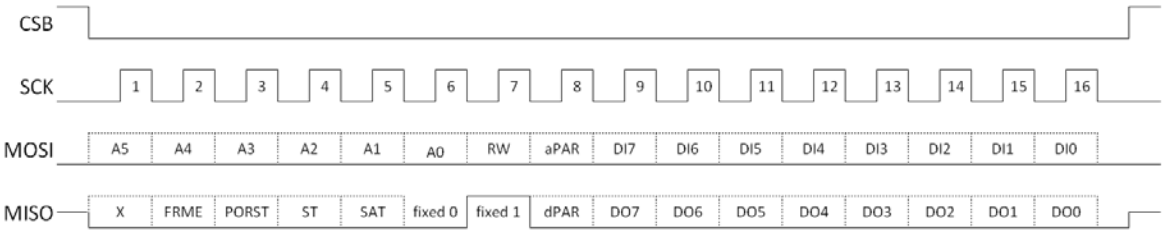

Figure 13. SPI frame format for the accelerometer interface

- MOSI
  - A5:A0 Register address
  - R/W Read/Write selection, '0' = read, '1' = write
  - aPAR Odd parity for bits A5:A0, R/W
  - DI7:DI0 Input data for data write
- MISO
  - Bit 1 Not defined
  - FRME FRaMe Error indication (from previous frame)
  - Bit 3-5 status bits
    - PORST Power On Reset Status
    - ST Self Test error
    - SAT Output SATuration indicator
  - Bit 6 Fixed bit, always '0'
  - Bit 7 Fixed bit, always '1'
  - dPAR Odd parity for output data (DO7:DO0)
  - DO7:DO0 Output data

The first 8 bits in the MOSI line contain info about the operation (read/write) and the register address being accessed. The first 6 bits form an address field for the selected operation, which is defined by bit 7 ('0' = read '1' = write) and is followed by an odd parity bit (aPAR) for the address. The following 8 bits in the MOSI line contain data for the write operation and are ignored in case of a read operation.

The first bits in the MISO line are the Frame Error bit of the previous frame (FRME), the Power On Reset STatus bit (PORST), the Self-Test status bit (ST), the Saturation status bit (SAT), the fixed zero bit, the fixed one bit and the Odd Parity bit for output data (dPAR). Parity is calculated from data that is currently being sent. The following 8 bits contain data for a read operation. During a write operation, these data bits are the previous data bits of the addressed register.

For write commands, data is written into the addressed register on the rising edge of the CSB. If the command frame is invalid, data will not be written into the register.

For read commands, the output register is shifted out MSB first to the MISO output. An attempt to read a reserved register outputs data of 0x00.

During the CSB high state between data transfers, the MISO line is kept in high-impedance state.

5.4.2 Accelerometer SPI Read Frame

An example of X-axis acceleration read command is presented in Figure 14.

16-bit acceleration data is sent in two 8-bit data frames. Each frame contains a parity bit for data (odd parity). The acceleration data is presented in 2's complement format.

When reading acceleration data, always read the MSB register before the LSB register because reading of MSB latches the LSB so the data in both registers will be from the same moment in time.

The master gives the register address to be read via the MOSI line: '05' in hex format and '000101' in binary format, register X_MSB. The 7th bit is set to '0' to indicate a read operation, and the 8th bit is 1 for odd parity.

The sensor replies to the requested operation by transferring the register content via the MISO line. After transferring the X_MSB register content, the master gives next register address to be read: '04' in hex format and '000100' in binary format, register X_LSB. The sensor replies to the requested operation by transferring the register content MSB bit first.

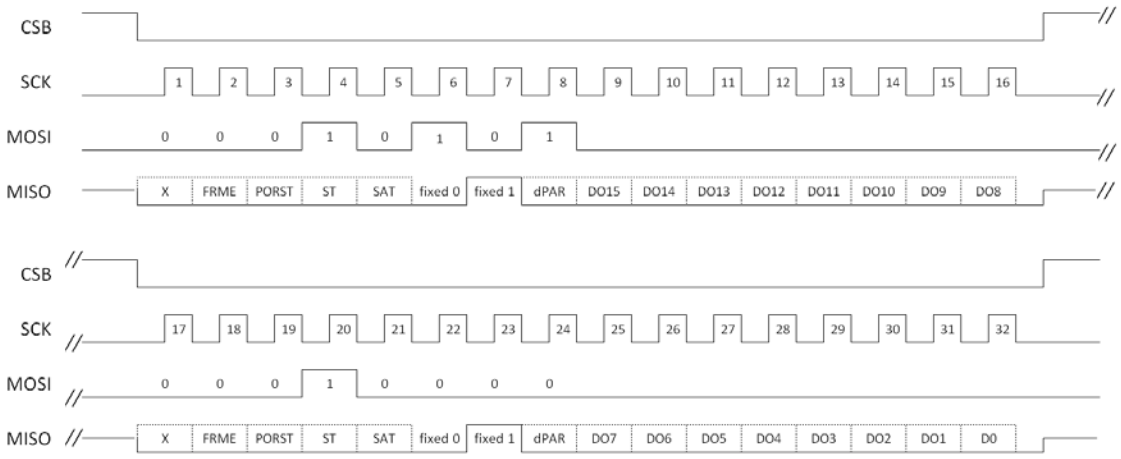

Figure 14. Example of 16-bit acceleration data transfer from registers X_MSB, X_LSB (05h, 04h)

DO15…DO0 bits are acceleration data (DO15 = MSB) and parity (dPAR) is odd parity for each 8-bit data transmission. FRME is the possible frame error bit of previous frame, PORST is the reset bit, ST is the self-test status bit and SAT is the output saturation status bit.

See section 5.5.2 for details about acceleration data conversion.

5.4.3 Accelerometer SPI Write Frame

An example of a CTRL register write command is presented in Figure 15.

The master gives the register address to be written via the MOSI line: the CTRL register is '01' in hex format and '000001' in binary format. The 7th bit is set to '1' to indicate a write operation, and the 8th bit is 1 for odd parity. MISO data bits DO0 ... DO7 are the previous data bits of the CTRL register.

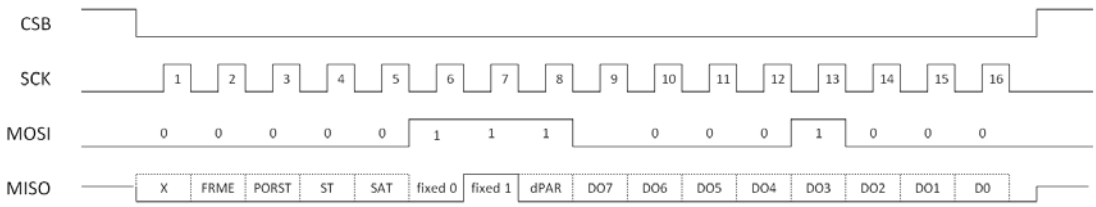

Figure 15. Example of CTRL register write, set PORST = 0, Start STC (see Table 11)

5.4.4 Accelerometer Decremented Register Read Operation

Figure 16 shows a decremented read operation where the content of four output registers is read by one SPI frame. After normal register addressing and reading of one register content, the MCU keeps the CSB line low and continues supplying SCK pulses. After every 8 SCK pulses, the output data address is decremented by one and the previous acceleration output register's content is shifted out without parity bits. The parity bit is calculated and transferred only for the first 8 bits of data. From the X_LSB register address the ASIC output address jumps to Z_MSB. Decremented reading is possible only for registers X_LSB ... Z_MSB.

Accelerometer output registers are not updated during CSB low state, so the decremented read operation can be used to read all acceleration output registers' (Z_MSB ... X_LSB) content from the same moment of time. Decremented read is not recommended in fail-safe critical applications, because output data parity is only available for the first 8 bits of data.

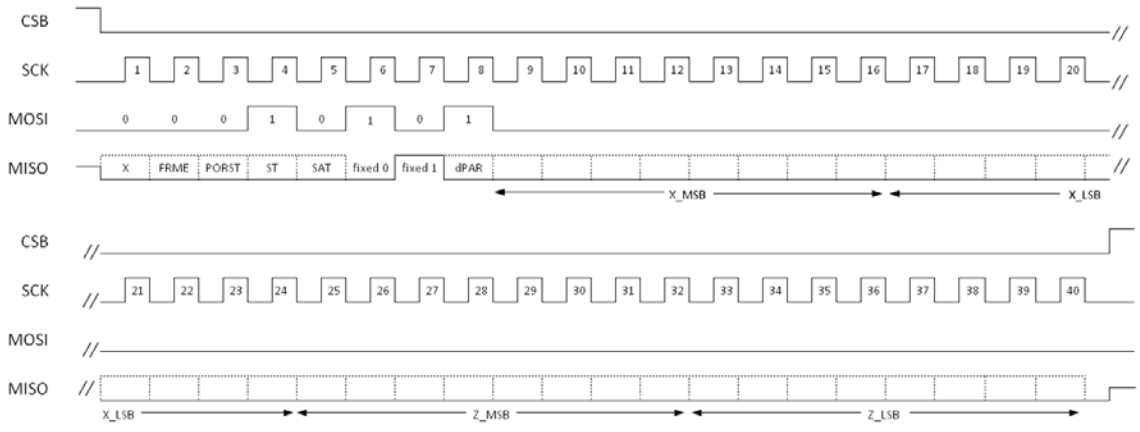

Figure 16. An Example of decremented read operation

5.4.5 Accelerometer SPI Error Conditioning (Self Diagnostics)

5.4.5.1 FRME bit

If the CSB is raised to '1' before sending all 16 SCKs in a frame, the frame is considered invalid. To support the decremented mode reading, the FRaMe Error is raised if the number of SCK pulses is not divisible by 8. The FRME bit is also set in case a wrong address parity (aPar) is sent. When an invalid frame is received, the last command is simply ignored and the register contents are left unchanged. The bit STATUS.FRME in the STATUS register (0x02) is set to indicate this error condition. During the next SPI frame this error bit is sent out as FRME status bit on the MISO line. The frame error condition will be reset only when a correct frame is received.

5.4.5.2 PORST bit

The PORST bit is set if the chip is reset (HW reset by Power On Reset or supply on/off) or under voltage is detected. This bit is also set after power-up because the chip has been in a reset state. PORST can be set to zero (reset) by writing CTRL.PORST = 0. Software (SW) reset does not set the PORST bit.

When CTRL.PORST bit is written to 0 via the SPI, there is a 300ns delay before the register value is set to zero.

5.4.5.3 ST bit

The self-test frame status bit (ST) is set if STC or STS is alarmed or memory checksum test is not passed.

- CASE 1: Checksum fails and the ST frame bit is set to 1. ST is set back to zero only when a new checksum calculation is passed.

- CASE 2: The ST frame bit is set to 1 because STC or STS is alarmed. In this case the ST frame bit can be cleared by reading the INT_STATUS register.

5.4.5.4 SAT bit

The saturation status (SAT) is set to 1 if any of the axis X,Y,Z output values is saturated. SAT can be cleared by reading the INT_STATUS register. This bit is kept high even after the failure condition is over if not cleared by reading the INT_STATUS register.

5.4.5.5 aPAR bit

The aPAR is an odd parity bit of input address + R/W-bit. The master writes and the slave checks this bit.

- If there is a parity error and R/W = '1', the write command is ignored and the FRME (frame error) bit is set in the STATUS register and in the SPI frame. The next correct SPI frame will zero this bit.

- If there is a parity error and R/W = '0', the read command is performed normally and the FRME bit is set in the STATUS register and in the SPI frame. The next correct SPI frame will zero this bit.

Table 14. Examples of correct address parity bit value

Address							
A5	A4	A3	A2	A1	A0	R/W	aPAR
0	0	0	0	0	0	0	**1**
1	1	1	1	1	1	1	**0**
1	0	1	0	1	0	1	**1**
0	1	0	1	0	1	0	**0**

5.4.5.6 dPAR bit

The dPAR bit is an odd parity bit for 8-bit data that is currently sent in the frame. The master compares this bit to the received data. By using dPAR, at least 1-bit errors in data transmission can be detected.

5.4.5.7 Fixed bits

Bits 6 and 7 in the MISO line are always fixed. Bit 6 should always be '0' and bit 7 always '1'. These bits can be used to verify that the MISO line is not permanently stuck to '1' or '0'.

5.4.5.8 SPI error effect on acceleration output data

1. **Reset stage:** When the component is in reset or under voltage state, the PORST bit in the SPI frame and the CTRL.PORST bit are set. In addition, all acceleration output register values are set to zero.
2. **Saturation:** When acceleration exceeds the sensor's measurement range, the output data is saturated to ± 6.3 g (-4096 / 4095 counts)
3. **Self-diagnostic failure:** The ST bit in the SPI frame is set when the memory diagnostic or signal path diagnostic functions fail. In addition, acceleration output data is forced to 0x7FFF if memory diagnostic fails or to 0xFFFF if signal path diagnostic functions (STC/STS) fail.

5.5 Accelerometer ASIC Addressing Space

The SCC1300 accelerometer ASIC register contents and bit definitions are described in detail in the following sections.

Table 15. Accelerometer register address space

Address hex	Register Name	Bits	Read/ Write	Description
01h	CTRL	7:0	R/W	Please refer to Table 16 for CTRL register details.
02h	STATUS	7:2	R	Reserved
		1	R	CSMERR: EEPROM checksum error 1 – Error, 0 – No error CSMERR also sets ST bit in SPI frame
		0	R	FRME: SPI frame error. Bit is reset when next correct SPI frame is received. FRME also sets FRME bit in SPI frame
03h	RESET	7:0	R/W	Writing 0C'hex, 05'hex, 0F'hex in this order resets component
04h	X_LSB	7:0	R	X-axis LSB data frame (Read always X_MSB prior to X_LSB)
05h	X_MSB	7:0	R	X-axis MSB data bits (Reading of this register latches X_LSB)
06h	Y_LSB	7:0	R	Y-axis LSB data frame (Read always Y_MSB prior to Y_LSB)
07h	Y_MSB	7:0	R	Y-axis MSB data bits (Reading of this register latches Y_LSB)
08h	Z_LSB	7:0	R	Z-axis LSB data frame (Read always Z_MSB prior to Z_LSB)
09h	Z_MSB	7:0	R	Z-axis MSB data bits (Reading of this register latches Z_LSB)
12h	TEMP_LSB	7:0	R	Data bits [7:0] of temperature sensor Always read TEMP_MSB prior to TEMP_LSB
13h	TEMP_MSB	7:0	R	Data bits [15:8] of temperature sensor Reading of this register latches TEMP_LSB
16h	INT_STATUS	7	R	Reserved
		6	R	SAT: Saturation status of output data 1 – Over range detected, at least one of XYZ axis is saturated and output data is not valid. 0 – Data in range SAT bit is also visible in SPI frame. This bit can be active after start-up, reset or PORST stage before signal path settles to final value. If accelerometer self diagnostics is used follow power-up sequence to acknowledge this bit (Table 11).
		5	R	STS: Status of gravitation based start-up self test 1 – Failure 0 – No failure STS also sets ST bit in SPI frame
		4	R	STC: Status of continuous self test 1 – Failure 0 – No failure STC also sets ST bit in SPI frame
		3:0	R	Reserved
27h	ID	7:0	R	Customer readable component identification number, value 90h

Note: INT_STATUS: The bits in the interrupt status register and the corresponding SPI frame bits are cleared after this register has been read. Register reading is treated as interrupt acknowledgement signal. Bits in this register are kept active even if the failure condition is over until they are acknowledged by reading the register.

5.5.1 Control Register (CTRL)

Table 16. SCC1300 accelerometer CTRL control register (address 01h) bit level description

Bit	Mode	Initial Value	Name	Description
7	R/W	0		Reserved, write to 0
6	RW	0	PORST	1 means reset state. Bit is set to 1 when the chip is reset by supply off control or under voltage control. Bit is set after supply off/on transition or startup. This bit can not be set by SPI but it can be reset by writing a 0 to it. This bit is also sent as Bit3 (PORST) of SPI output data frame on MISO.
5	R/W	0	PDOW	Write 1 to set accelerometer to power down mode
4	R/W	0		Reserved, write to 0
3	R/W	0	ST	Write 1 to enable continuous self test calculation (STC). This bit can not be set to 1 if CTRL.PDOW or CTRL.MST is already 1 or if CTRL.PDOW or CTRL.MST is being set by the current SPI command. Use INT_STATUS.STC and the ST bit in SPI frame for test result monitoring.
2	R/W	0	MST	Memory self-test function is activated when user sets this bit to 1. The bit is reset to 0 when self test is over. This bit can not be set to 1 if CTRL.PDOW is already 1 or if CTRL. PDOW is being set by the current SPI command. Test is done automatically during start-up. Set other bits in CTRL register to zero with a separate SPI command before starting memory self-test with CTRL.MST command. Use STATUS.CSMERR and the ST bit in SPI frame for test result monitoring. During memory self test, SPI access is prevented for 85us.
1	R/W	0	ST_CFG	Write 1 to start gravitation based start-up self-test calculation (STS). This bit can not be set to 1 if CTRL.PDOW or CTRL.MST is already 1 or if CTRL.PDOW or CTRL.MST is being set by the current SPI command. STC and STS have same priority and they can be set and used simultaneously. This bit is set to 0 when test is over. Use INT_STATUS.STS and ST bit of SPI frame for test result monitoring.
0	R/W	0		Reserved, write to 0

5.5.2 Acceleration output registers

Acceleration data is presented in 14-bit, 2's complement format in registers X_LSB … Z_MSB. At 0 g acceleration the output is ideally 0000h. Acceleration data bit weights are shown in Table 17:

Table 17. Acceleration output bit weights [mg] (Sensitivity 650 LSB/g).

DOUT MSB bits(7:0)								DOUT LSB bits(7:0)							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
s	s	3150.8	1575.4	787.7	393.8	196.9	98.5	49.2	24.6	12.3	6.15	3.08	1.54	x	x

s = sign bit

5.5.2.1 Example of acceleration data conversion

For example, if X_MSB = 0xFA and X_LSB = 0xEC, the combined X-axis acceleration data is 0xFAEC. Acceleration output bits 1:0 are not used and need to be discarded (Table 17). As the data is presented in 2's complement format, the number sign needs to be handled correctly. This can be done as an arithmetic shift right by 2. So the actual data for acceleration calculation will be 0xFEBB which equals -325 decimal. The sensitivity of the SCC1300-D04 is 650 LSB/g (Table 2) so the acceleration in g's will be:

X_acc[g] = -325[LSB] / 650 LSB/g = -0.5 g

5.5.3 Accelerometer Temperature Output Registers

Offset of the accelerometer temperature data is factory calibrated, but sensitivity varies from part to part. Temperature data is presented in 13-bit unsigned format and uses 13 bits (13:1) of TEMP_MSB/TEMP_LSB registers. Always read TEMP_MSB prior to TEMP_LSB because reading the MSB register latches the LSB register.

5.5.3.1 Example of accelerometer temperature conversion

Table 18. Bit level description for the accelerometer temperature registers

TEMP MSB bits(7:0)								TEMP LSB bits(7:0)							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
x	x	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0	x

x = not used

The temperature registers' typical output at +23 °C is 4096 counts and a 1 °C change in temperature typically corresponds to 25.6 counts. Temperature information is converted from counts to [°C] as follows:

$$Temp[°C] = (23 \pm 10) + \frac{Temp_{LSB} - 4096}{k}$$

where Temp[°C] is temperature in Celsius and $Temp_{LSB}$ is temperature from TEMP_MSB and TEMP_LSB registers in decimal format, bits(T12:0). k is the temperature slope factor specified as

	Min	Typ	Max	Unit
k	22.4	25.6	28.8	LSB/^{o}C

6 Application Information

6.1 Application Circuitry and External Component Characteristics

Recommended circuit diagram is presented in Figure 17. The component characteristics are presented in Table 19.

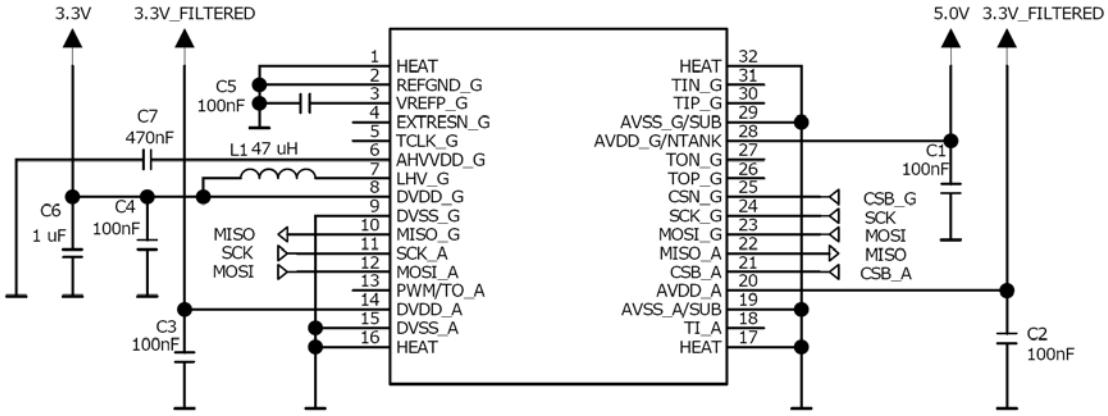

Figure 17. Recommended circuit diagram of the SCC1300.

The optional filtering recommendation for a better PSRR (Power Supply Rejection Ratio) is presented in Figure 18. Please note that PSSR filtering is optional and not required if the 3.3V power supply is already stable enough. RC filtering (R1 & C8 without L2) could also be sufficient for most cases.

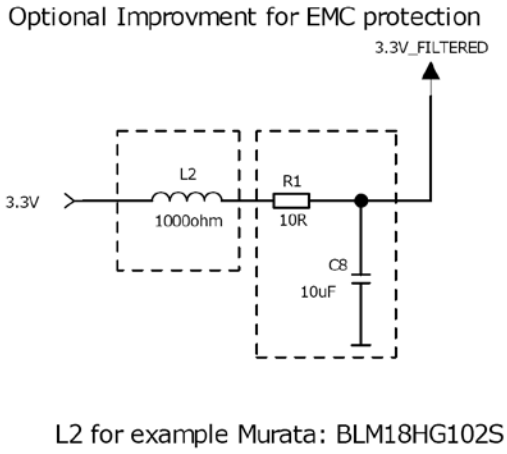

Figure 18. Optional filtering recommendation to improve PSRR if required.

6.1.1 Separate Analog and Digital Ground Layers with Long Power Supply Lines

If power supply routings/cablings are long, separate ground cabling, routing and layers for analog and digital supply voltages should be used to avoid excessive power supply ripple.

In the recommended circuit diagram (Figure 17) and layout example (Figure 20), joint ground is used as it is the simplest solution and is adequate as long as the supply voltage lines are not long (when connecting the SCC1300 directly to µC on the same PCB).

Table 19. SCC1300 external components

Component	Parameter	Min	Typ	Max	Unit
C1, C2, C3, C4, C5	Capacitance	70	100	130	nF
	ESR @ 1 MHz			100	mΩ
	Voltage rating	7			V
C7	Capacitance	376	470	564	nF
	ESR @ 1 MHz			100	mΩ
	Voltage rating	30			V
L1	Inductance	37	47	57	µH
	ESR L=47 µH			5	Ω
	Voltage rating	30			V
C6	Capacitance	0.7	1	1.3	µF
	ESR @ 1 MHz			100	mΩ
Optional for better PSRR:					
R1	Resistance		10		Ω
C8	Capacitance		4.7		µF
L2	Impedance		1k		Ω

6.2 Boost Regulator and Power Supply Decoupling in Layout

Recommended layout for DVDD_G/LHV pin decoupling is shown in Figure 19.

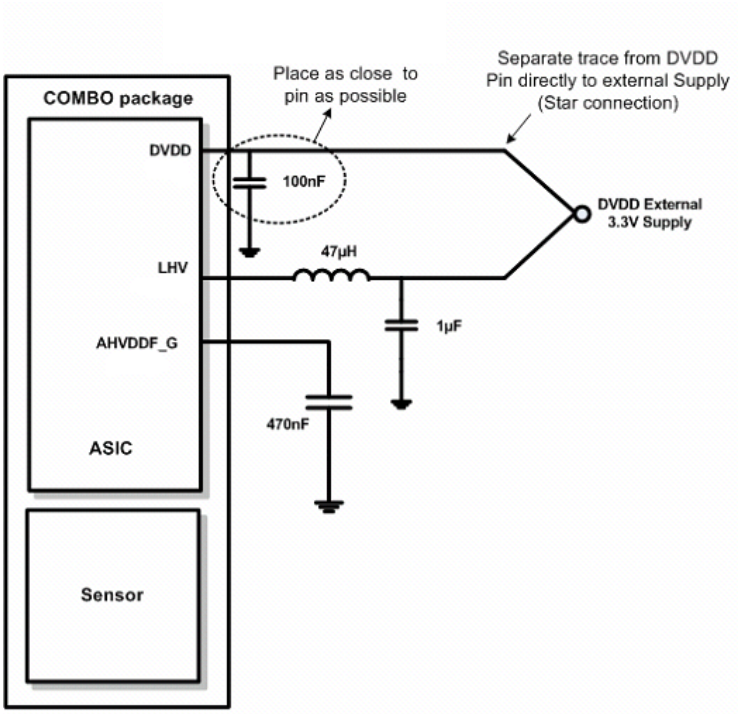

Figure 19. Layout recommendations for DVDD_G/LHV pin decoupling

6.2.1 Layout Example

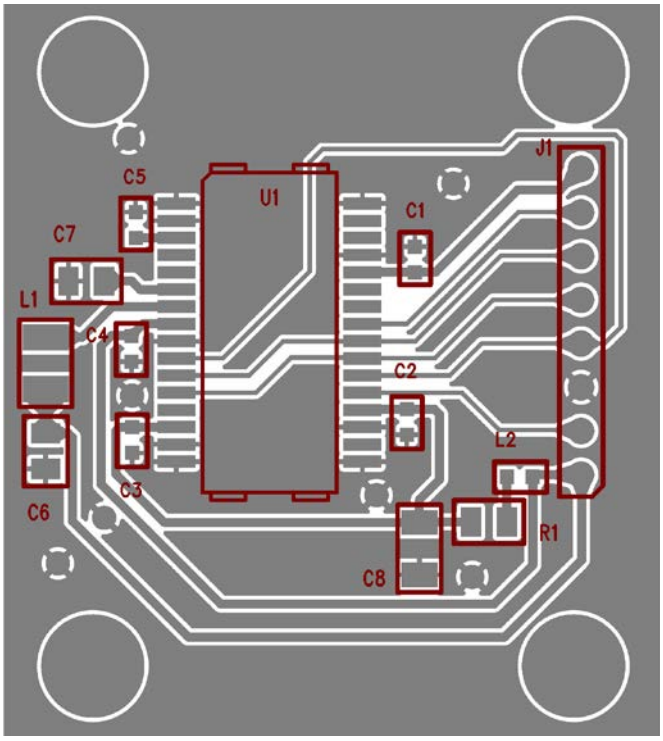

Figure 20. Example layout for the SCC1300

6.2.2 Thermal Connection

The component has heat sink pins to transfer internally generated heat from the package to ambient. Thermal resistance to ambient should be low enough not to self heat the device. If the internal junction temperature gets too high compared to ambient, this may lead to out of specification behavior.

Table 20. Thermal resistance

Component	Parameter	Min	Typ	Max	Unit
Thermal resistance Θ_{JA}	Total thermal resistance from junction to ambient			50	°C/W

6.3 Assembly Instructions

Usage of PCB coating materials may effect component performance. The coating material and coating process used should be validated. For additional assembly related details, please refer to “Technical Note 82” for assembly instructions.