SC905A
CDMA Cellular Phone Power Management IC

POWER MANAGEMENT

Description

The SC905A is a power management integrated circuit (PMIC) designed for the latest CDMA chip sets. The device provides four general purpose low dropout regulators (LDOs), and five low noise LDOs designed for analog circuits. The VMOT LDO can be used as a general purpose regulator or as an adjustable motor drive output that can supply up to 150mA to drive a vibrator motor.

Each LDO's enable and output voltage are controlled via the I^2C bus. The VTCXO output has an external enable pin that can be used instead of the register bit when timing is critical for minimizing sleep current. The VMOT also has an external enable pin for additional flexibility.

Initial power-on is achieved by activating either the ON button, the battery charger, or the HFPWR signal, and the PGOOD input is used by the microprocessor to latch power on or disable the device.

The thermally-efficient MLPQ-32 package combined with miniature ceramic bypass capacitors minimize required PCB area, making the SC905A ideal for space-conscious portable applications.

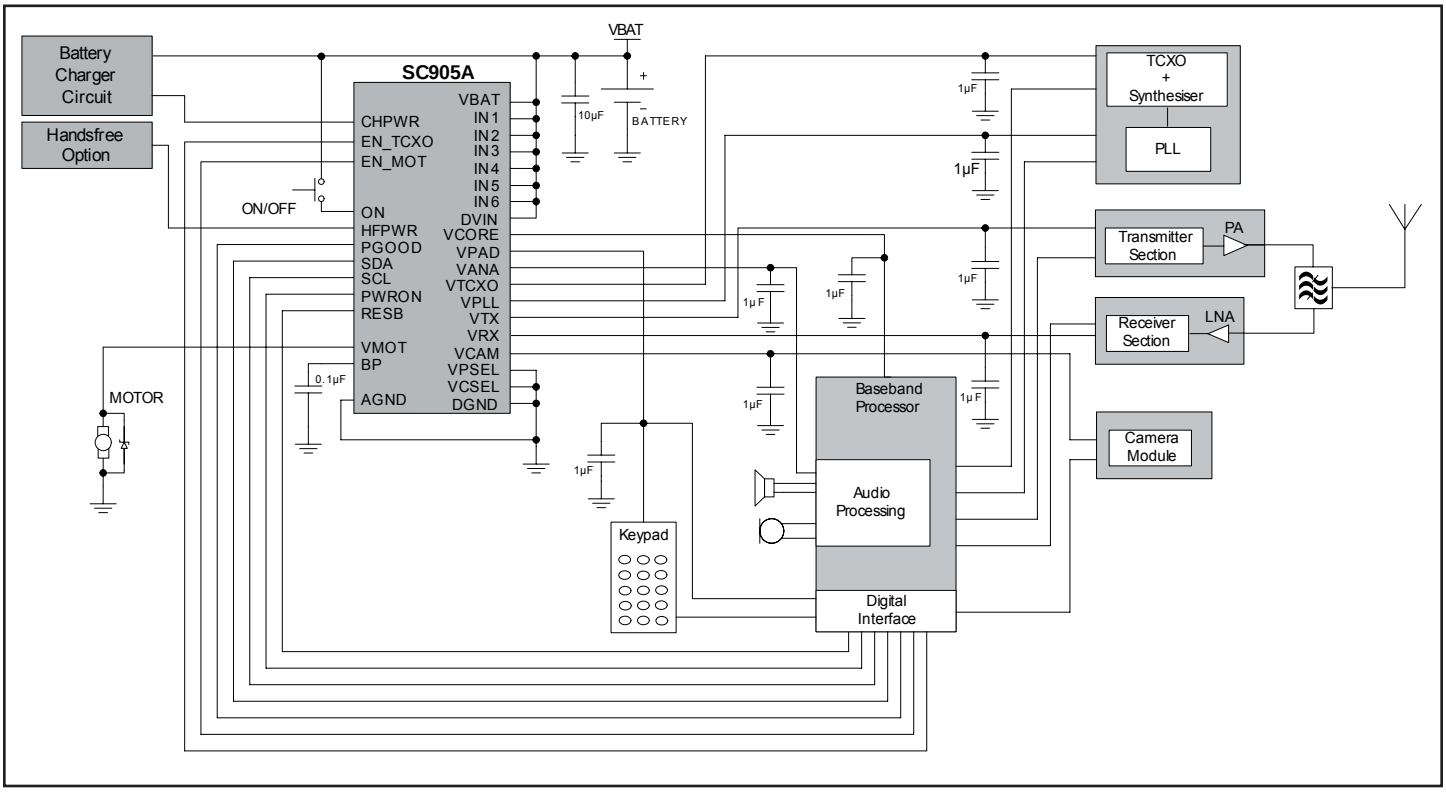
Features

- 9 LDO Linear Regulators
- CORE: 1.35V - 2.90V @ 300mA
- ANA: 2.55V - 2.90V @ 200mA
- PAD: 1.75V - 3.30V @ 300mA
- RX: 2.75V - 3.10V @ 150mA
- TX: 2.75V - 3.10V @ 150mA
- TCXO: 2.75V - 3.10V @ 80mA
- PLL: 2.75V - 3.10V @ 80mA
- Camera: 1.75V - 3.30V @ 100mA
- Motor Drive: 1.75V - 3.30V @ 150mA
- I^2C Interface for Microprocessor Control
- Less than 1µA Quiescent Current in Shutdown
- 65dB PSRR for Analog LDOs
- Over-Temperature Protection
- Power-On Control
- Small 5mm x 5mm 32-Pin MLPQ Package

Applications

- CDMA Cellular Handsets
- PDAs/Smartphones
- Wireless VOIP Handsets

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Input Supply Voltage	V_{IN}	-0.3 to +7	V
Digital Input Voltage	V_{DIG}	-0.3 to V_{IN}+0.3	V
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Operating Junction Temperature Range	T_J	-40 to +125	°C
Peak IR Reflow Temperature	T_{LEAD}	260	°C
Storage Temperature	T_{STG}	-60 to +150	°C
Thermal Resistance Junction to Ambient(1)	θ_{JA}	26	°C/W
ESD Protection Level(2)	ESD	2	kV

Notes:
(1) Calculated from package in still air, mounted to 3" x 4.5", 4 layer FR4 PCB with thermal vias under the exposed pad as per JESD51 standards.
(2) Tested according to JEDEC standard JESD22-A114-B.

Electrical Characteristics

Unless otherwise noted V_{IN} = 3.7V, T_A = -40 to +85˚C. Typical values are at T_A = +25˚C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
General						
Supply Voltage	V_{IN}		2.7		5.5	V
Shutdown Current	I_{SD}	ON = 0V, HFPWR = 0V, CHPWR = 0V, PGOOD = 0V			1	µA
Quiescent Supply Current	I_{SU}	Default Start-Up Mode		300		µA
	I_{STBY}	I²C, V_{REF} Active, All Outputs Disabled		30	60	µA
Supply Bypass Capacitor	C_{VCC}	At Each Power Input Pin		1		µF
Start-Up Time	t_{SU}	C_{BP} = 0.1µF		25		ms
Under-Voltage Lockout	UVLO	Descending, Hysteresis = 50mV		2.5		V
Over-Temperature	OT	Hysteresis = 20°C		160		°C
Digital Inputs						
Digital Input Voltage(1)	V_{IL}				0.4	V
	V_{IH}		1.25			V
Digital Input Current	I_{DIG}	Logic Level High or Low	-0.2		0.2	µA
Digital Outputs						
Digital Output Voltage(2)	V_{OL}	I_{SINK} = 1.2mA		2	10	%VPAD
	V_{OH}	I_{SOURCE} = 0.5mA, VPAD ≥ 1.8V	90	98		%VPAD
LDO Regulator (CORE) - 300mA						
Output Voltage Accuracy(3)	ΔV_{OUT}	1.35V ≤ V_{OUT} ≤ 2.90V, I_{OUT} = 1mA, V_{OUT} +0.35V ≤ V_{IN} ≤ 5.5V	-75		+75	mV
Current Limit	I_{LIM}	V_{CORE} = 0V	350		900	mA
Default At Start-Up: ON	V_{OUT-HI}	VCSEL - High		1.80		V
	V_{OUT-LO}	VCSEL - Low		1.35		V

Electrical Characteristics (Cont.)

Parameter	Symbol	Condition	Min	Typ	Max	Units
LDO Regulator (CORE) - 300mA (Cont.)						
Line Regulation	REG_{LINE}	I_{OUT} = 1mA, V_{OUT} +0.35V < V_{IN} < 5.5V		2.5	12	mV
Load Regulation	REG_{LOAD}	1mA < I_{OUT} < 300mA		-3	-30	mV
Dropout Voltage	V_{DO}	V_{OUT} = 2.90V, I_{OUT} = 300mA		300	350	mV
Power Supply Rejection Ratio	$PSRR_{CORE}$	f = 10Hz - 1kHz, C_{OUT} = 1µF, I_{OUT} = 50mA		50		dB
LDO Regulator (PAD) - 300mA						
Output Voltage Accuracy(3)	ΔV_{OUT}	1.75V ≤ V_{OUT} ≤ 3.30V, I_{OUT} =1mA, V_{OUT} +0.35V ≤ V_{IN} ≤ 5.5V	-75		+75	mV
Current Limit	I_{LIM}	V_{PAD} = 0V	350		900	mA
Default at Start-Up: ON	V_{OUT-HI}	VPSEL - High		3.00		V
	V_{OUT-LO}	VPSEL - Low		2.20		V
Line Regulation	REG_{LINE}	I_{OUT} = 1mA, V_{OUT} +0.35V < V_{IN} < 5.5V		2.5	12	mV
Load Regulation	REG_{LOAD}	1mA < I_{OUT} < 300mA		-3	-30	mV
Dropout Voltage	V_{DO}	V_{OUT} = 3.30V, I_{OUT} = 300mA		300	350	mV
Power Supply Rejection Ratio	$PSRR_{PAD}$	f = 10Hz - 1kHz, C_{OUT} = 1µF, I_{OUT} = 50mA		50		dB
LDO Regulator (ANA) - 200mA						
Output Voltage Accuracy(4)	ΔV_{OUT}	2.55V ≤ V_{OUT} ≤ 2.90V, I_{OUT} = 1mA, V_{OUT} +0.35V ≤ V_{IN} ≤ 5.5V	-75		+75	mV
Current Limit	I_{LIM}	V_{ANA} = 0V	250		650	mA
Default At Start-Up: ON	V_{OUT}			2.60		V
Line Regulation	REG_{LINE}	I_{OUT} = 1mA, V_{OUT} +0.35V < V_{IN} < 5.5V		2.5	12	mV
Load Regulation	REG_{LOAD}	1mA < I_{OUT} < 200mA		-3	-20	mV
Dropout Voltage	V_{DO}	V_{OUT} = 2.90V, I_{OUT} = 200mA		200	250	mV
Power Supply Rejection Ratio	$PSRR_{ANA}$	f = 10Hz - 1kHz, C_{OUT} = 1µF, I_{OUT} = 50mA		65		dB
Output Voltage Noise	e_n	f = 10Hz to 100kHz, I_{OUT} = 50mA, C_{BP} = 0.1µF, C_{OUT} = 1µF		45		μV_{RMS}
LDO Regulator (TCXO) - 80mA						
Output Voltage Accuracy(4)	ΔV_{OUT}	2.75V ≤ V_{OUT} ≤ 3.10V, I_{OUT} = 1mA, V_{OUT} +0.35V ≤ V_{IN} ≤ 5.5V	-75		+75	mV
Current Limit	I_{LIM}	V_{TCXO} = 0V	250		650	mA
Default At Start-Up: ON	V_{OUT}			3.05		V
Line Regulation	REG_{LINE}	I_{OUT} = 1mA, V_{OUT} +0.35V < V_{IN} < 5.5V		2.5	12	mV
Load Regulation	REG_{LOAD}	1mA < I_{OUT} < 80mA		-3	-20	mV
Dropout Voltage	V_{DO}	V_{OUT} = 3.10V, I_{OUT} = 80mA		200	250	mV
Power Supply Rejection Ratio	$PSRR_{TCXO}$	f = 10Hz - 1kHz, C_{OUT} = 1µF, I_{OUT} = 50mA		65		dB
Output Voltage Noise	e_n	f = 10Hz - 100kHz, I_{OUT} = 50mA, C_{BP} = 0.1µF, C_{OUT} = 1µF		45		μV_{RMS}

Electrical Characteristics (Cont.)

Parameter	Symbol	Condition	Min	Typ	Max	Units
LDO Regulator (TX) - 150mA						
Output Voltage Accuracy(4)	ΔV_{OUT}	$2.75V \le V_{OUT} \le 3.10V$, I_{OUT} = 1mA, V_{OUT} +0.35V ≤ V_{IN} ≤ 5.5V	-75		+75	mV
Current Limit	I_{LIM}	V_{TX} = 0V	250		650	mA
Default At Start-Up: OFF	V_{OUT}			3.05		V
Line Regulation	REG_{LINE}	I_{OUT} = 1mA, V_{OUT} +0.35V < V_{IN} < 5.5V		2.5	12	mV
Load Regulation	REG_{LOAD}	1mA < I_{OUT} < 150mA		-3	-20	mV
Dropout Voltage	V_{DO}	V_{OUT} = 3.10V, I_{OUT} = 150mA		200	250	mV
Power Supply Rejection Ratio	$PSRR_{TX}$	f = 10Hz - 1kHz, C_{OUT} = 1µF, I_{OUT} = 50mA		65		dB
Output Voltage Noise	e_n	f = 10Hz - 100kHz, I_{OUT} = 50mA, C_{BP} = 0.1µF, C_{OUT} = 1µF		45		μV_{RMS}
LDO Regulator (RX) - 150mA						
Output Voltage Accuracy(4)	ΔV_{OUT}	$2.75V \le V_{OUT} \le 3.10V$, I_{OUT} = 1mA, V_{OUT} +0.35V ≤ V_{IN} ≤ 5.5V	-75		+75	mV
Current Limit	I_{LIM}	V_{RX} = 0V	250		650	mA
Default At Start-Up: OFF	V_{OUT}			3.05		V
Line Regulation	REG_{LINE}	I_{OUT} = 1mA, V_{OUT}+0.35V < V_{IN} < 5.5V		2.5	12	mV
Load Regulation	REG_{LOAD}	1mA < I_{OUT} < 150mA		-3	-20	mV
Dropout Voltage	V_{DO}	V_{OUT} = 3.10V, I_{OUT} = 150mA		200	250	mV
Power Supply Rejection Ratio	$PSRR_{RX}$	f = 10Hz - 1kHz, C_{OUT} = 1µF, I_{OUT} = 50mA		65		dB
Output Voltage Noise	e_n	f = 10Hz - 100kHz, I_{OUT} = 50mA, C_{BP} = 0.1µF, C_{OUT} = 1µF		45		μV_{RMS}
LDO Regulator (CAM) - 100mA						
Output Voltage Accuracy(3)	ΔV_{OUT}	$1.75V \le V_{OUT} \le 3.30V$, I_{OUT} = 1mA V_{OUT} +0.35V ≤ V_{IN} ≤ 5.5V	-75		+75	mV
Current Limit	I_{LIM}	V_{CAM} = 0V	250		650	mA
Default At Start-Up: OFF	V_{OUT}			2.20		V
Line Regulation	REG_{LINE}	I_{OUT} = 1mA, V_{OUT} +0.35V < V_{IN} < 5.5V		2.5	12	mV
Load Regulation	REG_{LOAD}	1mA < I_{OUT} < 100mA		-3	-20	mV
Dropout Voltage	V_{DO}	V_{OUT} = 3.30V, I_{OUT} = 100mA		200	250	mV
Power Supply Rejection Ratio	$PSRR_{CAM}$	f = 10Hz - 1kHz, C_{OUT} = 1µF, I_{OUT} = 50mA		50		dB
LDO Regulator (PLL) - 80mA						
Output Voltage Accuracy(4)	ΔV_{OUT}	$2.75V \le V_{OUT} \le 3.10V$, I_{OUT} = 1mA, V_{OUT} +0.35V ≤ V_{IN} ≤ 5.5V	-75		+75	mV
Current Limit	I_{LIM}	V_{PLL} = 0V	250		650	mA

Electrical Characteristics (Cont.)

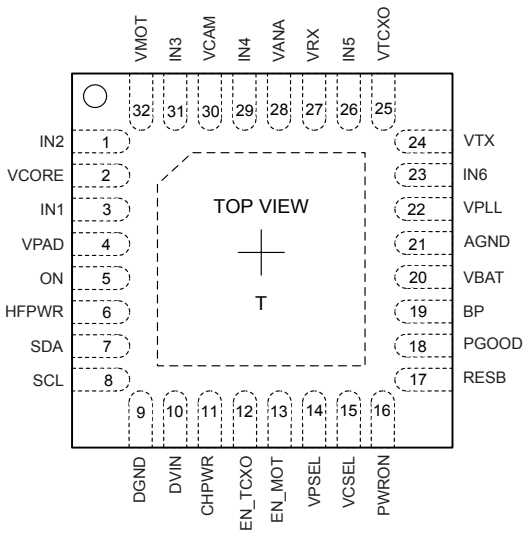
Parameter	Symbol	Condition	Min	Typ	Max	Units
Default At Start-Up: OFF	V_{OUT}			3.05		V
Line Regulation	REG_{LINE}	I_{OUT} = 1mA, V_{OUT} +0.35V < V_{IN} < 5.5V		2.5	12	mV
Load Regulation	REG_{LOAD}	1mA < I_{OUT} < 80mA		-3	-20	mV
Dropout Voltage	V_{DO}	V_{OUT} = 3.10V, I_{OUT} = 80mA		200	250	mV
Power Supply Rejection Ratio	$PSRR_{PLL}$	f = 10Hz - 1kHz, C_{OUT} = 1µF, I_{OUT} = 50mA		65		dB
Output Voltage Noise	e_n	f = 10Hz - 100kHz, I_{OUT} = 50mA, C_{BP}= 0.1µF, C_{OUT} = 1µF		45		$µV_{RMS}$
LDO Regulator (MOT) - 150mA						
Output Voltage Accuracy(3)	ΔV_{OUT}	1.75V ≤ V_{OUT} ≤ 3.30V, I_{OUT} = 1mA, V_{OUT} +0.35V ≤ V_{IN} ≤ 5.5V	-75		+75	mV
Current Limit	I_{LIM}	V_{MOT} = 0V	250		650	mA
Default at Start-Up: OFF	V_{OUT}			1.80		V
Line Regulation	REG_{LINE}	I_{OUT} = 1mA, V_{OUT} +0.35V < V_{IN} < 5.5V		2.5	12	mV
Load Regulation	REG_{LOAD}	1mA < I_{OUT} < 150mA		-3	-20	mV
Dropout Voltage	V_{DO}	V_{OUT} = 3.30V, I_{OUT} = 150mA		200	250	mV
Power Supply Rejection Ratio	$PSRR_{MOT}$	f = 10Hz - 1kHz, C_{OUT} = 1µF, I_{OUT} = 50mA		50		dB

Electrical Characteristics (Cont.)

Parameter	Symbol	Condition	Min	Typ	Max	Units
I²C Interface(5) Interface complies with slave mode I²C interface as described by Philips I²C specification version 2.1 dated January, 2000.						
Digital Input Voltage	V_{IL}				0.4	V
	V_{IH}		1.25			V
SDA Output Low Level		I_{DIN} (SDA) ≤ 3mA			0.4	V
Digital Input Current	I_{DG}		-0.2		0.2	µA
Hysteresis of Schmitt Trigger Inputs	V_{HYS}			0.1		V
Maximum Glitch Pulse Rejection	t_{SP}			50		ns
I/O Pin Capacitance	C_{IN}			10		pF
I²C Timing(5)						
Clock Frequency	SCL			400	440	kHz
SCL Low Period	t_{LOW}		1.3			µs
SCL High Period	t_{HIGH}		0.6			µs
Data Hold Time	t_{HD_DAT}		0			µs
Data Setup Time	t_{SU_DAT}		100			ns
Setup Time for Repeated START Condition	t_{SU_STA}		0.6			µs
Hold Time for Repeated START Condition	t_{HD_STA}		0.6			µs
Setup Time for STOP Condition	t_{SU_STO}		0.6			µs
Bus-Free Time Between STOP and START	t_{BUF}		1.3			µs
RESET Timeout Delay	t_{RD}		75	100	125	ms
Power-up Delay Between PAD, ANA, TXCO	t_{DELAY}	Delay Between Each Output Activating		100		µs
Maximum Glitch Pulse Rejection	t_{SP}			50		ns
Interface Start-up Time	t_{EN}	Bus Start-up Time After EN Pin is Pulled High			350	µs

Notes:
(1) Applies to pin names, ON, HFPWR, CHPWR, PGOOD, VCSEL, VPSEL, EN_MOT, EN_TCXO.
(2) Applies to pin names, PWRON, RESB.
(3) For V_{OUT} settings see Table A.
(4) For V_{OUT} settings see Table B.
(5) Guaranteed by design.

Pin Configuration



MLPQ32: 5X5 32 Lead

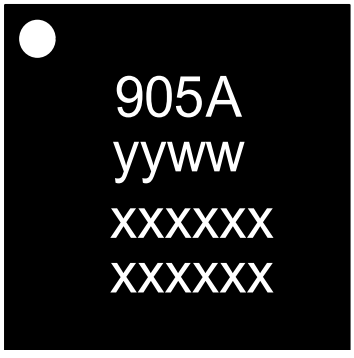
Ordering information

DEVICE	PACKAGE
SC905AMLTRT(1)(2)	MLP 5x5 32L
SC905AEVB	Evaluation Board

Notes:
(1) Available in tape and reel only. A reel contains 3,000 devices.
(2) Available in lead-free package only. Device is WEEE and RoHS compliant.

Marking Information

Top Marking

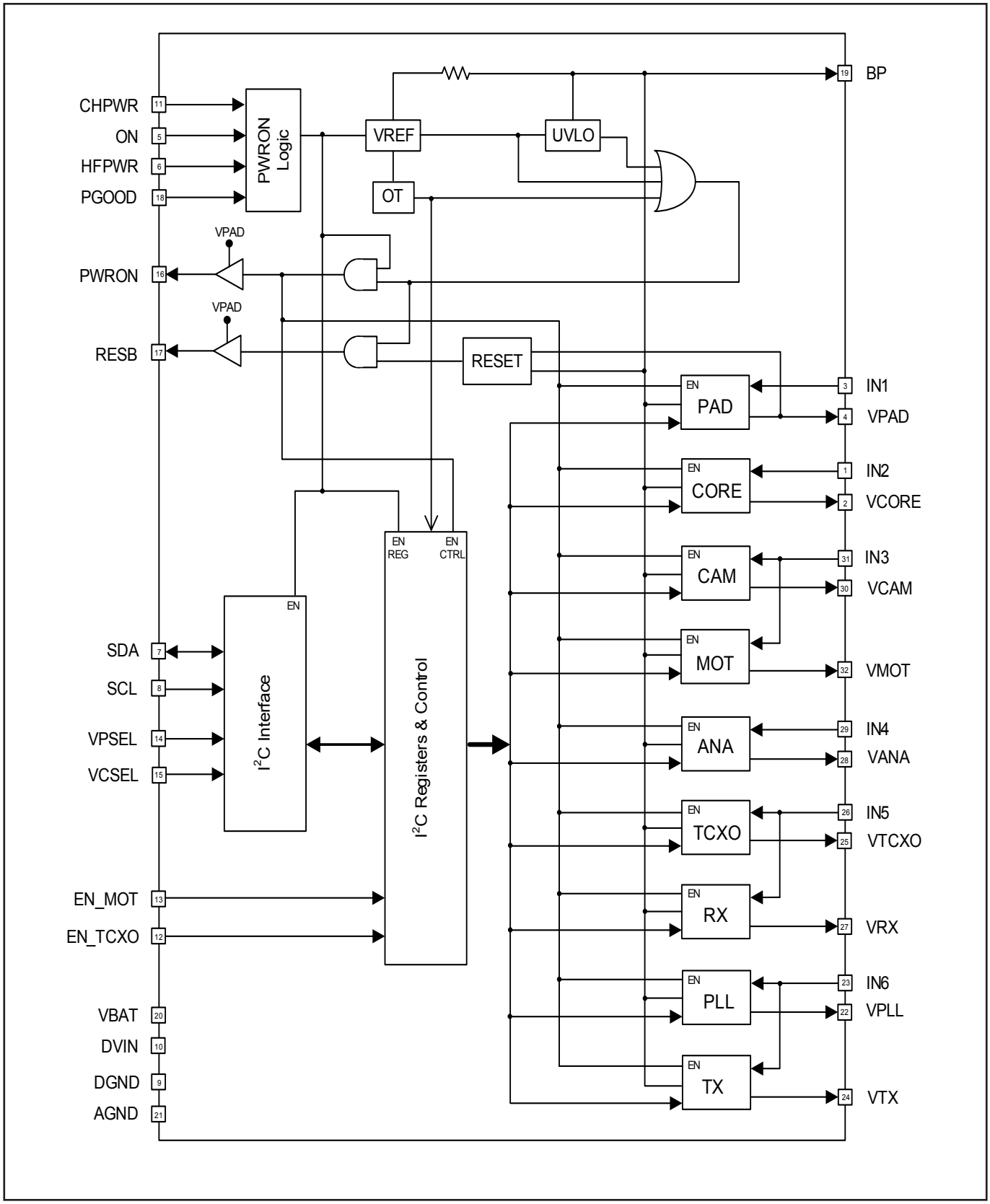


yy = two digit year of manufacture
ww = two digit week of manufacture
xxxxxx = Semtech Lot Number

Pin Descriptions

Pin #	Pin Name	I/O	Pin Function
1	IN2	Input	Input voltage terminal to VCORE LDO.
2	VCORE	Output	300mA LDO output for MSM core processor supply.
3	IN1	Input	Input voltage terminal to VPAD LDO.
4	VPAD	Output	300mA LDO PAD output to MSM I/O circuits.
5	ON	Input	Active high power on/off key. When the push button is closed it is shorted to battery.
6	HFPWR	Input	Power on input from accessory, active high.
7	SDA	Input/Output	Bi-directional open drain digital I/O. I^2C serial data.
8	SCL	Input	Digital input. I^2C serial clock.
9	DGND	-	Digital ground.
10	DVIN	Input	Main digital input voltage terminal.
11	CHPWR	Input	Logic input. OR'd with ON and HFPWR.
12	EN_TCXO	Input	Logic input. External enable for VTCXO LDO. State is recorded in bit 0 of the status register.
13	EN_MOT	Input	Logic input. External enable for VMOT LDO. State is recorded in bit 2 of the status register.
14	VPSEL	Input	Default control for VPAD LDO supply. Ground for 2.20V default, tie high for 3.00V.
15	VCSEL	Input	Default control for VCORE LDO supply. Ground for 1.35V default, tie high for 1.80V.
16	PWRON	Output	Logic OR output of ON, HFPWR and PGOOD. Active high.
17	RESB	Output	Reset output. Active low.
18	PGOOD	Input	Logic input signal from MSM to indicate power is good, latches the SC905A on. Low disables the SC905A.
19	BP	Output	LDO bypass output. Bypass with a 0.1µF capacitor.
20	VBAT	Input	Main battery supply input terminal.
21	AGND	-	Analog ground pin.
22	VPLL	Output	LDO output for PLL power.
23	IN6	Input	Input voltage terminal for VPLL & VTX LDOs.
24	VTX	Output	LDO output for transmitter power.
25	VTCXO	Output	LDO output for TCXO power.
26	IN5	Input	Input voltage terminal for VTCXO & VRX LDOs.
27	VRX	Output	LDO output for receiver power.
28	VANA	Output	LDO output for analog power.
29	IN4	Input	Input voltage terminal to VANA LDO.
30	VCAM	Output	LDO output for camera power.
31	IN3	Input	Input voltage terminal to VCAM & VMOT LDOs.
32	VMOT	Output	LDO output voltage for vibrator motor power. Can also be a general purpose output.
T	Thermal Pad	-	Pad for heatsinking purposes. Connect to ground plane using multiple vias. Not connected internally.

Block Diagram



Applications Information

General Description

The SC905A includes nine low dropout (LDO) voltage regulators to provide complete power regulation capability for CDMA handsets or other portable electronic equipment.

Five of the LDOs are designed to be used with analog circuitry such as audio, radio frequency, or oscillator circuits. These devices have very low noise levels and high power supply rejection. The output voltage range for four of these LDOs, VTCXO, VPLL, VTX and VRX, is 2.75V to 3.1V in 50mV steps, and for the fifth, VANA, the output voltage range is 2.55V to 2.9V in 50mV steps. The TCXO LDO has the additional feature of an external enable, EN_TCXO, which can be used when timing is critical.

Two other LDOs are general purpose regulators designed to be used with digital circuits. The noise requirements for these LDOs are relaxed, but their voltage range is expanded to cover the wide range of voltages needed for different types of functions. The outputs for these LDOs are VCORE and VPAD.

Two other LDOs are general purpose regulators that can be used with other peripheral circuits. The VMOT and VCAM outputs can be programmed to supply from 1.75V to 3.3V in 50mV steps. The VMOT output is specifically designed to drive a vibrator motor. This output can supply up to 150mA at any of the output voltage settings, allowing designers the flexibility to select the output voltage that provides maximum vibration. The VMOT output also has its own external enable, EN_MOT, to allow greater flexibility. When not used in conjunction with a vibrator, this output can be used as a general purpose digital regulator. The VCAM output is capable of supplying up to 100mA to drive a digital camera module or any other peripheral circuit found in a portable application.

Power-On Control

The SC905A is activated when the ON pin is pulled high, provided that the input voltage is within the specified operating range. The ON pin responds to logic-high edge triggering to power up the handset. The rising edge ON signal is latched when the CORE, PAD, ANA, and TCXO LDOs are turned on and PGOOD goes high. When the PAD LDO output voltage reaches 77% of its regulation point, the reset timer starts and the RESB signal transitions high after delay of typically 100ms. After a successful power up sequence, any subsequent condition that toggles RESB (e.g. VPAD short-circuit, over-temperature, under voltage lockout, I^2C disable of VPAD) will see a delay in the RESB transition back to high of typically 250ms. The microprocessor then raises PGOOD high to keep the SC905A powered on. There is no time limit for the MSM to activate PGOOD. If the MSM fails to raise PGOOD before the ON switch is released, the SC905A will transition back into standby mode.

Once the phone is powered on, the SC905A can only be directly powered off when the PGOOD signal goes low. Therefore, if the ON pin transitions high when the PGOOD signal is high, the LDOs and RESB signal will remain in their state until the microprocessor pulls the PGOOD signal low. Once the PGOOD signal is low, all the LDOs immediately power off and all the logic resets to the shutdown condition. The SC905A can be indirectly powered off by using the I^2C command to turn off the core supply. This will result in a loss of power to the MSM causing PGOOD to go low, thus disabling the SC905A.

The HFPWR and CHPWR pins operate identically to the ON pin. These pins provide alternative sources for activating power so that remote devices such as battery chargers or system connector pins can be used to enable the device.

LDO Programmable Output Voltage

The output voltage of each LDO regulator is programmable. Each LDO has a program voltage register that can be accessed through the I^2C interface and the output voltage adjusted as necessary. (See the Tables on pages 14, 15 and 16 for more information.)

ON/OFF Control Register

Each individual LDO may be turned on or off by accessing the ON/OFF control register. LDOs are turned on by setting their respective on/off bits to 1 and disabled by setting the on/off bits to 0. This allows for on/off control with a single write command.

The register data is maintained when an on/off bit is toggled, but all programmed information will be lost when the PGOOD input goes low.

It should be noted that the enable signal control from the I^2C for LDOs TCXO and MOT are OR'd with their respective external enable signals EN_TCXO and EN_MOT. This

Applications Information (Cont.)

means that these LDOs are on when there is a '1' in their respective bit locations (register 6, bit 3 for VTCXO, register 2, bit 6 for VMOT), or if their external enable pins are pulled HIGH. To turn these LDOs off the I²C on/off control bit must be '0' and the external enable must be pulled LOW. The state of EN_TCXO and EN_MOT can be established by reading bits 0 and 2, respectively, in the Status Register.

VCSEL & VPSEL Pin

The VCSEL & VPSEL pins set the default voltage of CORE and PAD LDOs respectively. When the VCSEL pin is set to VIN the default voltage for the CORE LDO is 1.80V. When this pin is set to GND the default voltage for the CORE LDO is 1.35V. Likewise, when the VPSEL pin is set to VIN the default voltage for the PAD LDO is 3.00V. When this pin is set to GND, the default voltage for the PAD LDO is 2.20V.

In both cases the VCSEL and VPSEL pins must be tied to GND or VIN prior to the device being powered on. This voltage cannot change on the fly by switching the pin voltage between VIN or GND once the device is on. The voltage can be changed from its default state after start-up by writing to the appropriate voltage code register.

Active Shutdown

The shutdown control bits determine how the on-chip active shutdown switches behave. Register 7 is the active shutdown control register and is used to control the shutdown behavior. Each LDO has a specific shutdown bit assigned to it. When the active shutdown bit is enabled (set to 1), the output capacitance on the LDO output is discharged by an on-chip FET when the LDO is disabled. When the active shutdown bit is disabled (set to 0), the output capacitance on the LDO output is discharged by the load. The default state for each LDO active shutdown bit is on.

Default Status Bit

In many multi-threaded environments it is necessary to maintain synchronization between the host micro-controller and the target IC. The SC905A has a default status bit (DSB) that will facilitate this task. The DSB can be useful in keeping the MSM and the SC905A synchronized. However, this is only useful if the MSM is powered by an external switching regulator such as Semtech's SC190A switching regulator.

The DSB is bit 7 of register 0, and shares this register space with the PAD voltage control bits. The DSB is only set to 1 during power-up to indicate that the part is set to the default state. Moreover, the DSB cannot be written to a 1 through the I²C interface the way the other bits in this register can; it can only be cleared to 0 through the I²C interface. This feature prevents a software race condition by always writing to register 0 with bit 7 high when changing the PAD control voltage. To clear the bit simply write a 0 to bit 7.

Applying the DSB

Upon power-up, the SC905A LDOs and internal registers are set to their default state. The DSB is set to a 1 to indicate that the SC905A is in its default state. Upon reading this defaulted state condition, the MSM knows to perform whatever synchronization is needed to set the SC905A into a known user state. This user state is entered by a two-stage process.

1) The MSM writes a 0 to the DSB indicating its desire to modify the state of the SC905A. It then writes all of the correct register information to the SC905A to set it to the user state.

2) The MSM reads back all of the information to verify the data. Then it reads back the DSB again to ensure it is still set to 0. This verifies that no reset took place during the time that the multiple writes and read verifications happened. If the DSB has been reset to 1, this process needs to be repeated since the chip was reset sometime during the initialization. Once the MSM and the SC905A are synchronized, the DSB can be read back as a status check periodically, as needed. If it is ever set back to the default state, a new synchronization process is required. This handshake-style protocol makes sure that the MSM and SC905A are always synchronized.

LDO Power-On Sequence

When the SC905A first turns on, the four LDOs that default on are sequenced in the following fashion: 1) CORE, 2) PAD, 3) ANA, 4) TCXO. During the power-on sequence, there is a 200µs delay between CORE and PAD to allow the output of CORE to reach 1.2V before PAD is turned on, a delay of 100µs between PAD and ANA turning on, and a delay of 100µs between ANA and TCXO turning on. This process eliminates large voltage spikes across the battery supply during power-up. (For further information on LDO power on sequencing, refer to the Timing Diagram on page 19.)

Applications Information (Cont.)

Protection Circuitry

The SC905A contains protection circuitry that prevents the device from operating in an unspecified state. These include Under-voltage Lockout Protection, Over-temperature Protection and Short-circuit Protection.

Under-Voltage Lockout

The SC905A provides an under-voltage lockout (UVLO) circuit to protect the device from operating in an unknown state if the input voltage supply is too low.

When the battery voltage drops below the UVLO threshold, as defined in the Electrical Characteristics section, the LDOs are disabled and RESB is held low. When the battery voltage is increased above the hysteresis level, the LDOs are re-enabled into their previous states, provided PGOOD has remained high. If PGOOD goes low, the SC905A will shut down. When powering-up with a battery voltage below the UVLO threshold, RESB will be held low.

Over-Temperature Protection

The SC905A provides an internal over-temperature (OT) protection circuit that monitors the internal junction temperature. When the temperature exceeds the OT threshold as defined in the Electrical Characteristics section, the OT protection disables all the LDO outputs, holds the RESB signal low and sets the OTF bit low in the status register. When the junction temperature drops below the hysteresis level, the OT protection resets the OTF bit high and re-enables all the LDOs in their previous states, provided PGOOD has remained high. If PGOOD goes low, the SC905A will shut down. This is only useful if the MSM is not powered by the SC905A, since during an OT fault the MSM will lose power. An external switching regulator such as Semtech's SC190A could power the MSM in the case where monitoring the OTF bit is desired.

Short-Circuit Protection

Each LDO output has short-circuit protection. If any output is short-circuited to ground, the output voltage will drop and the output current will be limited to the short circuit current until the short is removed.

Status Register

The status register monitors the OTF and the state of the external enable pins dedicated to the TCXO and MOT LDOs. The MSM can periodically poll this register to determine their status. This is a read-only register.

Layout Considerations

The PCB layout associated with the SC905A is straightforward, with the main consideration being given to the value and position of the input bypass capacitors. The device has eight input voltage pins which can be powered from a single supply or from a number of individual supplies depending on how much copper is available on the input voltage feed track and how much real estate is available on the PCB for components.

If all the supply inputs are fed from one single supply trace or from a power plane, a 10µF low ESR capacitor or two 4.7µF low ESR capacitors should be used. Larger input capacitance and lower ESR provide better supply noise rejection and line transient response.

The copper trace to the inputs should be fairly thick in order to keep trace inductance to a minimum and the capacitors should be located as close to the SC905A as possible. If the supply trace is thin then the inputs should be treated as if they were powered from individual supplies; each input should be bypassed by at least one 1µF low ESR capacitor located very close to each input pin.

The SC905A is designed to have excellent stability with a minimum output capacitance of 1µF. Low ESR ceramic capacitors are recommended and should be located as close to the LDO output pins as possible.

POWER MANAGEMENT

Register Map

Register Name	Register Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VPAD	0	DSB[1] 1 / 0 **Default State** / User State	X	X	VPAD 4	VPAD 3	VPAD 2	VPAD 1	VPAD 0
VCORE	1	X	X	X	VCORE4	VCORE3	VCORE2	VCORE1	VCORE0
VMOT	2	VMOT_EN 1 / 0 ON / **OFF**	VMOT Active SHDN 1 / 0 ON / **OFF**	X	VMOT4	VMOT3	VMOT2	VMOT1	VMOT0
VANA/VCAM	3	VANA2	VANA1	VANA0	VCAM4	VCAM3	VCAM2	VCAM1	VCAM0
VTCXO/VRX	4	X	VRX2	VRX1	VRX0	X	VTCXO2	VTCXO1	VTCXO0
VPLL/VTX	5	X	VTX2	VTX1	VTX0	X	VPLL2	VPLL1	VPLL0
ON/OFF CONTROL	6	VPAD_EN 1 / 0 **ON** / OFF	VCORE_EN 1 / 0 **ON** / OFF	VANA_EN 1 / 0 **ON** / OFF	VCAM_EN 1 / 0 ON / **OFF**	VTCXO_EN 1 / 0 **ON** / OFF	VPLL_EN 1 / 0 ON / **OFF**	VTX_EN 1 / 0 ON / **OFF**	VRX_EN 1 / 0 ON / **OFF**
ACTIVE[2] SHUTDOWN	7	VPAD Active SHDN 1 / 0 **ON** / OFF	VCORE Active SHDN 1 / 0 **ON** / OFF	VANA Active SHDN 1 / 0 **ON** / OFF	VCAM Active SHDN 1 / 0 **ON** / OFF	VTCXO Active SHDN 1 / 0 **ON** / OFF	VPLL Active SHDN 1 / 0 **ON** / OFF	VTX Active SHDN 1 / 0 **ON** / OFF	VRX Active SHDN 1 / 0 **ON** / OFF
STATUS (READ ONLY)	8	X	X	X	X	OTF 1 / 0 **OK** / FAULT	EN_MOT 1 / 0 ON / OFF	X	EN_TCXO 1 / 0 ON / OFF

Defaults are indicated in BOLD.

SC905A Slave Address:

DEVICE ADDRESS							R/W
0	0	0	1	0	0	0	**X**

Notes:
(1) The default status bit (DSB) is set to 1 only when the SC905A is enabled by either the HFPWR pin or the ON pin being pulled high, and it cannot be set to one through the I^2C interface. When changing the VPAD control voltage, always write to register 0 with bit seven high. Set bit seven low only when the DSB is to be cleared by the MSM. This will prevent any software race condition in a multi-tasking environment. See the applications section for more information on using the DSB.

(2) The Active Shutdown defaults ON at power-up, but the registers maintain their settings as the LDOs are enabled and disabled during normal operation.

Register Map (Cont.)

Digital LDO Voltage Tables A and B

A 5-bit linear DAC controls the output voltage of each LDO. The DAC and error-amp gain are scaled so that the LSB size at the output is 50mV. Output voltage can be set by writing the proper code to the desired LDO register. See Table A for the bitcodes and their corresponding voltages for LDO CORE, and Table B for bitcodes and their corresponding voltages for LDOs PAD, MOT and CAM.

TABLE A - Output Voltage Code Bits for VCORE

X4	X3	X2	X1	X0	LDO Output Voltage
0	0	0	0	0	1.35V
0	0	0	0	1	1.40V
0	0	0	1	0	1.45V
0	0	0	1	1	1.50V
0	0	1	0	0	1.55V
0	0	1	0	1	1.60V
0	0	1	1	0	1.65V
0	0	1	1	1	1.70V
0	1	0	0	0	1.75V
0	1	0	0	1	1.80V
0	1	0	1	0	1.85V
0	1	0	1	1	1.90V
0	1	1	0	0	1.95V
0	1	1	0	1	2.00V
0	1	1	1	0	2.05V
0	1	1	1	1	2.10V
1	0	0	0	0	2.15V
1	0	0	0	1	2.20V
1	0	0	1	0	2.25V
1	0	0	1	1	2.30V
1	0	1	0	0	2.35V
1	0	1	0	1	2.40V
1	0	1	1	0	2.45V
1	0	1	1	1	2.50V
1	1	0	0	0	2.55V
1	1	0	0	1	2.60V
1	1	0	1	0	2.65V
1	1	0	1	1	2.70V
1	1	1	0	0	2.75V
1	1	1	0	1	2.80V
1	1	1	1	0	2.85V
1	1	1	1	1	2.90V

TABLE B - Output Voltage Code Bits for VPAD, VMOT and VCAM

X4	X3	X2	X1	X0	LDO Output Voltage
0	0	0	0	0	1.75V
0	0	0	0	1	1.80V
0	0	0	1	0	1.85V
0	0	0	1	1	1.90V
0	0	1	0	0	1.95V
0	0	1	0	1	2.00V
0	0	1	1	0	2.05V
0	0	1	1	1	2.10V
0	1	0	0	0	2.15V
0	1	0	0	1	2.20V
0	1	0	1	0	2.25V
0	1	0	1	1	2.30V
0	1	1	0	0	2.35V
0	1	1	0	1	2.40V
0	1	1	1	0	2.45V
0	1	1	1	1	2.50V
1	0	0	0	0	2.55V
1	0	0	0	1	2.60V
1	0	0	1	0	2.65V
1	0	0	1	1	2.70V
1	0	1	0	0	2.75V
1	0	1	0	1	2.80V
1	0	1	1	0	2.85V
1	0	1	1	1	2.90V
1	1	0	0	0	2.95V
1	1	0	0	1	3.00V
1	1	0	1	0	3.05V
1	1	0	1	1	3.10V
1	1	1	0	0	3.15V
1	1	1	0	1	3.20V
1	1	1	1	0	3.25V
1	1	1	1	1	3.30V

Register Map (Cont.)

Analog LDO Voltage Tables C and D

The bit code controls the output voltage of each LDO. The LSB size at the output is 50mV. Output voltage can be set by writing the proper code to the desired LDO register. See Table C for the bitcodes and their corresponding voltages for LDO ANA, and Table D for the bitcodes and their corresponding voltages for LDOs TCXO, TX, RX and PLL.

TABLE C - Output Voltage Code Bits for LDO VANA

X2	X1	X0	LDO Output Voltage
0	0	0	2.55V
0	0	1	2.60V
0	1	0	2.65V
0	1	1	2.70V
1	0	0	2.75V
1	0	1	2.80V
1	1	0	2.85V
1	1	1	2.90V

TABLE D - Output Voltage Code Bits for LDOs VTCXO, VTX, VRX, VPLL

X2	X1	X0	LDO Output Voltage
0	0	0	2.75V
0	0	1	2.80V
0	1	0	2.85V
0	1	1	2.90V
1	0	0	2.95V
1	0	1	3.00V
1	1	0	3.05V
1	1	1	3.10V

Using the I²C Serial Port

The I²C General Specification

The SC905A is a read-write slave-mode I²C device and complies with the Philips I²C standard Version 2.1 dated January, 2000. The SC905A has eight user-accessible internal 8-bit registers. The I²C interface has been designed for program flexibility, in that once the slave address has been sent to the SC905A enabling it to be a slave transmitter/receiver, any register can be written or read independently of each other. While there is no auto increment/decrement capability in the SC905A I²C logic, a tight software loop can be designed to randomly access the next register independent of which register you begin accessing. The start and stop commands frame the data-packet and the repeat start condition is allowed if necessary.

SC905A Limitations to the I²C Specifications

Seven bit addressing is used and ten bit addressing is not allowed. Any general call address will be ignored by the SC905A. The SC905A is not CBUS compatible. The SC905A can operate in standard mode (100kbit/s) or fast mode (400kbit/s).

Supported Formats

Direct Format - Write

The simplest format for an I²C write is given below. After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The SC905A I²C then acknowledges that it is being addressed, and the master responds with an 8-bit data byte consisting of the register address. The slave acknowledges and the master sends the appropriate 8-bit data byte. Once again the slave acknowledges and the master terminates the transfer with the stop condition [P].

I²C Direct Format - Write

S	Slave Address	W	A	Register Address	A	Data	A	P

S: Start Condition
W: Write = '0'
A: Acknowledge (sent by slave)
P: Stop condition

Slave Address: 7-bit
Register Address: 8-bit
Data: 8-bit

Combined Format - Read

After the start condition [S], the slave address is sent, followed by an eighth bit indicating a write. The SC905A I²C then acknowledges that it is being addressed, and the master responds with an 8-bit data byte consisting of the register address. The slave acknowledges and the master sends the repeated start condition [Sr]. Once again, the slave address is sent, followed by an eighth bit indicating a read. The slave responds with an acknowledge and the previously addressed 8-bit data byte; the master then sends a non-acknowledge (NACK). Finally, the master terminates the transfer with the stop condition [P].

I²C Combined Format - Read

S	Slave Address	W	A	Register Address	A	Sr	Slave Address	R	A	Data	NACK	P

S: Start Condition
W: Write = '0'
R: Read = '1'
A: Acknowledge (sent by slave)
NACK: Non-Acknowledge (sent by master)
Sr: Repeated Start Condition
P: Stop condition

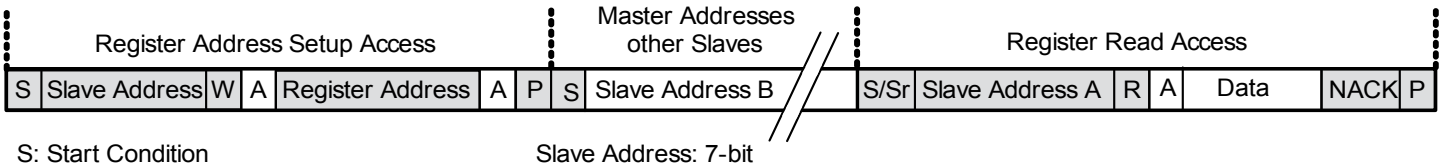
Slave Address: 7-bit
Register Address: 8-bit
Data: 8-bit

Using the I²C Serial Port (Cont.)

Stop-Separated Reads

Stop-separated reads can also be used. This format allows a master to set up the register address pointer for a read and return to that slave at a later time to read the data. In this format the slave address followed by a write command are sent after a start [S] condition. The SC905A then acknowledges it is being addressed, and the master responds with the 8-bit register address. The master sends a stop or restart condition and may then address another slave. After performing other tasks, the master can send a start or restart condition to the SC905A with a read command. The SC905A acknowledges this request and returns the data from the register location that had previously been set up.

I²C Stop Separated Format- Read

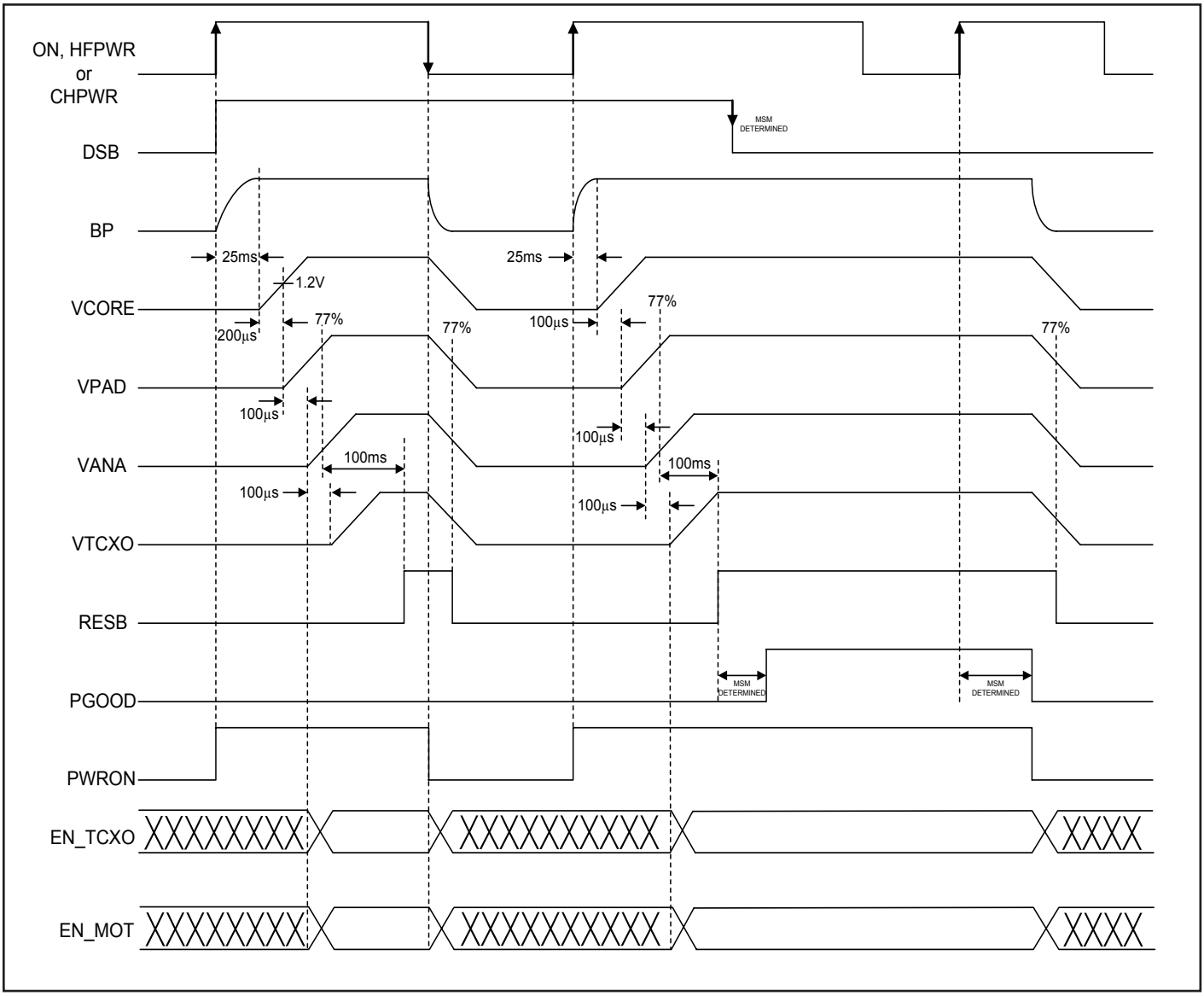


S: Start Condition
W: Write = '0'
R: Read = '1'
A: Acknowledge (sent by slave)
NACK: Non-Acknowledge (sent by master)
Sr: Repeated Start Condition
P: Stop condition

Slave Address: 7-bit
Register Address: 8-bit
Data: 8-bit

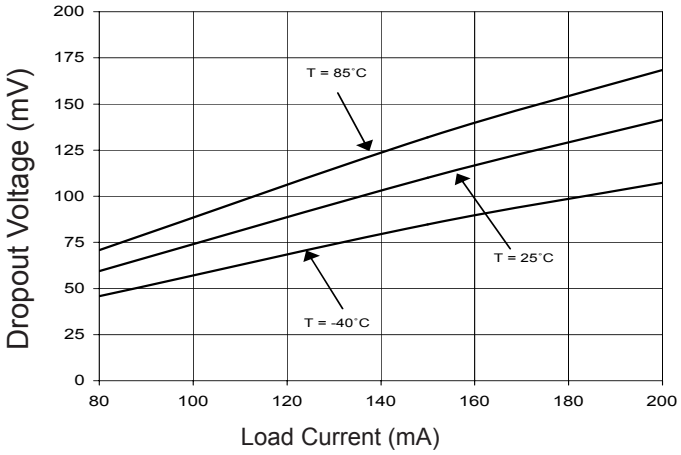
Timing Diagram

Power On-Off Timing Diagram

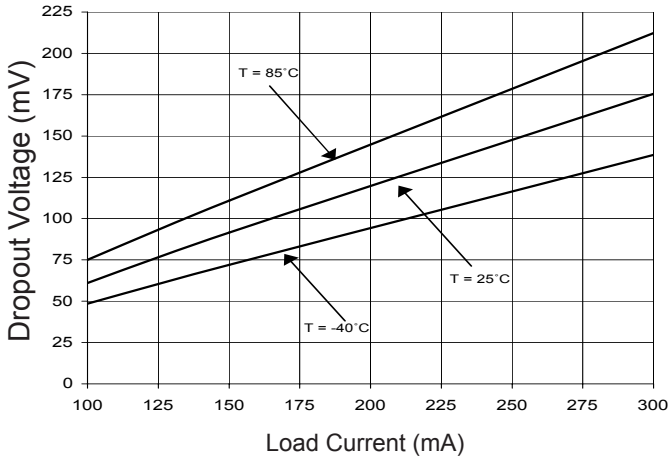


Typical Characteristics

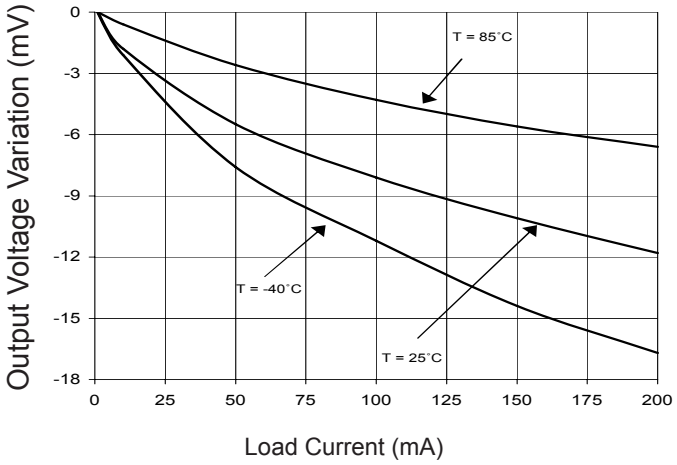
Dropout Voltage vs. Load Current (Analog LDOs)



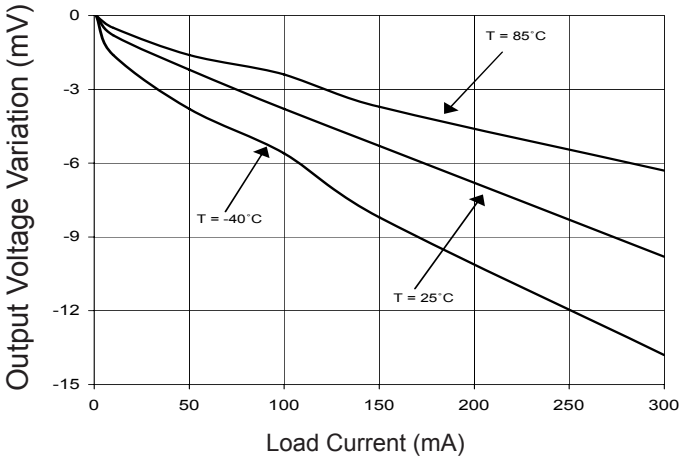
Dropout Voltage vs. Load Current (Digital LDOs)



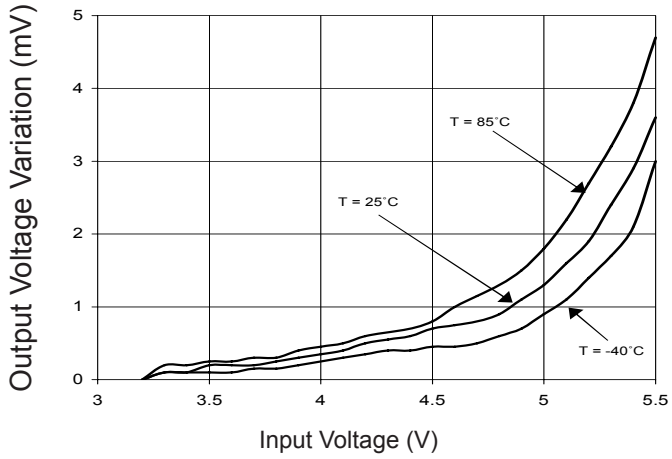
Load Regulation (Analog LDOs) V_{IN} = 3.7V



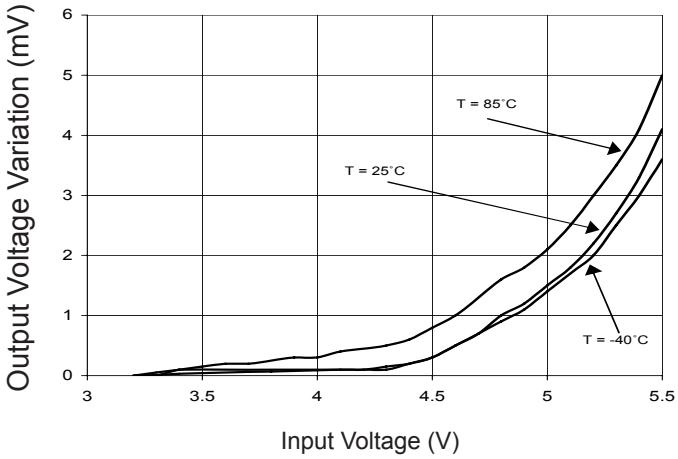
Load Regulation (Digital LDOs) V_{IN} = 3.7V



Line Regulation (Analog LDOs) I_{LOAD} = 1mA

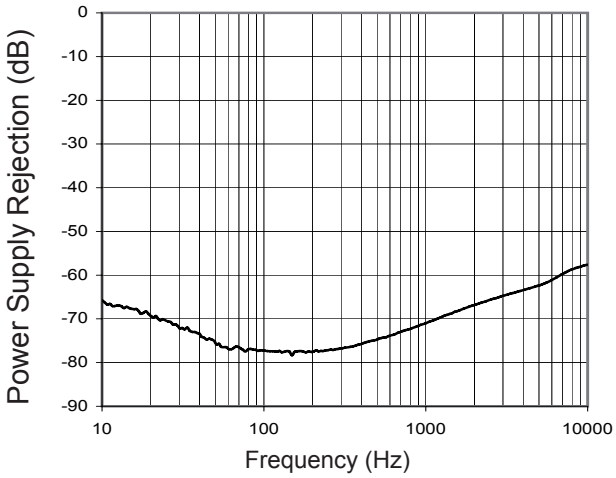


Line Regulation (Digital LDOs) I_{LOAD} = 1mA

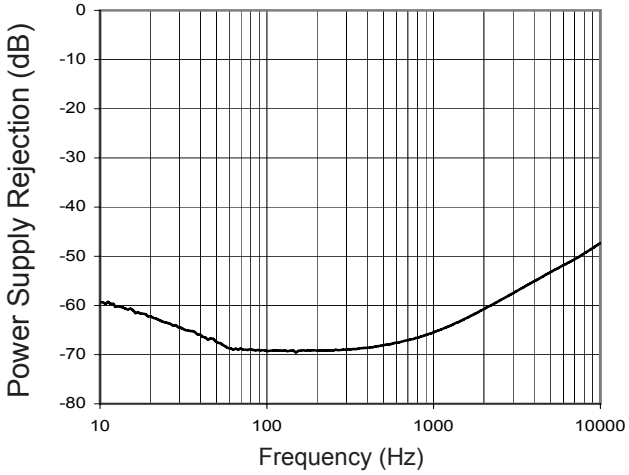


Typical Characteristics (Cont.)

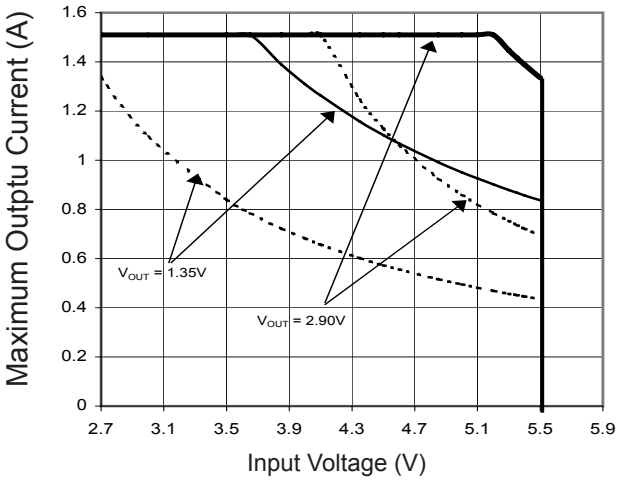
PSRR vs. Frequency (Analog LDOs)
$V_{OUT} = V_{OUT(MAX)}$, V_{IN} = 3.7V, I_{LOAD} = 50mA



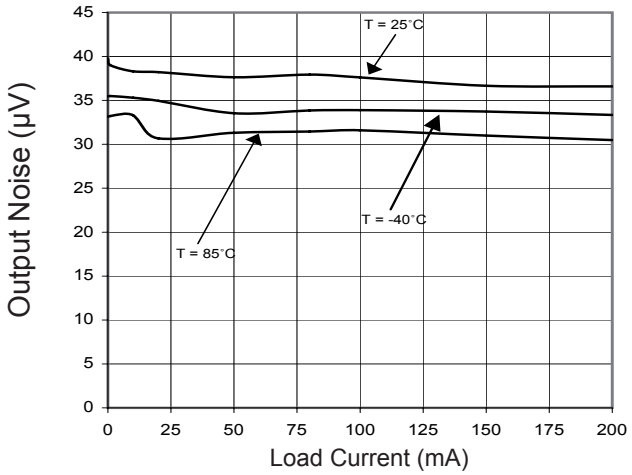
PSRR vs. Frequency (Digital LDOs)
$V_{OUT} = V_{OUT(MAX)}$, V_{IN} = 3.7V, I_{LOAD} = 50mA



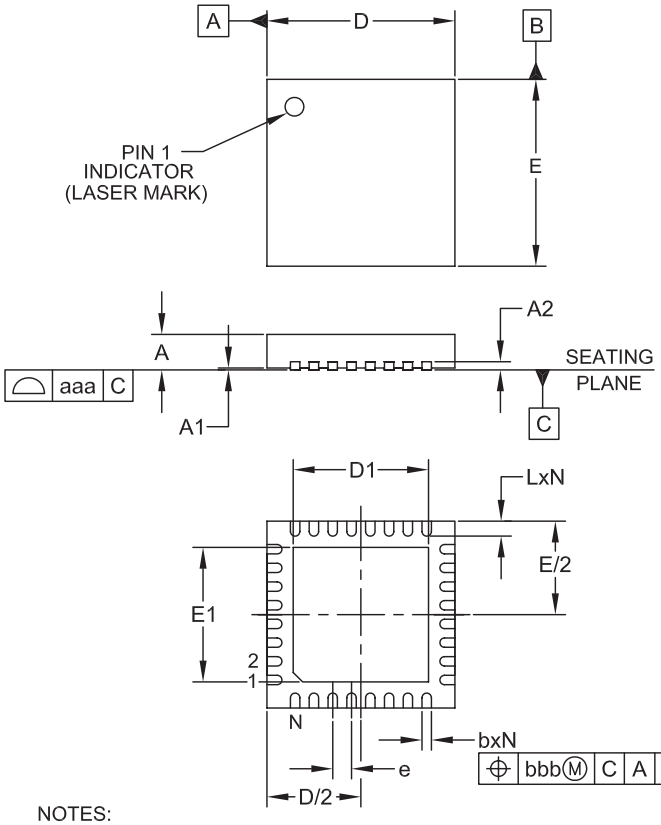
Safe Operating Limits



Output Noise vs. Load Current (Analog LDOs)
$V_{OUT} = V_{OUT(MAX)}$, V_{IN} = 3.7V



Outline Drawing - MLPQ-32 5x5

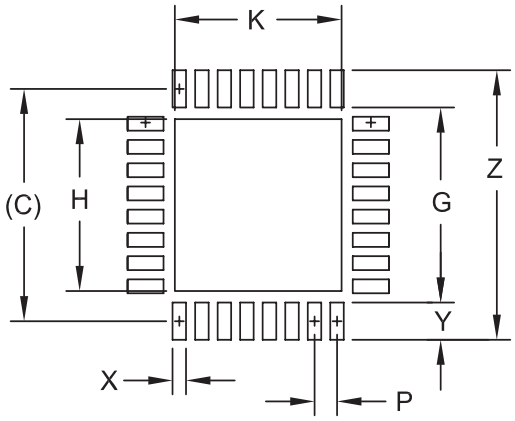


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.031	-	.039	0.80	-	1.00
A1	.000	-	.002	0.00	-	0.05
A2	-	(.008)	-	-	(0.20)	-
b	.007	.010	.012	0.18	0.25	0.30
D	.193	.197	.201	4.90	5.00	5.10
D1	.130	.136	.140	3.30	3.45	3.55
E	.193	.197	.201	4.90	5.00	5.10
E1	.130	.136	.140	3.30	3.45	3.55
e	.020 BSC			0.50 BSC		
L	.012	.016	.020	0.30	0.40	0.50
N	32			32		
aaa	.003			0.08		
bbb	.004			0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Land Pattern - MLPQ-32 5x5



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.197)	(5.00)
G	.165	4.20
H	.146	3.70
K	.146	3.70
P	.020	0.50
X	.012	0.30
Y	.031	0.80
Z	.228	5.80

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY.
   CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR
   COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD
   SHALL BE CONNECTED TO A SYSTEM GROUND PLANE.
   FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR
   FUNCTIONAL PERFORMANCE OF THE DEVICE.
4. SQUARE PACKAGE - DIMENSIONS APPLY IN BOTH " X " AND " Y " DIRECTIONS.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111 FAX (805)498-3804