EcoSpeed® DC-DC Buck Controller with Integrated LDO

POWER MANAGEMENT

Features

- Power system
  - Input voltage — 3V to 28V
  - Integrated bootstrap switch
  - Fixed 5V LDO output — 200mA
  - 1% reference tolerance -40 to +85 °C
  - Selectable internal/external bias power supply
  - EcoSpeed® architecture with pseudo-fixed frequency adaptive on-time control
- Logic input and output control
  - Independent enable controls for LDO and switcher
  - Programmable soft-start time
  - Programmable V_{IN} UVLO threshold
  - Power Good output
  - Selectable power-save mode
- Protections
  - Automatic restart on fault shutdown
  - Over-voltage and under-voltage
  - TC compensated $R_{DS(ON)}$ sensed current limit
  - Thermal shutdown
  - Smart power-save
  - Pre-bias start-up
- Capacitor types: SP, POSCAP, OSCON, and ceramic
- Package — 3 x 3(mm), 20-pin MLPQ
- Lead-free and halogen-free
- RoHS and WEEE compliant

Applications

- Office automation and computing
- Networking and telecommunication equipment
- Point-of-load power supplies and module replacement

Description

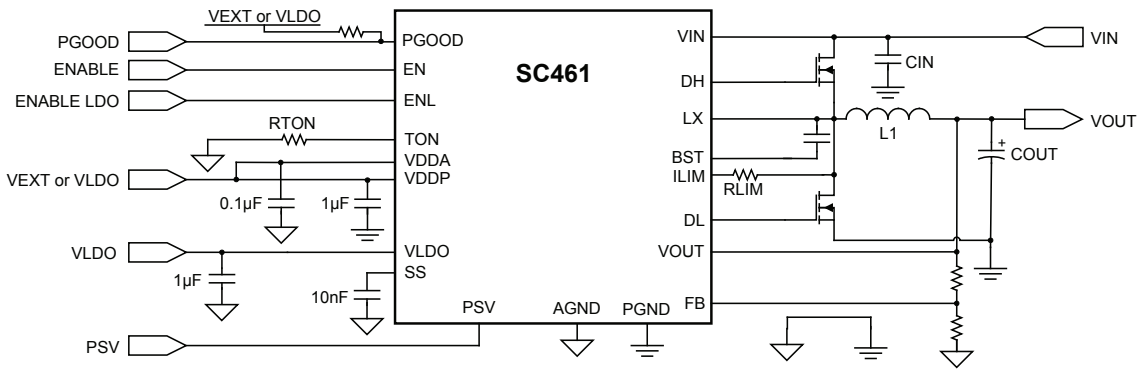
The SC461 is a synchronous EcoSpeed® buck regulator which incorporates Semtech's advanced, patented adaptive on-time control architecture to provide excellent light-load efficiency and fast transient response. It features an integrated bootstrap switch and a fixed 5V LDO in a 3 x 3(mm) package. The device is highly efficient and uses minimal PCB area.

The SC461 supports using standard capacitor types such as electrolytic or special polymer, in addition to ceramic, at switching frequencies up to 1MHz. The programmable frequency, synchronous operation, and programmable power-save provide high efficiency operation over a wide load range.

Additional features include cycle-by-cycle current limit, programmable soft-start, under and over-voltage protection, programmable over-current protection, start-up into pre-biased output, automatic fault recovery (hiccup restart), soft-shutdown, and a selectable power-save mode. The device also provides separate enable inputs for the PWM controller and LDO as well as a Power Good output for the PWM controller. Output voltage range is 0.6 to 5V, with output voltages greater than 5V supported using additional components.

The input voltage can range from 3V to 28V. The wide input voltage range, programmable frequency, and integrated 5V LDO make the device extremely flexible and easy to use in a broad range of applications. Support is provided for multi-cell battery systems in addition to traditional DC power supply applications.

Typical Application Circuit



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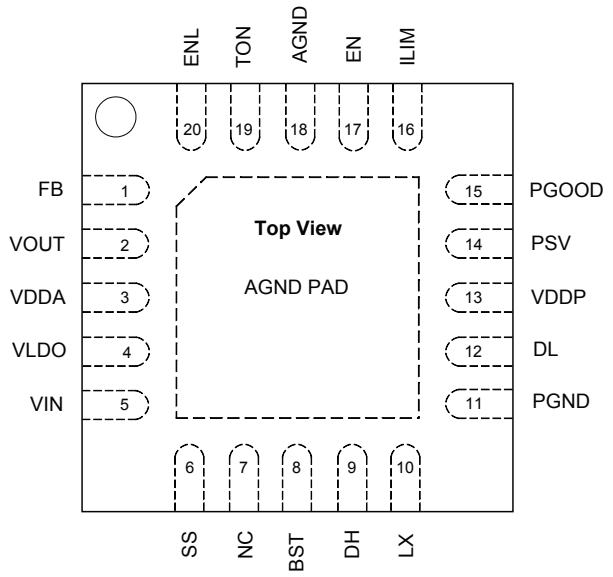
Pin Configuration



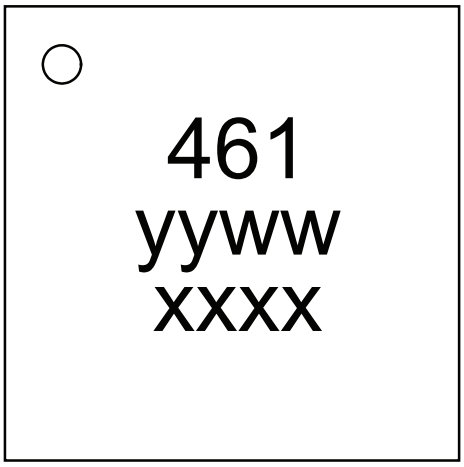
MLPQ-UT20

Ordering Information

Device	Package
SC461ULTRT[1][2]	MLPQ-UT20
SC461EVB	Evaluation Board

Notes:
1) Available in tape and reel only. A reel contains 3000 devices.
2) Lead-free packaging only. Device is WEEE and RoHS compliant and halogen-free.

Marking Information



yyww = Date Code
xxxx = Semtech Lot Number

Absolute Maximum Ratings[1]

LX to PGND (V) ..... -0.3 to +28
LX to PGND (V) (transient — 100ns) ..... -2.0 to +28
DH, BST to PGND (V) ..... -0.3 to +35
DH, BST to LX (V) ..... -0.3 to +6
DL to PGND (V) ..... -0.3 to +6
VIN to PGND (V) ..... -0.3 to +30
EN, FB, ILIM, PGOOD to AGND (V) ... -0.3 to +(VDDA + 0.3)
PSV, SS, TON to AGND (V) ..... -0.3 to +(VDDA + 0.3)
VLDO, VOUT to AGND (V) ..... -0.3 to +(VDDA + 0.3)
TON to AGND (V) ..... -0.3 to +(VDDA -1.5)
ENL to AGND (V) ..... -0.3 to VIN
VDDP to PGND, VDDA to AGND (V) ..... -0.3 to +6
VDDA to VDDP (V) ..... -0.3 to +0.3
AGND to PGND (V) ..... -0.3 to +0.3
ESD Protection Level[1] (kV) 2

Recommended Operating Conditions

Input Voltage (V) ..... 3.0 to 28
VDDA to AGND, VDDP to PGND (V) ..... 3.0 to 5.5
VOUT to PGND (V)[2] ..... 0.6 to 5.5
Supports output voltages greater than 5.5V using external components

Thermal Information

Storage Temperature (°C) ..... -60 to +150
Maximum Junction Temperature (°C) 150
Operating Junction Temperature (°C) ..... -40 to +125
Thermal resistance, junction to ambient[3] (°C/W) 50
Peak IR Reflow Temperature (°C) 260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) Tested according to JEDEC standard JESD22-A114.
(2) VOUT pin must not exceed (VDDA + 0.3V).
(3) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless specified: V_{IN} =12V, VDDA = VDDP = 5V, T_A = +25°C for Typ, -40 to +85 °C for Min and Max, T_J < 125°C, Typical Application Circuit

Parameter	Conditions	Min	Typ	Max	Units
Input Supplies					
Input Supply Voltage (V_{IN})	VDDA = 5V	3		28	V
V_{IN} UVLO Threshold[1]	Sensed at ENL pin, rising edge	1.46	1.55	1.64	V
	Sensed at ENL pin, falling edge.	1.14	1.24	1.34	
V_{IN} UVLO Hysteresis	Sensed at ENL pin; EN = 5V		0.31		V
VDDA UVLO Threshold	Measured at VDDA pin, rising edge	2.75	2.84	2.92	V
	Measured at VDDA pin, falling edge	2.45	2.62	2.84	
VDDA UVLO Hysteresis			0.22		V
V_{IN} Supply Current	Shutdown mode; ENL, EN = 0V, V_{IN} = 28V		18	25	µA
	Standby mode; VDDA, VDDP, ENL = 5V, EN = 0V		130		

SEMTECH

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Input Supplies (continued)					
VDDA + VDDP Supply Current[2]	ENL , EN = 0V		3	7	µA
	Power-save operation EN = 5V, PSV = open (float), V_{FB} > 600mV		0.4		mA
	Forced Continuous Mode operation Operating f_{SW} = 220kHz, PSV = VDDA, no load		14		
FB Comparator Threshold	Static V_{IN} and load, 0 to +85 °C	0.5952	0.600	0.6048	V
	Static V_{IN} and load, -40 to +85 °C	0.594		0.606	V
Frequency Range	Continuous mode operation			1000	kHz
Timing					
On-Time	Forced Continuous Mode operation V_{IN} = 15V, V_{OUT} = 3V, R_{TON} = 300kΩ, VDDA = 5V	1530	1700	1870	ns
Minimum On-Time			80		ns
Minimum Off-Time			250		ns
Soft-Start					
Soft-Start Charge Current			3.0		µA
Analog Inputs/Outputs					
VOUT Input Resistance			500		kΩ
Current Sense					
Zero Cross Detector Threshold	LX with respect to PGND	-3	0	+3	mV
Power Good					
Power Good Threshold	Upper limit, V_{FB} > internal 600mV reference		+20		%
	Lower limit, V_{FB} < internal 600mV reference		-9		
Startup Delay Time	EN rising edge to PGOOD rising edge, CSS = 10nF, VDDA = 5V		12.5		ms
	EN rising edge to PGOOD rising edge, CSS = 10nF, VDDA = 3V		7.5		
Fault (noise immunity) Delay Time			5		µs
Leakage	PGOOD = high impedance (open)			1	µA
Power Good On-Resistance	PGOOD = pulled low to AGND		9		Ω

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Fault Protection					
I_{LIM} Source Current	Temperature 25°C	9	10	11	µA
I_{LIM} Source Current Temperature Coefficient			0.28		%/°C
I_{LIM} Comparator Offset	With respect to AGND	-8	0	+8	mV
Output Under-Voltage Threshold	V_{FB} with respect to internal 600mV reference, 8 consecutive cycles		-25		%
Smart Power-Save Protection Threshold	V_{FB} with respect to internal 600mV reference		+10		%
Over-Voltage Protection Threshold	V_{FB} with respect to internal 600mV reference		+20		%
Over-Voltage Fault Delay			5		µs
Over-Temperature Shutdown	10°C hysteresis		165		°C
Logic Inputs/Outputs					
Logic Input High Voltage — EN		1.4			V
Logic Input High Voltage — PSV	Forced Continuous Mode operation; PSV pin with respect to VDDA	-0.4			V
Logic Input Low Voltage — EN, ENL[3]	With respect to AGND			0.4	V
EN Input Bias Current	EN = VDDA or AGND	-10		+10	µA
ENL Input Bias Current	V_{IN} = 28V		+11		µA
FB Input Bias Current	FB = VDDA or AGND	-1		+1	µA
PSV Input Bias Current	PSV = VDDA		5	16	µA
	0.8V ≤ PSV ≤ 1.5V		1		µA
Linear Regulator					
VLDO Accuracy	VLDO load = 10mA	4.875	5.0	5.125	V
Current Limit	VLDO < 1V (typ) start-up		15		mA
	1V < VLDO < 4.0V (typ)		96		
	Operating, VLDO > 4.0V (typ)		200		
VLDO Drop Out Voltage	V_{IN} to VLDO, LDO load = 50mA		1.4		V

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
High-Side Driver (DH, BST, LX)					
Peak Current	VDDP = 5V, DH pin sourcing or sinking		2		A
On Resistance	$R_{DH_PULL\text{-}UP,}$ LX < 0.5V, VDDP = 5V		3.6	5	Ω
	$R_{DH_PULL\text{-}UP,}$ LX > 0.5V, VDDP = 5V		1.1	2.1	Ω
	$R_{DH_PULL\text{-}DOWN,}$ VDDP = 5V		0.65	1.20	Ω
Rise Time	$C_{DH\text{-}LX}$ = 3nF, VDDP = 5V		22		ns
Fall Time	$C_{DH\text{-}LX}$ = 3nF, VDDP = 5V		12		ns
Propagation Delay	From FB Input to DH		45		ns
Shoot-thru Protection Delay	VDDP = 5V		45		ns
Bootstrap Switch Resistance	VDDP = 5V		16		Ω
Low-Side Driver (DL, VDDP, PGND)					
Peak Current	VDDP = 5V, DL sourcing		2		A
	VDDP = 5V, DL sinking		4		A
On Resistance	$R_{DL_PULL\text{-}UP,}$ VDDP = 5V		0.85	1.60	Ω
	$R_{DL_PULL\text{-}DOWN,}$ VDDP = 5V		0.28	0.50	Ω
Rise Time	C_{DL} = 3nF, VDDP = 5V		7		ns
Fall Time	C_{DL} = 3nF, VDDP = 5V		3.5		ns

Notes:

(1) V_{IN} UVLO is programmable using a resistor divider from VIN to ENL to AGND. The ENL voltage is compared to an internal reference. Note that because the V_{IN} UVLO threshold at the ENL pin is above the enable threshold of the LDO, the LDO must be used as bias power for the device when using the V_{IN} UVLO feature.

(2) For FCM operation, the VDDA and VDDA supply current includes the DH/DL current required to drive the external MOSFETs.

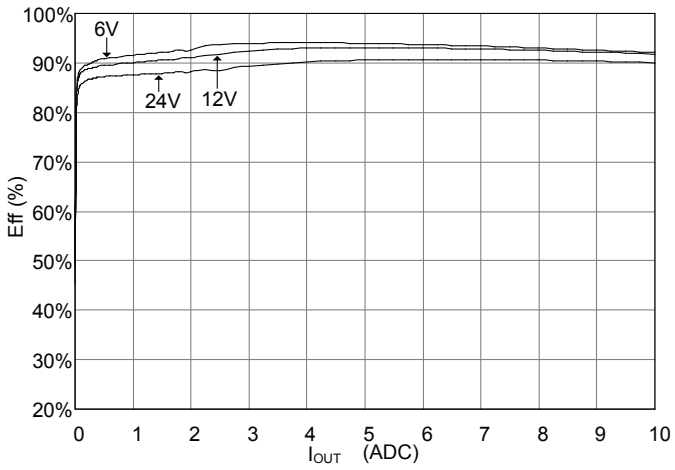
(3) The ENL pin will enable the LDO with 0.8V typical. The V_{IN} ULVO function of the ENL pin will disable the switcher unless the ENL pin exceeds the V_{IN} UVLO Threshold which is typically 1.55V.

Typical Characteristics

Characteristics in this section are based on using the Detailed Application Circuit.

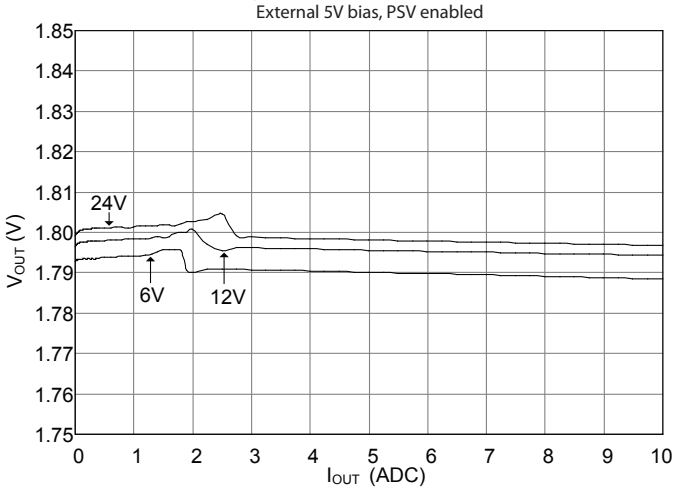
Efficiency vs. Load — Power Save Mode

External 5V bias, PSV enabled



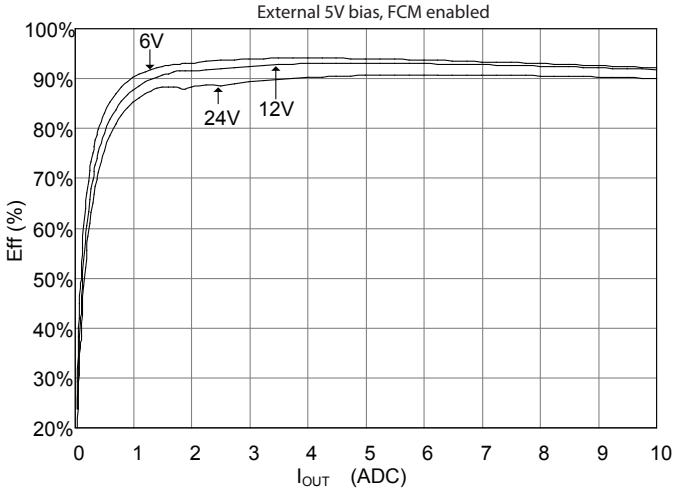
Load Regulation — Power Save Mode

External 5V bias, PSV enabled



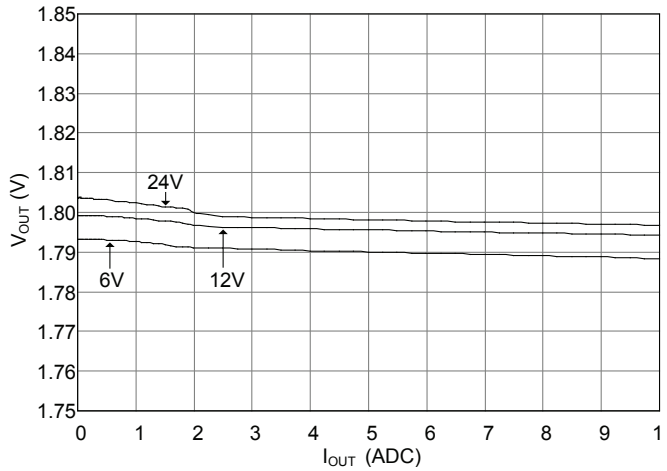
Efficiency vs. Load — Forced Continuous Mode

External 5V bias, FCM enabled



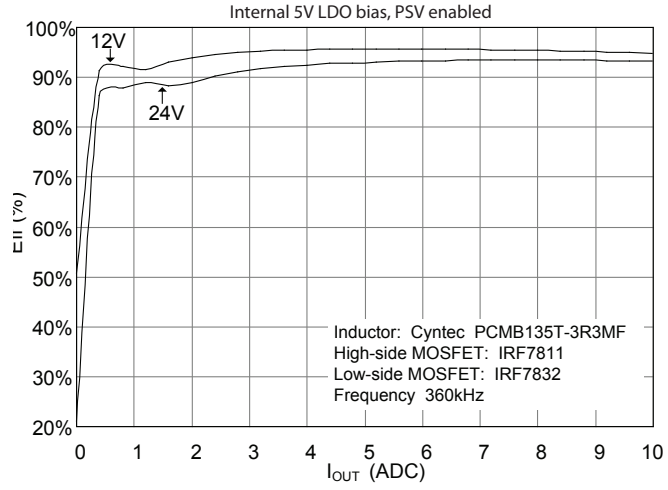
Load Regulation — Forced Continuous Mode

External 5V bias, FCM enabled



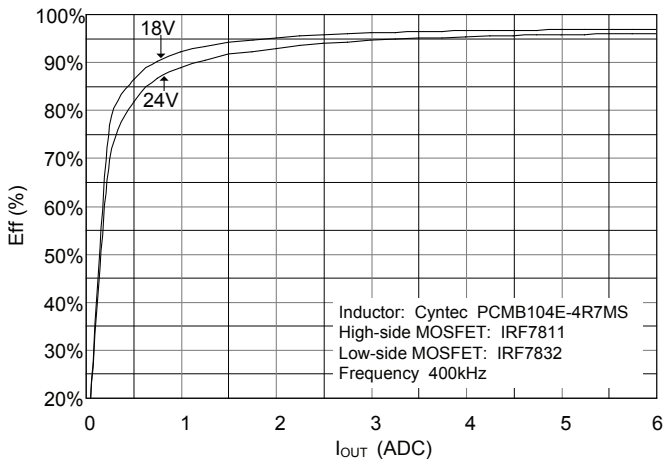
Efficiency vs Load - 5V output

Internal 5V LDO bias, PSV enabled



Efficiency vs Load - 12V output

Internal 5V LDO bias, FCM enabled

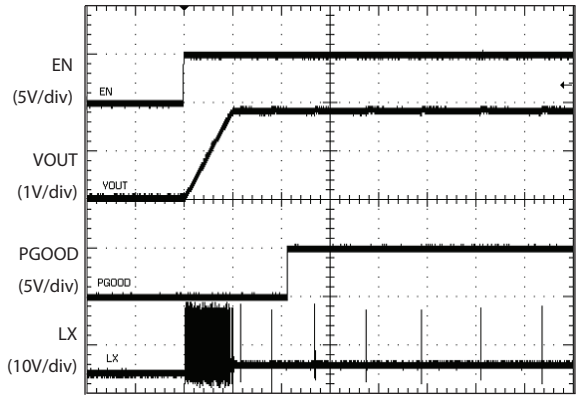


Typical Characteristics (continued)

Characteristics in this section are based on using the Detailed Application Circuit.

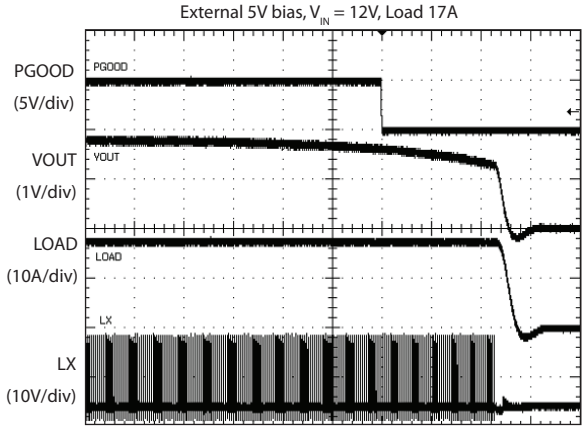
Start-up — EN Input

External 5V bias, V_{IN} = 12V, no load, PSV enabled



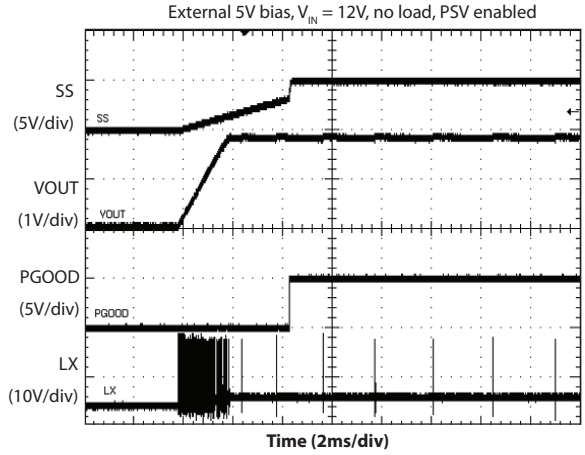
Over-current Response

External 5V bias, V_{IN} = 12V, Load 17A



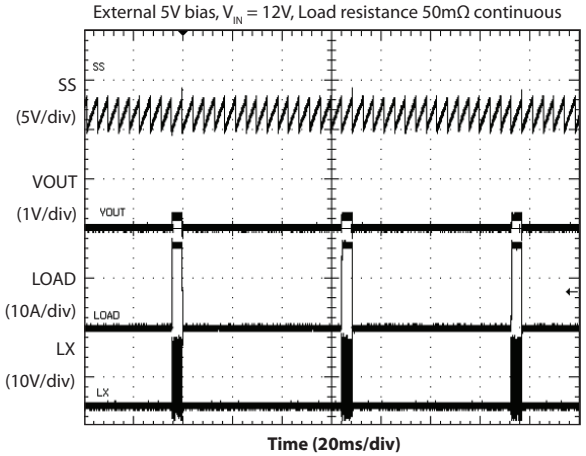
Start-up — SS ramp-up

External 5V bias, V_{IN} = 12V, no load, PSV enabled



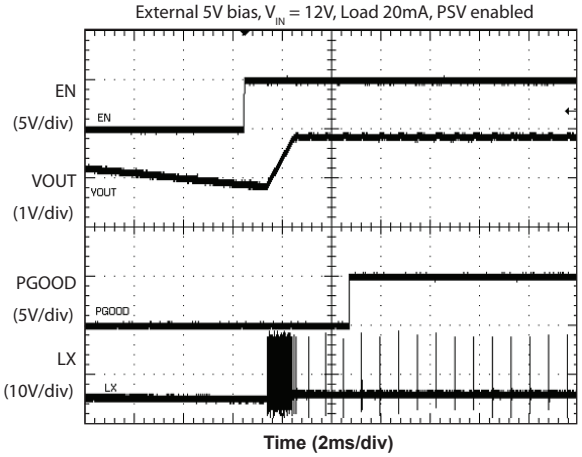
Automatic Restart — Over-current

External 5V bias, V_{IN} = 12V, Load resistance 50mΩ continuous



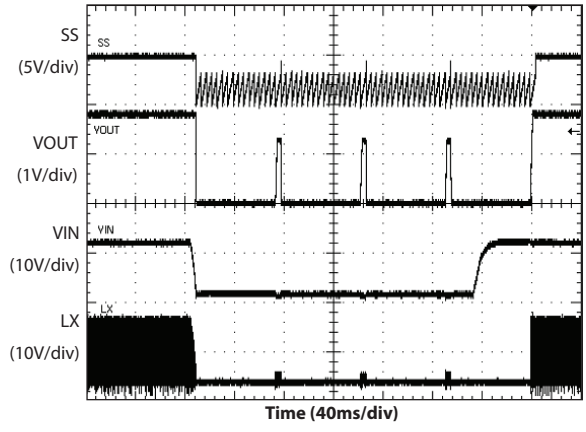
Startup into Pre-bias Output

External 5V bias, V_{IN} = 12V, Load 20mA, PSV enabled



Automatic Restart — V_{IN} transient

External 5V bias, V_{IN} = 12V, Load 1A

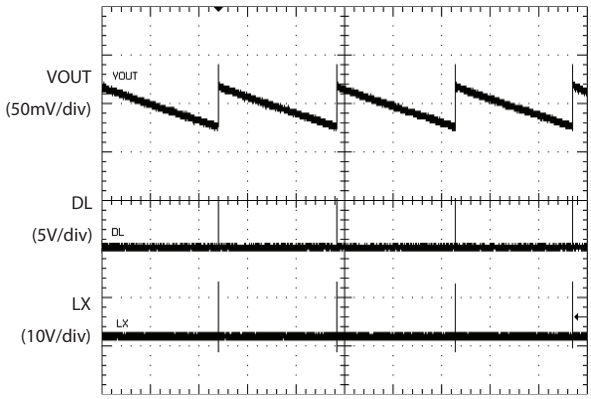


Typical Characteristics (continued)

Characteristics in this section are based on using the Detailed Application Circuit.

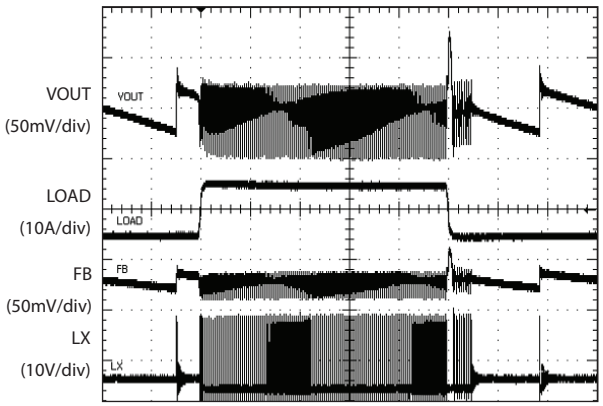
Switching — Power-Save Mode, No Load

External 5V bias, V_{IN} = 12V, no load, PSV enabled



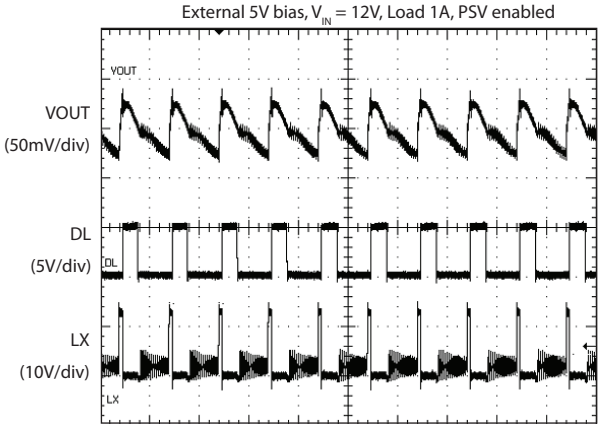
Transient Response — Power-Save Mode

External 5V bias, V_{IN} = 12V, V_{OUT} = 1.8V, Load 0A to 10A, PSV enabled



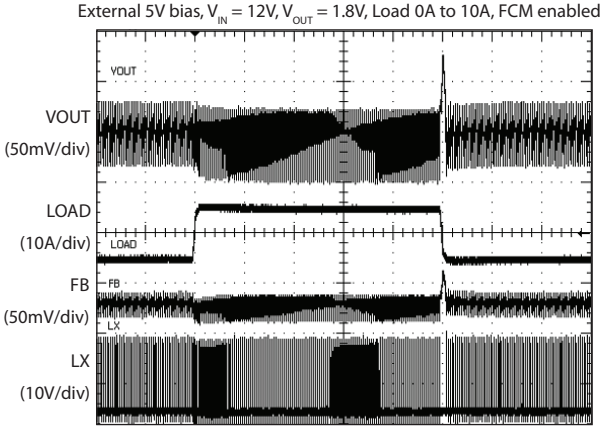
Switching — Power-Save Mode, Light Load

External 5V bias, V_{IN} = 12V, Load 1A, PSV enabled



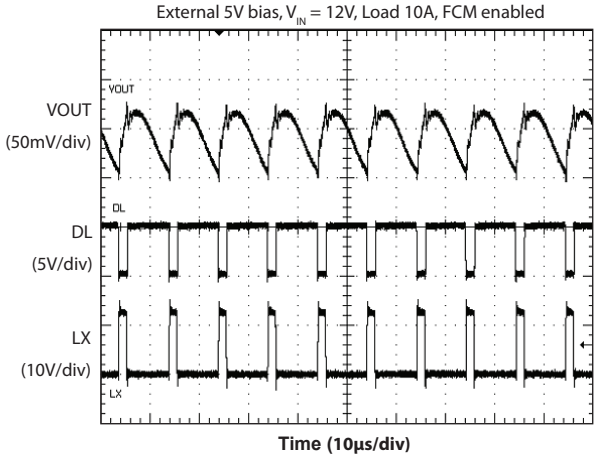
Transient Response — Forced Continuous Mode

External 5V bias, V_{IN} = 12V, V_{OUT} = 1.8V, Load 0A to 10A, FCM enabled



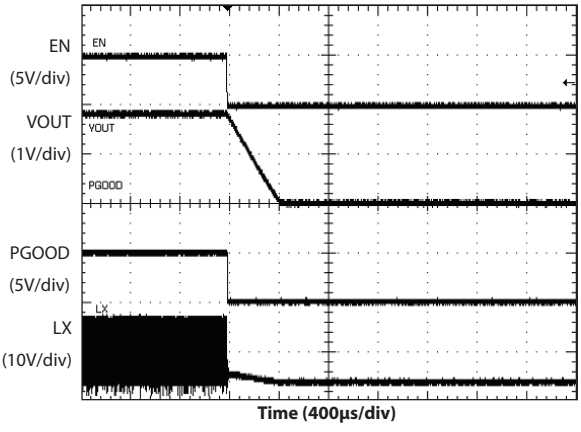
Switching — Forced Continuous Mode

External 5V bias, V_{IN} = 12V, Load 10A, FCM enabled

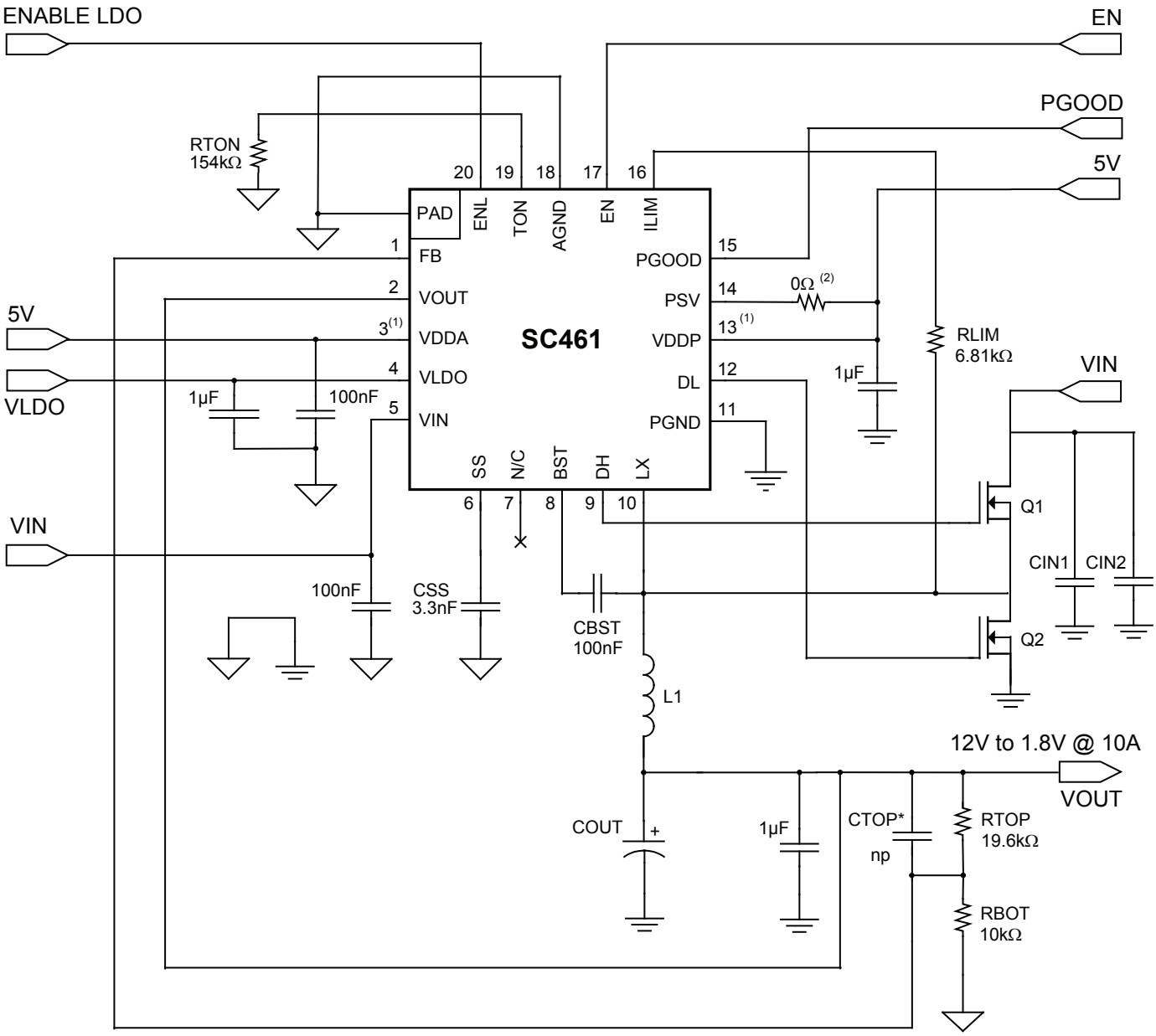


Output Shutdown

External 5V bias, V_{IN} = 12V, V_{OUT} = 1.8V, Load 1A



Detailed Application Circuit



Key Components

Component	Value	Manufacturer	Part Number	Web
CIN1, CIN2	10µF/25V	Murata	GRM32DR71E106KA12L	www.murata.com
COUT	2x220µF/15mΩ/4V	Sanyo	4TPE220MF	edc.sanyo.com
L1	1.5µH	Cyntec	PCMB1335T-1R5MF	www.cyntec.com
Q1	IRF7821	I.R.	IRF7821	www.irf.com
Q2	IRF7832	I.R.	IRF7832	www.irf.com

Notes:

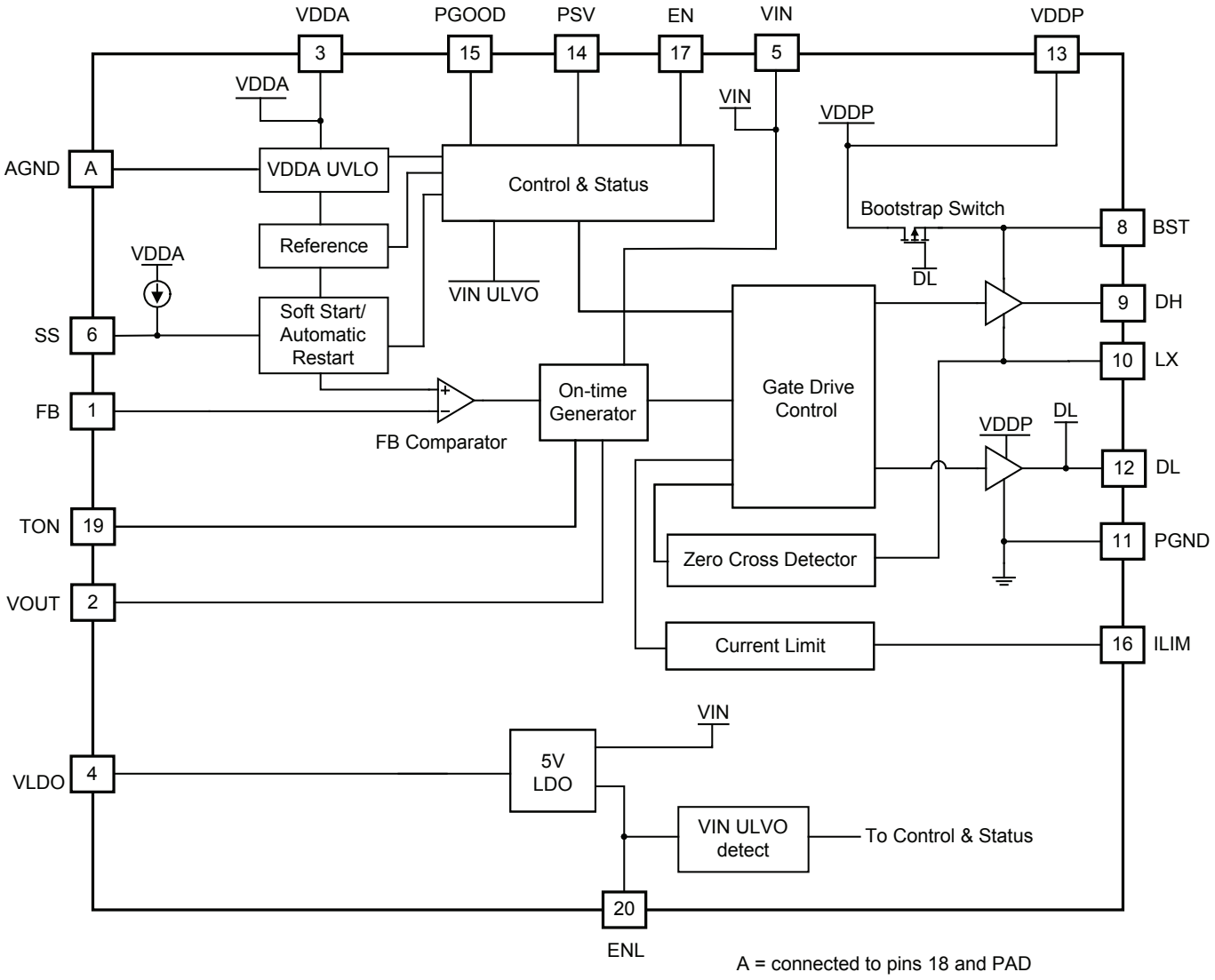
(1) 5V: Connect VDDA and VDDP to external 5V supply for external bias.
Connect VDDA and VDDP to VLDO for self-biased operation.

(2) PSV: Remove 0Ω resistor for Power-Save operation.
Connect 0Ω resistor from PSV pin to VDDA for Forced Continuous Mode operation.

Pin Descriptions

Pin #	Pin Name	Pin Function
1	FB	Feedback input for switching regulator — connect to an external resistor divider from output — used to program the output voltage.
2	VOUT	Switcher output voltage sense pin. The voltage at this pin must not exceed the VDDA pin. For output voltages up to VDDA connect this pin directly to the switcher output. For output voltages exceeding 5V connect this pin to the switcher output through a resistor divider.
3	VDDA	Supply input for internal analog circuits — connect to an external 3.3V or 5V supply or connect to VLDO — also the sense input for VDDA Under Voltage Lockout (VDDA UVLO).
4	VLDO	Output of the 5V LDO — The voltage at this pin must not exceed the voltage at the VDDA pin.
5	VIN	Input supply voltage — connect to the same supply used for the high-side MOSFET. Connect a 100nF capacitor from this pin to AGND to filter high frequency noise.
6	SS	Soft-Start — connect an external capacitor to AGND to program the soft-start and automatic recovery time.
7	NC	No Connection
8	BST	Bootstrap pin — connect a 100nF minimum capacitor from BST to LX to develop the floating voltage for the high-side gate drive.
9	DH	High-side gate drive output
10	LX	Switching (phase) node
11	PGND	Power ground for the DL and DH drivers and the low-side external MOSFET.
12	DL	Low-side gate drive output
13	VDDP	Supply input for the DH and DL gate drives — connect to the same 3.3V or 5V supply used for VDDA.
14	PSV	Power-save programming input — float pin to select power-save with no minimum frequency — pull up to VDDA to disable power-save and select forced continuous mode.
15	PGOOD	Open-drain Power Good indicator — high impedance indicates the switching regulator output is good. An external pull-up resistor is required.
16	ILIM	Current limit sense pin — used to program the current limit by connecting a resistor from ILIM to LX.
17	EN	Enable input for switching regulator — logic low disables the switching regulator — logic high enables the switching regulator.
18	AGND	Analog ground
19	TON	ON time programming input — set the on-time by connecting through a resistor to AGND.
20	ENL	Enable input for the LDO and VIN UVLO input for the switching regulator — connect ENL to AGND to disable the LDO — drive to logic high (>1.7V) to enable the LDO and inhibit V_{IN} UVLO — connect to resistor divider from VIN to AGND to program the V_{IN} UVLO threshold.
PAD	AGND	Analog ground

Block Diagram



Applications Information

Synchronous Buck Converter

The SC461 is a step down synchronous DC-DC buck controller with an internal 5V LDO. It provides efficient operation in a space saving 3x3 (mm) 20-pin package. The programmable operating frequency range up to 1MHz enables optimizing the configuration for PCB area and efficiency.

The controller uses a pseudo-fixed frequency adaptive on-time control. This allows fast transient response which permits the use of smaller output capacitors.

Input Voltage Requirements

The SC461 requires two input supplies for normal operation: V_{IN} and VDDA/VDDP. V_{IN} operates over the wide range of 3V to 28V. VDDA and VDDP require a 3.3V or 5V supply which can be from an external source or from the internal LDO. VDDA and VDDP must be derived from the same source voltage.

Psuedo-fixed Frequency Adaptive On-time Control

The PWM control method used by the SC461 is pseudo-fixed frequency, adaptive on-time, as shown in Figure 1. The ripple voltage generated at the output capacitor ESR is used as a PWM ramp signal. This ripple is used to trigger the on-time of the controller.

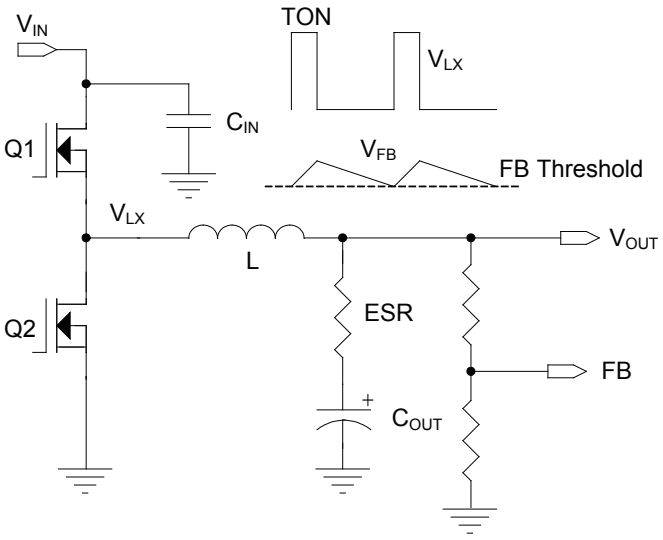


Figure 1 — PWM Control Method, V_{OUT} Ripple

The adaptive on-time is determined by an internal one-shot timer. When the one-shot is triggered by the output ripple, the device sends a single on-time pulse to the high-side MOSFET. The pulse duration is determined by V_{OUT} and V_{IN}. The duration is proportional to output voltage and inversely proportional to input voltage. With this adaptive on-time configuration, the device automatically anticipates the on-time needed to regulate V_{OUT} for the present V_{IN} condition and at the selected frequency.

The advantages of adaptive on-time control are:

- Predictable operating frequency compared to other variable frequency methods.
- Reduced component count by eliminating the error amplifier and compensation components.
- Reduced component count by removing the need to sense and control inductor current.
- Fast transient response — the response time is controlled by a fast comparator instead of a typically slow error amplifier.
- Reduced output capacitance due to fast transient response.

One-Shot Timer and Operating Frequency

One-shot timer operation is shown in Figure 2. The FB comparator output goes high when V_{FB} is less than the internal 600mV reference. This feeds into the DH gate drive and turns on the high-side MOSFET, and also starts the one-shot timer. The one-shot timer uses an internal comparator and a capacitor. One comparator input is connected to V_{OUT}, the other input is connected to the capacitor. When the on-time begins, the capacitor charges from zero volts through a current which is proportional to V_{IN}. When the capacitor voltage reaches V_{OUT}, the on-time is completed and the high-side MOSFET turns off.

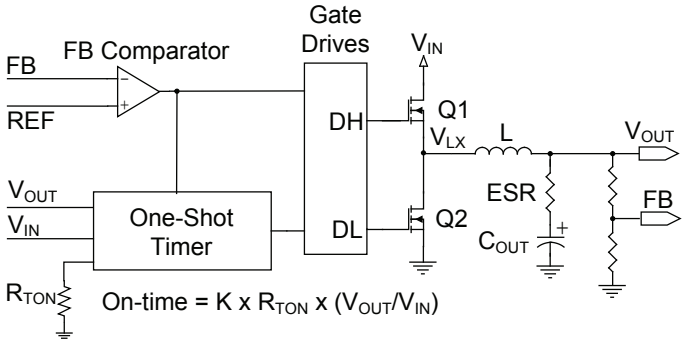


Figure 2 — On-Time Generation

Applications Information (continued)

This method automatically produces an on-time that is proportional to V_{OUT} and inversely proportional to V_{IN}. Under steady-state conditions, the switching frequency can be determined from the on-time by the following equation.

$$f_{SW} = \frac{V_{OUT}}{T_{ON} \times V_{IN}}$$

The SC461 uses an external resistor to set the on-time which indirectly sets the frequency. The on-time can be programmed to provide an operating frequency of up to 1MHz using a resistor between the TON pin and ground. The resistor value is selected by the following equation.

$$R_{TON} = \frac{(T_{ON} - 10ns) \times V_{IN}}{28.2pF \times V_{OUT}} = \frac{\left(\frac{V_{OUT}}{V_{IN} \times f_{SW}} - 10ns\right) \times V_{IN}}{28.2pF \times V_{OUT}}$$

The maximum recommended R_{TON} value is shown by the following equation.

$$R_{TON_MAX} = \frac{V_{IN_MIN}}{20 \times 1.5\mu A}$$

Immediately after the on-time, the DL output drives high to energize the low-side MOSFET. DL has a minimum high time of ~250ns, after which DL continues to stay high until one of the following occurs:

- The FB input falls below the 600mV reference
- The Zero Cross Detector trips if power-save is active

TON Limitations and VDDA Supply Voltage

For VDDA below 4.5V, the TON accuracy may be limited by V_{IN}. The previous RTON equation is accurate if V_{IN} satisfies the below relation over the entire V_{IN} range:

V_{IN} < (VDDA - 1.6V) x 10

If V_{IN} exceeds ((VDDA - 1.6V) x 10) for all or part of the V_{IN} range, the previous RTON equation is not accurate. In all cases where VIN > ((VDDA - 1.6V) x 10), the RTON equation must be modified as follows.

$$R_{TON} = \frac{(T_{ON} - 10ns) \times (VDDA - 1.6V) \times 10}{28.2pF \times V_{OUT}}$$

Note that when V_{IN} is greater than ((VDDA - 1.6V) x 10), the actual on-time is fixed and does not vary with V_{IN}. When operating in this condition, the switching frequency will vary inversely with V_{IN} rather than approximating fixed frequency.

V_{OUT} Voltage Selection

The switcher output voltage is regulated by comparing V_{OUT} as seen through a resistor divider at the FB pin to the internal 600mV reference voltage (see Figure 3).

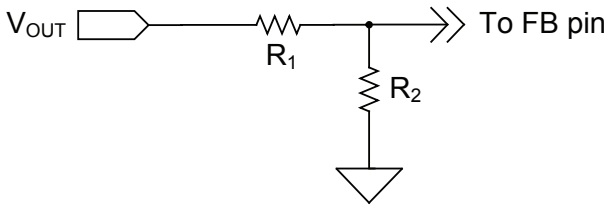


Figure 3 — Output Voltage Selection

Note that this control method regulates the valley of the output ripple voltage, not the DC value. The DC value of V_{OUT} is offset by the output ripple according to the following equation.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{V_{RIPPLE}}{2}\right)$$

In some applications a small capacitor C_{TOP} is placed in parallel with R1 to provide a larger ripple signal from V_{OUT} to the FB pin. In these applications, the output voltage V_{OUT} is calculated according to the following equation in which ω represents the switching frequency.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{V_{RIPPLE}}{2}\right) \times \sqrt{\frac{1 + (R_1 \omega C_{TOP})^2}{1 + \left(\frac{R_2 \times R_1}{R_2 + R_1} \omega C_{TOP}\right)^2}}$$

Configuring V_{OUT} Greater Than 5V

The switcher output voltage can be programmed higher than 5V with careful attention to the VOUT and RTON pins. In these applications the VOUT pin cannot connect directly

Applications Information (continued)

to the switcher output due to its maximum voltage rating. An additional resistor divider network is required to connect from the switcher output to the VOUT pin as shown in Figure 4.

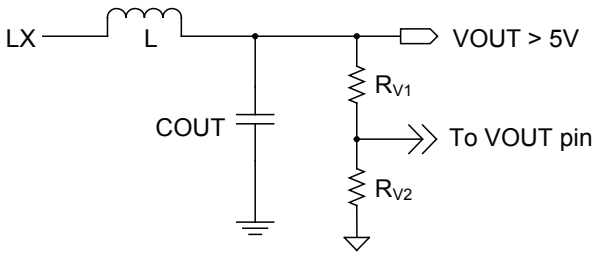


Figure 4 — Resistor Divider For V_{OUT} Exceeding 5V

The resistors must be chosen so that the VOUT does not exceed the VDDA supply. Note that the VOUT pin has an internal 500kΩ resistor connected to AGND. To minimize the effect of this resistor on the resistor divider ratio, the maximum recommend value for resistor R_{V2} in Figure 4 is 10kΩ.

In addition to the resistor divider, the RTON resistor value must be adjusted. The on-time is calculated according to the voltage at the VOUT pin. In order to select the desired on-time and operating frequency, the RTON resistor should be adjusted to a higher value to compensate for the reduced voltage at the VOUT pin. For output voltages exceeding 5V, the required RTON value can be determined by the following equation.

$$R_{TON} = \frac{\left(\frac{V_{OUT}}{V_{IN} \times f_{SW}} - 10ns\right) \times V_{IN}}{28.2pF \times V_{OUT}} \times \left(1 + \frac{R_{V1}}{R_{V2}}\right)$$

For applications where V_{OUT} exceeds 5V, FCM operation is recommended.

Forced Continuous Mode Operation

The SC461 operates the switcher in Forced Continuous Mode (FCM) by connecting the PSV pin to VDDA. The PSV pin should never exceed the VDDA supply. See Figure 5 for FCM waveforms. In this mode one of the power MOSFETs is always on, with no intentional dead time other than to avoid cross-conduction. This results in more uniform frequency across the full load range, with the trade-off being reduced efficiency at light loads due to the high-frequency switching of the MOSFETs.

The PSV pin contains a 5µA current sink to prevent stray leakage current from pulling the PSV pin up to the VDDA supply when the PSV pin is floated to select Power-Save operation. To select Forced Continuous Mode operation, the maximum recommended resistance between the VDDA supply and the PSV pin is 40kΩ.

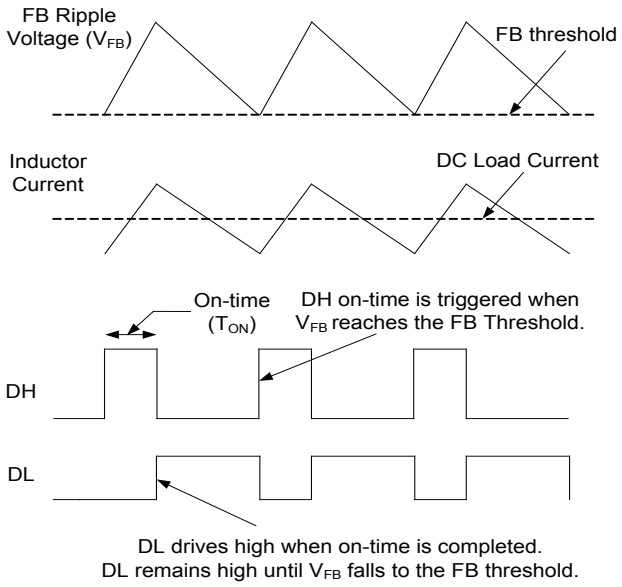


Figure 5 — Forced Continuous Mode Operation

Power-Save Mode Operation

The SC461 provides power-save operation at light loads with no minimum operating frequency, selected by floating the PSV pin (no connection). In this mode of operation, the zero cross comparator monitors inductor current via the voltage across the low-side MOSFET during the off-time. If the inductor current falls to zero for 8 consecutive switching cycles, the controller enters power-save operation. It will then turn off the low-side MOSFET on each subsequent cycle, provided that the current falls to zero. After the low-side MOSFET is off, both high-side and low-sides MOSFETs remain off until V_{FB} drops to the 600mV threshold. While the MOSFETs are off the load is supplied

Applications Information (continued)

by the output capacitor. If the inductor current does not reach zero on any switching cycle, the controller immediately exits power-save and returns to forced continuous mode. Figure 6 shows power-save operation at light loads.

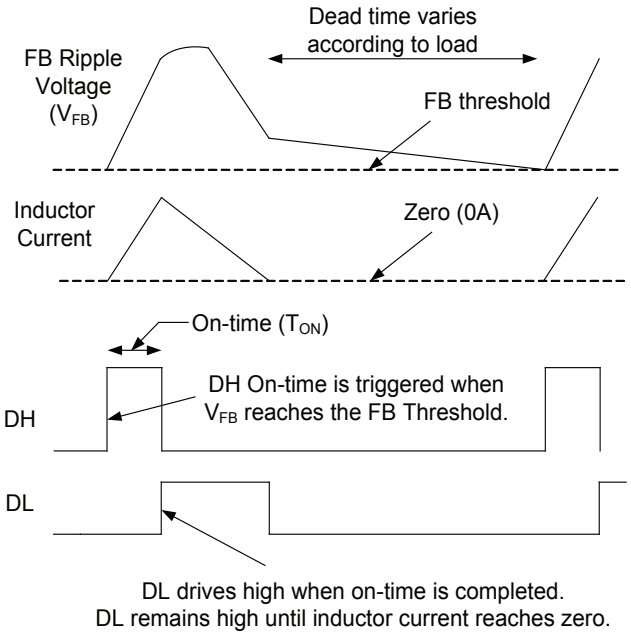


Figure 6 — Power-Save Operation

Smart Power-Save Protection

Active loads may leak current from a higher voltage into the switcher output. Under light load conditions with power-save enabled, this can force V_{OUT} to slowly rise and reach the over-voltage threshold, resulting in an over-voltage shutdown. Smart power-save prevents this condition. When the FB voltage exceeds 10% above nominal (exceeds 660mV), the device immediately disables power-save and DL drives high to turn on the low-side MOSFET. This draws current from V_{OUT} through the inductor and causes V_{OUT} to fall. When V_{FB} drops back to the 600mV trip point, a normal T_{ON} switching cycle begins. This method prevents over-voltage shutdown by cycling energy from V_{OUT} back to V_{IN}. It also minimizes operating power under light load conditions by avoiding forced continuous mode operation.

Figure 7 shows typical waveforms for the Smart Power-save feature.

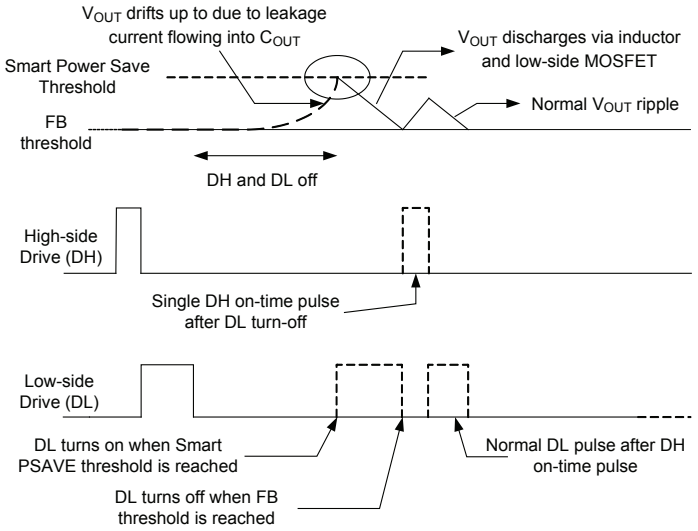


Figure 7 — Smart Power-Save

SmartDrive™

For each DH pulse, the DH driver initially turns on the high-side MOSFET at a slower speed, allowing a softer, smooth turn-off of the low-side diode. Once the diode is off and the LX voltage has risen 0.8V above PGND, the SmartDrive circuit automatically drives the high-side MOSFET on at a rapid rate. This technique reduces switching noise while maintaining high efficiency, reducing the need for snubbers.

Enable Input for Switching Regulator

The EN input is a logic level input. When EN is low (grounded), the switching regulator is off and in its lowest power state. When EN is low and VDDA is above the VDDA UVLO threshold, the output of the switching regulator soft-discharges into the VOUT pin through an internal 2kΩ resistor. When EN is a logic high (≥1V) the switching regulator is enabled.

The EN input has internal resistors — 2MΩ pullup to VDDA, and a 1MΩ pulldown to AGND. These resistors will normally cause the EN voltage to be near the logic high trip point as VDDA reaches the VDDA UVLO threshold. To prevent undesired toggling of EN and erratic start-up performance, the EN pin should not be allowed to float as open-circuit.

Applications Information (continued)

Note that the LDO enable pin (ENL) can also disable the switching regulator through the V_{IN} UVLO function. Refer to the ENL Pin and V_{IN} UVLO section.

Current Limit Protection

The SC461 features programmable current limiting, which is accomplished using the $RDS_{(ON)}$ of the lower MOSFET for current sensing. The current limit is set by R_{LIM} resistor which connects from the ILIM pin to the drain of the low-side MOSFET. When the low-side MOSFET is on, an internal 10µA current flows from the ILIM pin and through the R_{LIM} resistor, creating a voltage drop across the resistor. While the low-side MOSFET is on, the inductor current flows through it and creates a voltage across the $RDS_{(ON)}$. The voltage across the MOSFET is negative with respect to PGND. If this MOSFET voltage drop exceeds the voltage across R_{LIM}, the voltage at the ILIM pin will be negative and current limit will activate. The current limit then keeps the low-side MOSFET on and prevents another high-side on-time, until the current in the low-side MOSFET reduces enough to bring the ILIM pin voltage up to zero. This method regulates the inductor valley current at the level shown by I_{LIM} in Figure 8.

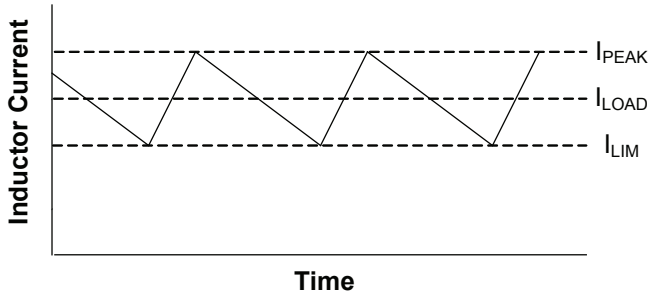


Figure 8 — Valley Current Limit

The current limit schematic with the R_{LIM} resistor is shown in Figure 9.

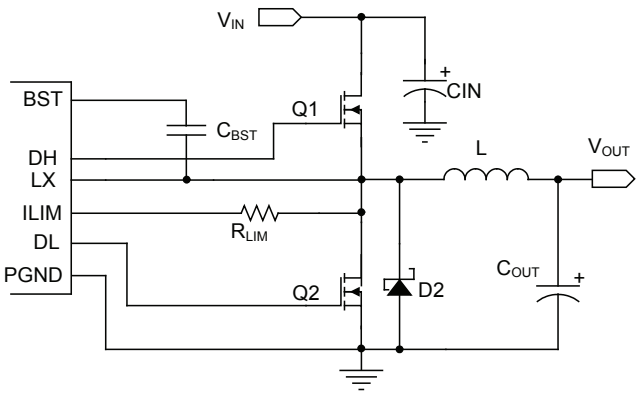


Figure 9 — Valley Current Limit

Setting the valley current limit to 10A results in a peak inductor current of 10A plus peak ripple current. In this situation the average current through the inductor is 10A plus one-half the peak-to-peak ripple current.

The R_{LIM} value is calculated by the next equation.

$$R_{LIM} = \frac{RDS_{ON} \times I_{LIM}}{10\mu A}$$

The internal 10µA current source is temperature compensated at 2800 ppm in order to provide tracking with the RDS_{ON}.

Soft-Start of PWM Regulator

The SC461 has a programmable soft-start time that is controlled by an external capacitor at the SS pin. During the soft-start time, the controller sources 3µA from the SS pin to charge the capacitor. During the start-up process (Figure 10), 40% of the voltage ramp at the SS pin is used as the reference for the FB comparator. The PWM comparator issues an on-time pulse when the FB voltage is less than 40% of the SS voltage, which forces the output voltage to follow the SS ramp. The output voltage reaches regulation when the SS pin voltage exceeds 1.5V and the FB reaches the 600mV threshold. The time between the first LX pulse and VOUT reaching the regulation point is the soft-start time (t_{SS}). The calculation for the soft-start time is shown by the following equation.

Applications Information (continued)

$$t_{SS} = \frac{C_{SS} \times 1.5V}{3\mu A}$$

After the SS capacitor voltage reaches 1.5V, the SS capacitor continues to charge until the SS voltage is equal to 67% of VDDA. At this time the Power Good monitor compares the FB pin and sets the PGOOD output high (open drain) if VOUT is in regulation. The time between VOUT reaching the regulation point and the PGOOD output going high is shown by the following equation.

$$t_{PGOOD} = \frac{C_{SS}}{3\mu A} \times \left(\frac{2 \times VDDA}{3} - 1.5V \right)$$

The time from the rising edge of the EN pin to the PGOOD output going high is shown by the following equation.

$$t_{EN_PGOOD} = \frac{C_{SS}}{3\mu A} \times \left(\frac{2 \times VDDA}{3} \right)$$

After the Power Good Start-up Delay Time is completed, the SS pin is internally pulled up to the VDDA supply.

The soft-start cycle and Power Good timing can be seen in the Figure 10.

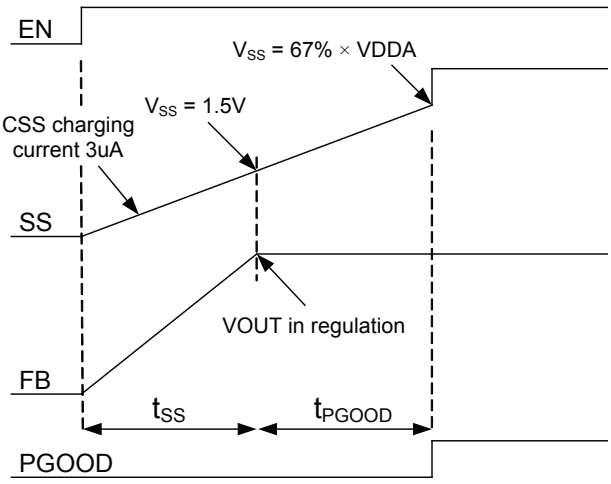


Figure 10 — Soft-start Cycle and Power Good timing

Pre-Bias Start-up

SC461 can support soft-start with an output pre-bias. The SS capacitor ramp time is the same as a normal start-up when the output voltage starts from zero. Under a pre-bias start-up, the DH and DL drivers inhibit switching until 40% of the ramp at the SS pin equals the pre-bias FB voltage level. Pre-bias start-up is achieved by turning off the lower MOSFET when the inductor current reaches zero during the soft-start cycle. This method helps prevent the output voltage from decreasing.

Power Good Output

The PGOOD (power good) output is an open-drain output which requires a pull-up resistor. During start-up, PGOOD is held low and is not allowed to transition high until the output voltage is in regulation and the SS pin has reached 67% of VDDA. The time from EN going high to PGOOD going high is typically 12.5ms for CSS = 10nF and VDDA = 5V. For CSS = 10nF and VDDA = 3V the typical PGOOD time is 7.5ms.

When the voltage at the FB pin is 10% below the nominal voltage, PGOOD is pulled low. Once PGOOD pulls low there is typically 2% hysteresis to prevent chatter on the PGOOD output.

PGOOD will transition low if the FB voltage exceeds +20% of nominal (720mV), which is also the over-voltage shutdown threshold. PGOOD also pulls low if the EN pin is low and VDDA is present.

Output Over-Voltage Protection

Over-voltage protection (OVP) becomes active as soon as the device is enabled. The OVP threshold is set at 600mV + 20% (720mV). There is a 5µs delay built into the OVP detector to prevent false transitions. When V_{FB} exceeds the OVP threshold, DL is driven high and the low-side MOSFET is turned on. DL remains high and the controller remains off. If the FB pin remains above the OVP threshold, DL remains high and the IC will maintain this maintain this state with no automatic recovery. If FB falls below the OVP threshold, the device goes through the automatic fault recovery cycle. When the automatic recovery cycle is completed, the device will attempt a new soft-start cycle. At the start of the soft-start cycle, the DL output will go low for typically 30us while the controller initializes the

Applications Information (continued)

soft-start sequence. PGOOD is also low after an OVP event.

Output Under-Voltage Protection

When V_{FB} falls 25% below its nominal voltage (falls to 450mV) for eight consecutive clock cycles, the switcher is shut off and the DH and DL drives are pulled low to tri-state the MOSFETs. The controller stays off while the device goes through the automatic fault recovery cycle.

Automatic Fault Recovery

The SC461 includes an automatic recovery feature (hiccup mode upon fault). If the switcher output is shut down due to a fault condition, the device uses the SS capacitor as a timer. Upon fault detection the SS pin is pulled low and then begins charging through the internal 3µA current source. When the SS capacitor reaches 67% of VDDA, the SS pin is again pulled low, after which the SS capacitor begins another charging cycle. The SS capacitor will be used for 15 cycles of charging from 0 to 67% of VDDA. (For Over-voltage and Over-Temperature faults, the count will be 16 cycles instead of 15). During these cycles the switcher is off and there is no MOSFET switching.

During the next charging cycle, the normal soft-start routine is implemented and the MOSFETs begin switching. Switching continues until the Power Good Start-up Delay Time is reached. If the switcher output is still in a fault condition, the switcher will again shut down and force 15 cycles of SS charging (16 cycles in the case of an Over-voltage or Over-Temperature fault) before attempting another soft-start. The long delay between soft-start cycles reduces the average power loss in the power components.

The automatic recovery timing is shown in Figure 11.

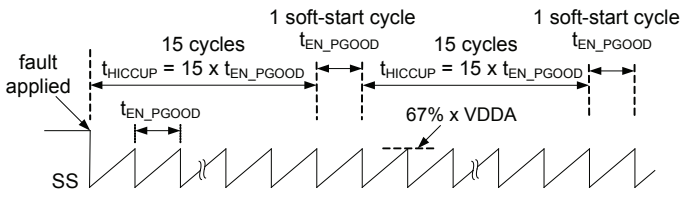


Figure 11 — Automatic Recovery Timing

The control of the low-side MOSFET during an Over-voltage fault is handled differently from other faults. If the fault was due to an over-voltage condition, the DL output will remain high during 16 SS charging cycles. For all other faults, the DL output will remain low. However, if the FB pin exceeds the Over-voltage threshold, the charging of the SS capacitor will not occur, and the DL output will remain high. If the FB pin falls below the OVP threshold, 16 SS charging cycles will occur while DL remains high. When the next start-up cycle commences, DL will drive low for typically 30us as the controller re-initializes the internal soft-start routine.

VDDA UVLO and POR

The VDDA Under-Voltage Lock-Out (UVLO) circuitry inhibits switching and tri-states the DH/DL drivers until VDDA rises above 2.84V. When VDDA exceeds 2.84V, an internal POR (Power-On Reset) resets the fault latch and the soft-start circuitry and then the SC461 is ready to begin a soft-start cycle. The switcher will shut off if VDDA falls below 2.62V. VDDP does not have UVLO protection.

LDO Regulator

When the LDO is providing bias power to the device, a minimum 0.1µF capacitor referenced to AGND is required, along with a minimum 1µF capacitor referenced to PGND to filter the gate drive pulses. Refer to the PCB Layout Guidelines section.

ENL Pin and V_{IN} UVLO

The ENL pin is also used for the V_{IN} under-voltage lockout (V_{IN} UVLO) for the switcher. The V_{IN} UVLO voltage is programmable via a resistor divider at the V_{IN}, ENL and AGND pins. The V_{IN} UVLO function has a typical threshold of 1.55V on the V_{IN} rising edge. The falling edge threshold is 1.24V.

Note that when the V_{IN} UVLO feature is used, the LDO is enabled because the ENL pin is above the LDO enable threshold (0.8V typical). In these cases the SC461 must use the internal LDO for bias power.

Timing is important when driving ENL with logic and not using the V_{IN} UVLO capability. The ENL pin must transition from high to low within 2 switching cycles to avoid the PWM output turning off. If ENL goes below the V_{IN} UVLO

Applications Information (continued)

threshold and stays above 1V, then the switcher will turn off but the LDO will remain on.

Note that it is possible to operate the switcher with the LDO disabled, but the ENL pin must be below the logic low threshold (0.4V maximum), otherwise the V_{IN} UVLO function will disable the switcher.

The next table summarizes the function of the ENL and EN pins.

EN	ENL	LDO status	Switcher status
low	low, < 0.4V	off	off
high	low, < 0.4V	off	on
low	high, < 1.24V	on	off
high	high, < 1.24V	on	off
low	high, > 1.55V	on	off
high	high, > 1.55V	on	on

Figure 12 shows the ENL voltage thresholds and their effect on LDO and Switcher operation.

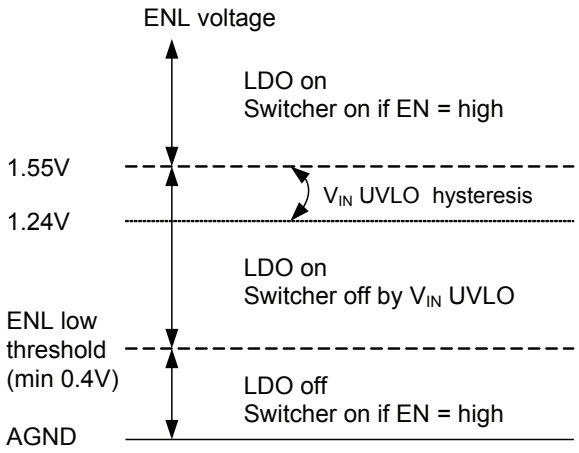


Figure 12 — ENL Thresholds

ENL Logic Control of PWM Operation

When the ENL input exceeds the V_{IN} UVLO threshold of 1.55V, internal logic checks the PGOOD signal. If PGOOD is high, the switcher is already running and the LDO will start without affecting the switcher. If PGOOD is low, the device disables PWM switching until the LDO output has reached 80% of its final value. This delay prevents the additional current needed by the DH and DL gate drives from overloading the LDO at start-up.

LDO Start-up

Before LDO start-up, the device checks the status of the following signals to ensure proper operation can be maintained.

1. ENL pin
2. VLDO output
3. V_{IN} input voltage

When the ENL pin is high and V_{IN} voltage is available, the LDO will begin start-up. During the initial phase when V_{LDO} is below 1V, the LDO initiates a current-limited start-up (typically 15mA). This protects the LDO from thermal damage if the VLDO pin is shorted to ground. As V_{LDO} exceeds 1V, the start-up current gradually increases to 96mA. When V_{LDO} reaches 4V, the LDO current limit increases to 200mA and the LDO output rises quickly to 5V. The LDO start-up profile is shown in Figure 13.

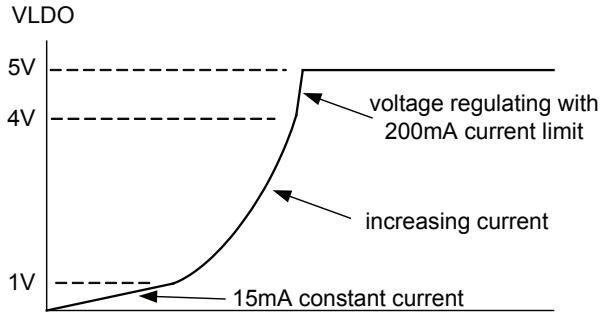


Figure 13 — LDO Start-Up

Using the Internal LDO to Bias the SC461

The following steps must be followed when using the internal LDO to bias the device.

- Connect VDDA and VDDP to VLDO before enabling the LDO.
- During the initial start-up the LDO, when the LDO output is less than 1V, the external load should not exceed 10mA. Above 1V, any external load on VLDO should not exceed 40mA until the LDO voltage has reached 4V.

Applications Information (continued)

When the LDO is used as bias power for the device, the EN and ENL inputs must be used carefully. Do not connect the EN pin directly to VDDA or another supply voltage. If this is done, driving the ENL pin low (to AGND) will turn off the LDO and the LDO switch-over MOSFET, but the switcher can continue operating. If V_{OUT} exceeds 2.5V, the output voltage can feed into the VDDA supplies through internal parasitic diodes via the VOUT pin. This can potentially damage the device, and also can prevent the switcher from shutting off until the VDDA supply drops below the VDDA UVLO threshold. For these applications a dedicated logic signal is required to drive EN low and disable the switcher. This signal can be combined with the ENL signal if needed, as long as the EN pin does not exceed Absolute Maximum Ratings.

LDO Usage at Low Input Voltage

Applications requiring steady-state or transient operation at low input voltages (V_{IN} below 6.5V) may use the internal LDO to bias the VDDA/VDDP pins within limitations. There are limitations to both startup and normal operation as explained below.

When starting up using the internal LDO, switcher operation is inhibited until the LDO output reaches 4V. During this time, the LDO start-up is implemented using a current source. At low V_{IN} it is important to not apply an external load to the LDO, in order to allow the LDO output to reach the 4V threshold and allow switching to begin.

Once switching begins, LDO operation transitions from current-source operation to voltage regulation. The minimum operating V_{IN} is then limited by the RDS_{ON} of the internal LDO MOSFET. The current required to power the SC461 and external MOSFET gates causes a voltage drop from the V_{IN} pin to the VLDO pin. The VLDO pin must stay above 4V, otherwise the LDO control will revert back to current-source operation, causing more voltage drop at the LDO output. The RDS_{ON} of the LDO MOSFET at low V_{IN} is typically 28 ohms at 25°C.

Design Procedure

When designing a switch mode supply the input voltage range, load current, switching frequency, and inductor ripple current must be specified.

The maximum input voltage (V_{INMAX}) is the highest specified input voltage. The minimum input voltage (V_{INMIN}) is determined by the lowest input voltage including the voltage drops due to connectors, fuses, switches, and PCB traces. The following parameters define the design.

- Nominal output voltage (V_{OUT})
- Static or DC output tolerance
- Transient response
- Maximum load current (I_{OUT})

There are two values of load current to evaluate — continuous load current and peak load current. Continuous load current relates to thermal stresses which drive the selection of the inductor and input capacitors. Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors, and design of the current limit circuit.

The following values are used in this design.

- V_{IN} = 24V ± 10%
- V_{OUT} = 1.8V ± 4%
- f_{SW} = 220kHz
- Load = 10A maximum

Frequency Selection

Selection of the switching frequency requires making a trade-off between the size and cost of the external filter components (inductor and output capacitor) and the power conversion efficiency.

The desired switching frequency is 220kHz.

A resistor, R_{TON} is used to program the on-time (indirectly setting the frequency) using the following equation.

$$R_{TON} = \frac{(T_{ON} - 10ns) \times V_{IN}}{28.2pF \times V_{OUT}} = \frac{\left(\frac{V_{OUT}}{V_{IN} \times f_{SW}} - 10ns\right) \times V_{IN}}{28.2pF \times V_{OUT}}$$

To select R_{TON}, use the maximum value for V_{IN}, and for T_{ON} use the value associated with maximum V_{IN}.

Applications Information (continued)

$$T_{ON} = \frac{V_{OUT}}{V_{INMAX} \times f_{SW}}$$

T_{ON} = 310 nsec at 26.4V_{IN}, 1.8V_{OUT}, 220kHz

Substituting for R_{TON} results in the following solution.

R_{TON} = 156kΩ, use R_{TON} = 154kΩ

Inductor Selection

In order to determine the inductance, the ripple current must first be defined. Low inductor values result in smaller size but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current/voltage and for a given DC resistance are more efficient. However, larger inductance translates directly into larger packages and higher cost. Cost, size, output ripple, and efficiency are all used in the selection process.

The ripple current will also set the boundary for power-save operation. The switching will typically enter power-save mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 4A then Power-save operation will typically start for loads less than 2A. If ripple current is set at 40% of maximum load current, then power-save will start for loads less than 20% of maximum current.

The inductor value is typically selected to provide a ripple current that is between 25% to 60% of the maximum load current. This provides an optimal trade-off between cost, efficiency, and transient performance.

During the DH on-time, voltage across the inductor is (V_{IN} - V_{OUT}). The following equation for determining inductance is shown.

$$L = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{I_{RIPPLE}}$$

In this example the inductor ripple current is set approximately equal to 50% of the maximum load current. Thus ripple current target will be 50% x 10A or 5A.

To find the minimum inductance needed, use the V_{IN} and T_{ON} values that correspond to V_{INMAX}.

$$L = \frac{(26.4 - 1.8) \times 310\,ns}{5\,A} = 1.52\,\mu H$$

A slightly smaller value of 1.5µH is selected.

Note that the inductor must be rated for the maximum DC load current plus 1/2 of the ripple current.

The ripple current under minimum V_{IN} conditions is also checked using the following equations.

$$T_{ON_VINMIN} = \frac{28.2pF \times R_{TON} \times V_{OUT}}{V_{INMIN}} + 10ns = 372ns$$

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{L}$$

$$I_{RIPPLE_VINMIN} = \frac{(21.6 - 1.8) \times 372ns}{1.5\mu H} = 4.9A$$

Capacitor Selection

The output capacitors are chosen based on required ESR and capacitance. The maximum ESR requirement is controlled by the output ripple requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple plus 1/2 of the peak-to-peak ripple. Change in the output ripple voltage will lead to a change in DC voltage at the output.

The design goal is for the output voltage regulation to be ±4% under static conditions. The internal 600mV reference tolerance is 1%. Allowing 1% tolerance from the FB resistor divider, this allows 2% tolerance due to V_{OUT} ripple. Since this 2% error comes from 1/2 of the ripple voltage, the allowable ripple is 4%, or 72mV for a 1.8V output.

The maximum ripple current of 5A creates a ripple voltage across the ESR. The maximum ESR value allowed is shown by the following equations.

$$ESR_{MAX} = \frac{V_{RIPPLE}}{I_{RIPPLEMAX}} = \frac{72mV}{5A}$$

ESR_{MAX} = 14.4 mΩ

The output capacitance is chosen to meet transient requirements. A worst-case load release, from maximum

Applications Information (continued)

load to no load at the exact moment when inductor current is at the peak, determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in < 1µs), the output capacitor must absorb all the inductor's stored energy. This will cause a peak voltage on the capacitor according to the following equation.

$$COUT_{MIN} = \frac{L\left(I_{OUT} + \frac{1}{2} \times I_{RIPPLEMAX}\right)^2}{(V_{PEAK})^2 - (V_{OUT})^2}$$

Assuming a peak voltage V_{PEAK} of 1.98 (180mV rise upon load release), and a 10A load release, the required capacitance is shown by the next equation.

$$COUT_{MIN} = \frac{1.5\mu H\left(10 + \frac{1}{2} \times 5\right)^2}{(1.98)^2 - (1.80)^2}$$

$COUT_{MIN}$ = 344µF

If the load release is relatively slow, the output capacitance can be reduced. At heavy loads during normal switching, when the FB pin is above the 600mV reference, the DL output is high and the low-side MOSFET is on. During this time, the voltage across the inductor is approximately ($-V_{OUT}$). This causes a down-slope or falling di/dt in the inductor. If the load di/dt is not faster than the -di/dt in the inductor, then the inductor current will tend to track the falling load current. This will reduce the excess inductive energy that must be absorbed by the output capacitor, therefore a smaller capacitance can be used.

The following can be used to calculate the needed capacitance for a given dI_{LOAD}/dt. Peak inductor current is shown by the next equation.

$I_{LPK} = I_{MAX} + 1/2 \times I_{RIPPLEMAX}$

$I_{LPK} = 10 + 1/2 \times 5 = 12.5A$

$$\text{Rate of change of Load Current} = \frac{dI_{LOAD}}{dt}$$

I_{MAX} = maximum load release = 10A

$$C_{OUT} = I_{LPK} \times \frac{L \times \frac{I_{LPK}}{V_{OUT}} - \frac{I_{MAX}}{dI_{LOAD}} \times dt}{2(V_{PK} - V_{OUT})}$$

Example

$$\frac{dI_{LOAD}}{dt} = \frac{2.5A}{\mu s}$$

This would cause the output current to move from 10A to zero in 4µs.

$$C_{OUT} = 12.5 \times \frac{1.5\mu H \times \frac{12.5}{1.8} - \frac{10}{2.5} \times 1\mu s}{2 \times (1.98 - 1.8)}$$

C_{OUT} = 223µF

Note that C_{OUT} is much smaller in this example, 223µF compared to 344µF based on a worst-case load release. To meet the two design criteria of minimum 336µF and maximum 14.4mΩ ESR, use two capacitors rated at 220µF/15mΩ.

It is recommended that an additional small capacitor with a value of 1 to 10µF be placed in parallel with C_{OUT} in order to filter high frequency switching noise.

Stability Considerations

Unstable operation is possible with adaptive on-time controllers, and usually takes the form of double-pulsing or ESR loop instability.

Double-pulsing occurs due to switching noise seen at the FB input or because the FB ripple voltage is too low. This causes the FB comparator to trigger prematurely after the 250ns minimum off-time has expired. In extreme cases the noise can cause three or more successive on-times. Double-pulsing will result in higher ripple voltage at the output, but in most applications it will not affect operation. This form of instability can usually be avoided by providing the FB pin with a smooth, clean ripple signal that is at least 10mVp-p, which may dictate the need to increase the ESR of the output capacitors. It is also imperative to provide a proper PCB layout as discussed in the Layout Guidelines section.

Applications Information (continued)

Another way to eliminate doubling-pulsing is to add a small capacitor across the upper feedback resistor, as shown in Figure 16. This capacitor should be left unpopulated unless it can be confirmed that double-pulsing exists. Adding the C_{TOP} capacitor will couple more ripple into FB to help eliminate the problem. An optional connection on the PCB should be available for this capacitor.

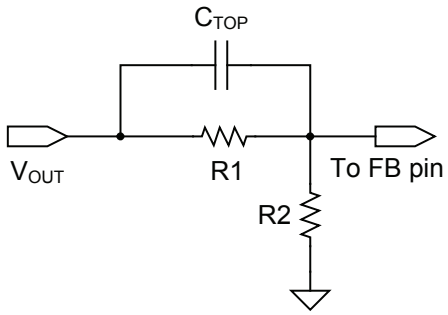


Figure 16 — Capacitor Coupling to FB Pin

NOTE: The C_{TOP} capacitor can moderately affect the DC output voltage, refer to the section on V_{OUT} voltage selection.

ESR loop instability is caused by insufficient ESR. The details of this stability issue are discussed in the ESR Requirements section. The best method for checking stability is to apply a zero-to-full load transient and observe the output voltage ripple envelope for overshoot and ringing. Ringing for more than one cycle after the initial step is an indication that the ESR should be increased.

One simple way to solve this problem is to add trace resistance in the high current output path. A side effect of adding trace resistance is decreased load regulation.

ESR Requirements

A minimum ESR is required for two reasons. One reason is to generate enough output ripple voltage to provide 10mVp-p at the FB pin (after the resistor divider) to avoid double-pulsing.

The second reason is to prevent instability due to insufficient ESR. The on-time control regulates the valley of the output ripple voltage. This ripple voltage is the sum of the two voltages. One is the ripple generated by the ESR, the other is the ripple due to capacitive charging and discharging during the switching cycle. For most applications the minimum ESR ripple voltage is dominated by the output capacitors, typically SP or POSCAP devices. For stability the ESR zero of the output capacitor should be lower than approximately one-third the switching frequency. The formula for minimum ESR is shown by the following equation.

$$ESR_{MIN} = \frac{3}{2 \times \pi \times C_{OUT} \times f_{sw}}$$

Using Ceramic Output Capacitors

When using high ESR value capacitors, the feedback voltage ripple lags the phase node voltage by 90 degrees and the converter is easily stabilized. When using ceramic output capacitors, the ESR value is normally too small to meet the above ESR criteria. As a result, the feedback voltage ripple is 180 degrees from the phase node leading to unstable operation. In this application it is necessary to add a small virtual ESR network that is composed of two capacitors and one resistor, as shown by R_L, C_L, and C_C in Figure 17.

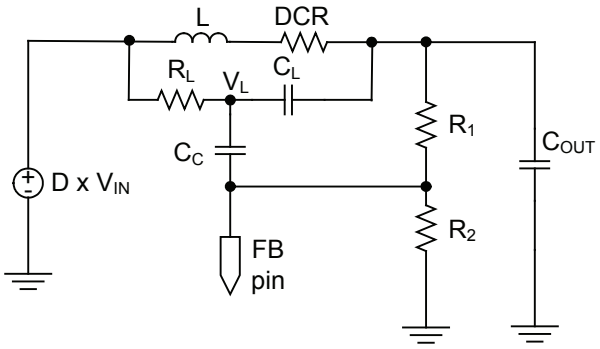


Figure 17 — Virtual ESR Ramp Circuit

The ripple voltage at FB is a superposition of two voltage sources: the voltage across C_L and the output ripple voltage. They are defined in the following equations.

$$Vc_L = \frac{I_L \times DCR(s \times L / DCR + 1)}{S \times R_L C_L + 1}$$

$$\Delta V_{OUT} = \frac{\Delta I_L}{8C \times f_{SW}}$$

Figure 18 shows the equivalent circuit for calculating the magnitude of the ripple contribution at the FB pin due to C_L.

Applications Information (continued)

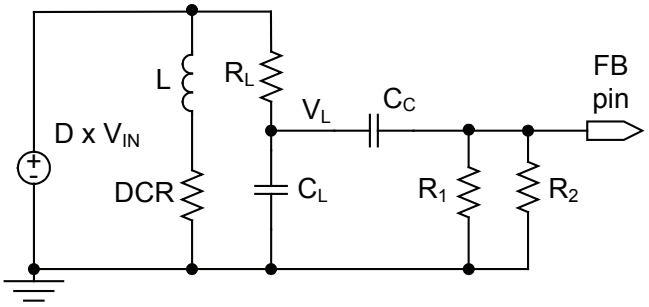


Figure 18 — FB Voltage by CL Voltage

The magnitude of the FB ripple contribution due to C_L is shown by the following equation.

$$VFBc_L = Vc_L \times \frac{(R_1 // R_2) \times S \times C_C}{(R_1 // R_2) \times S \times C_C + 1}$$

Figure 19 shows the equivalent circuit for calculating the magnitude of the ripple contribution due to the output voltage ripple.

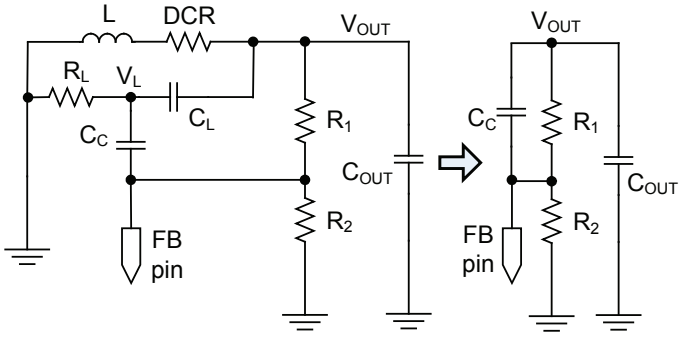


Figure 19 — FB Voltage by Output Voltage

The magnitude of the FB ripple contribution due to output voltage ripple is shown by the following equation.

$$VFB\Delta V_{OUT} = \Delta V_{OUT} \times \frac{R_2}{R_1 // \frac{1}{S \times C_C} + R_2}$$

The purpose of this network is to couple the inductor current ripple information into the feedback voltage such that the feedback voltage has 90 degrees phase lag to the switching node similar to the case of using standard high ESR capacitors. This is illustrated in Figure 20.

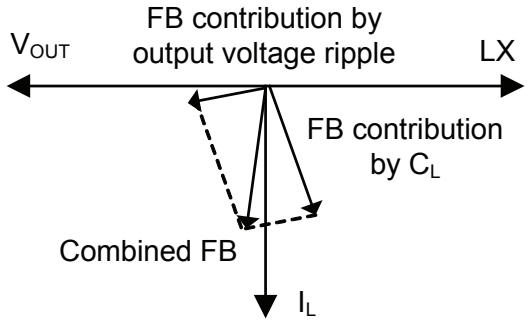


Figure 20 — FB voltage in Phaser Diagram

The magnitude of the feedback ripple voltage, which is dominated by the contribution from C_L, is controlled by the value of R_1, R_2 and C_C. If the corner frequency of (R_1// R_2) x C_C is too high, the ripple magnitude at the FB pin will be smaller, which can lead to double-pulsing. Conversely, if the corner frequency of (R_1// R_2) x C_C is too low, the ripple magnitude at FB pin will be higher. Since the SC461 regulates to the valley of the ripple voltage at the FB pin, a high ripple magnitude is undesirable as it significantly impacts the output voltage regulation. As a result, it is desirable to select a corner frequency for (R_1// R_2) x C_C to achieve enough, but not excessive, ripple magnitude and phase margin. The component values for R_1, R_2, and C_C should be calculated using the following procedure.

Select C_L (typical 10nF) and R_L to match with L and DCR time constant using the following equation.

$$R_L = \frac{L}{DCR \times C_L}$$

Select C_C by using the following equation.

$$C_C \approx \frac{1}{R_1 // R_2} \times \frac{3}{2 \times \pi \times f_{sw}}$$

The resistor values (R_1 and R_2) in the voltage divider circuit set the V_{OUT} for the switcher. The typical value for C_C is from 10pF to 1nF.

Dropout Performance

The output voltage adjust range for continuous-conduction operation is limited by the fixed 250ns (typical)

Applications Information (continued)

minimum off-time of the one-shot. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times.

The duty-factor limitation is shown by the following equation.

$$DUTY = \frac{T_{ON(MIN)}}{T_{ON(MIN)} + T_{OFF(MAX)}}$$

The inductor resistance and MOSFET on-state voltage drops must be included when performing worst-case dropout duty-factor calculations.

System DC Accuracy (V_{OUT} Controller)

Three factors affect V_{OUT} accuracy: the trip point of the FB error comparator, the ripple voltage variation with line and load, and the external resistor tolerance. The error comparator offset is trimmed so that under static conditions it trips when the feedback pin is 600mV, $\pm$1%.

The on-time pulse from the SC461 in the design example is calculated to give a pseudo-fixed frequency of 220kHz. Some frequency variation with line and load is expected. This variation changes the output ripple voltage. Because adaptive on-time converters regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if the output ripple is 50mV with V_{IN} = 6 volts, then the measured DC output will be 25mV above the comparator trip point. If the ripple increases to 80mV with V_{IN} = 25V, then the measured DC output will be 40mV above the comparator trip. The best way to minimize this effect is to minimize the output ripple.

To compensate for valley regulation, it may be desirable to use passive droop. Take the feedback directly from the output side of the inductor and place a small amount of trace resistance between the inductor and output capacitor. This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit. Passive droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced as seen at the load.

The use of 1% feedback resistors contributes up to 1% error. If tighter DC accuracy is required, 0.1% resistors should be used.

The output inductor value may change with current. This will change the output ripple and therefore will have a minor effect on the DC output voltage. The output ESR also affects the output ripple and thus has a minor effect on the DC output voltage.

Switching Frequency Variations

The switching frequency will vary depending on line and load conditions. The line variations are a result of fixed propagation delays in the on-time one-shot, as well as unavoidable delays in the external MOSFET switching. As V_{IN} increases, these factors make the actual DH on-time slightly longer than the ideal on-time. The net effect is that frequency tends to falls slightly with increasing input voltage.

The switching frequency also varies with load current as a result of the power losses in the MOSFETs and the inductor. For a conventional PWM constant-frequency converter, as load increases the duty cycle also increases slightly to compensate for IR and switching losses in the MOSFETs and inductor. An adaptive on-time converter must also compensate for the same losses by increasing the effective duty cycle (more time is spent drawing energy from V_{IN} as losses increase). Because the on-time is essentially constant for a given V_{OUT}/V_{IN} combination, to offset the losses the off-time will reduce slightly as load increases. The net effect is that switching frequency increases slightly with increasing load.

PCB Layout Guidelines

A switch-mode converter requires good PCB layout which is essential to achieving high performance. The following guidelines will provide an optimum PCB layout.

The device layout recommendations consist of four parts.

- Grounding for PGND and AGND
- Power components
- Low-noise analog circuits
- Bypass capacitors

Grounding for PGND and AGND

- A ground plane layer for PGND is recommended to minimize the effects of switching noise, resistive losses, and to maximize heat removal from the power components.

Applications Information (continued)

- A separate ground plane or island should be used for AGND and all associated components. The AGND island should avoid overlapping switching signals on other layers (DH/DL/BST/LX).
- Connect PGND and AGND together with a zero ohm resistor or copper trace. Make the connection near the AGND and PGND pins of the IC.

Power Components

- Use short, wide traces between the following power components.
  - Input capacitors and high-side MOSFETs
  - High-side and Low-side MOSFETs and inductor (LX connection). Use wide copper traces to provide high current carrying capacity and for heat dissipation.
  - Inductor and output capacitors.
  - All PGND connections — the input capacitors, low-side MOSFETs, output capacitors, and the PGND pin of the SC461.
- An inner layer ground plane is recommended.
- Each power component requires a short, low impedance connection to the PGND plane.
- Place vias to the PGND plane directly near the component pins.
- Use short wide traces for the pin connections from the SC461 (LX, DH, DL and BST). Do not route these traces near the sensitive low-noise analog signals (FB, SS, TON, V_{OUT}).
- Avoid overlapping of the DL trace with LX/DH/BST. This helps reduce transient peaks on the gate of the low-side MOSFET during the turn-on of the high-side MOSFET.

Low-noise Analog Circuits

Low-noise analog circuits are sensitive circuits that are referenced to AGND. Due to their high impedance and sensitivity to noise, it is important that these circuits be located as far as possible from the switching signals.

- Use a plane or solid area for AGND. Place all components connected to AGND above this area.
  - Use short direct traces for the AGND connections to all components.
  - Place vias to the AGND plane directly near the component pins.
- Proper routing of the V_{OUT} sense trace is essential since it feeds into the FB resistor divider. Noise on the FB waveform will cause instability and multiple pulsing.
  - Connect the V_{OUT} sense trace directly to the output capacitor or a ceramic bypass capacitor.
  - Route this trace over to the VOUT pin, carefully avoiding all switching signals and power components.
  - Route this trace in a quiet layer if possible.
  - Route this trace away from the switching traces and components, even if the trace is longer. Avoid shorter trace routing through the power switching area.
  - If a bypass capacitor is used at the IC side of the V_{OUT} sense trace, it should be placed near the FB resistor divider.
- All components connected to the FB pin must be located near the pin. The FB traces should be kept small and not routed near any noisy switching connections or power components.
- Place the SS capacitor near the SS pin with a short direct connection to the AGND plane.
- Place the R_{LIM} resistor near the IC. For an accurate I_{LIM} current sense connection, route the R_{LIM} trace directly to the drain of the low-side MOSFET (LX). Use an inner routing layer if needed.
- Place the R_{TON} resistor near the TON pin. Route R_{TON} to the TON pin and to AGND using short traces and avoid all switching signals.

Bypass Capacitors

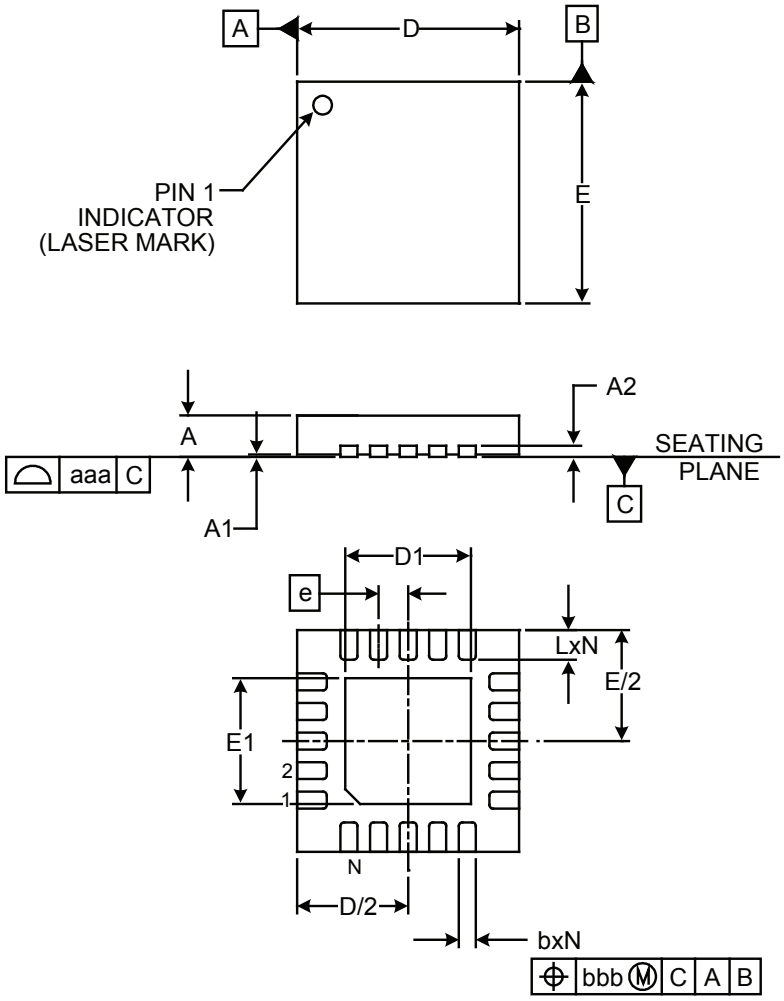
The device requires bypass capacitors for the following pins.

- VDDA pin with respect to AGND. This 0.1µF minimum capacitor must be placed and routed close to the IC pins, on the same layer as the IC. This capacitor also functions as bypass for the LDO output, since the VDDA and VLDO pins are adjacent.
- VDDP with respect to PGND. This 1µF minimum capacitor must be placed and routed close to the IC pins and on the same layer as the IC.

Applications Information (continued)

- BST pin with respect to LX. This 0.1µF minimum capacitor must be placed near the IC, on either side of the PCB. Use short traces for the routing between the capacitor and the IC.
- VIN pin with respect to AGND. This 0.1µF minimum capacitor must be placed and routed close to the IC pins. This capacitor provides noise filtering for the input to the internal LDO.

Outline Drawing — MLPQ-UT20 3x3

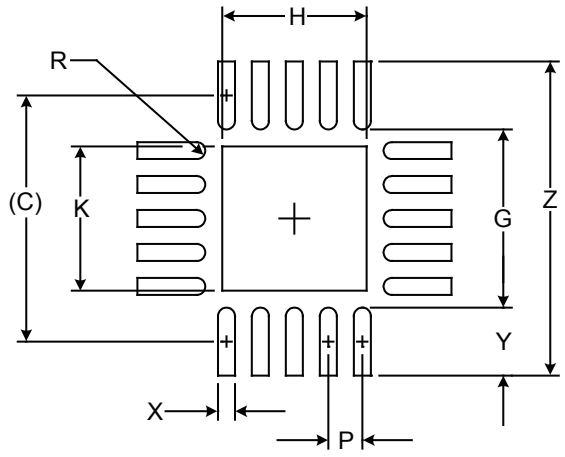


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(0.1524)	
b	.006	.008	.010	0.15	0.20	0.25
D	.114	.118	.122	2.90	3.00	3.10
D1	.061	.067	.071	1.55	1.70	1.80
E	.114	.118	.122	2.90	3.00	3.10
E1	.061	.067	.071	1.55	1.70	1.80
e		.016 BSC			0.40 BSC	
L	.012	.016	.020	0.30	0.40	0.50
N		20			20	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP is 1.90 x 190mm.

Land Pattern — MLPQ-UT20 3x3



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.083	2.10
H	.067	1.70
K	.067	1.70
P	.016	0.40
R	.004	0.10
X	.008	0.20
Y	.031	0.80
Z	.146	3.70

NOTES:

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Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805) 498-2111 Fax: (805) 498-3804

www.semtech.com