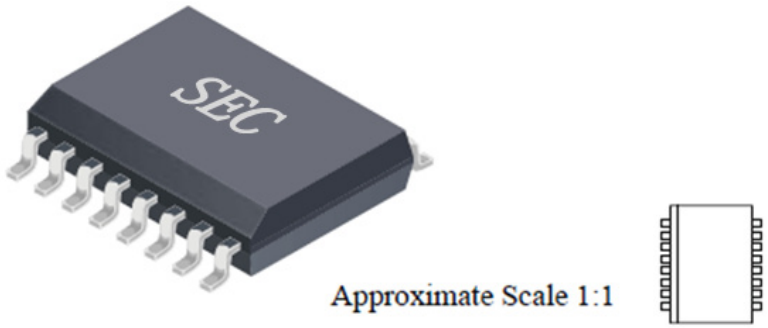
# SC212KSIT

***120 kHz Bandwidth, High Voltage Isolation Current Sensor with Integrated Overcurrent Detection***

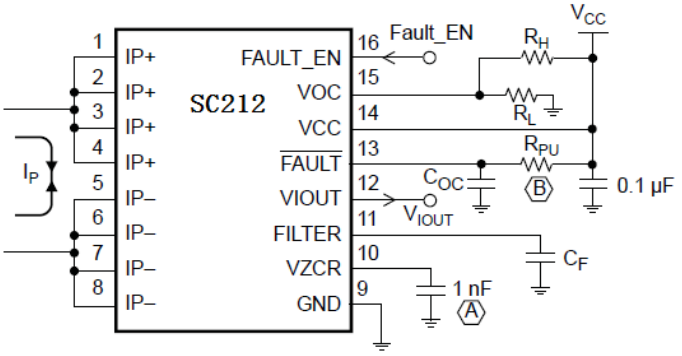
## Features and Benefits

1. Industry-leading noise performance with greatly improved bandwidth through proprietary amplifier and filter design techniques
2. Small footprint package suitable for space-constrained applications
3. 1 mΩ primary conductor resistance for low power loss
4. High isolation voltage, suitable for line-powered applications
5. User-adjustable Overcurrent Fault level
6. Overcurrent Fault signal typically responds to an overcurrent condition in < 2 µs
7. Integrated shield virtually eliminates capacitive coupling from current conductor to die due to high dV/dt voltage transients
8. Filter pin capacitor improves resolution in low bandwidth applications
9. 3 to 5.5 V, single supply operation
10. Factory trimmed sensitivity and quiescent output voltage
11. Chopper stabilization results in extremely stable quiescent output voltage
12. Ratiometric output from supply voltage




**Package: 16-pin SOIC Hall Effect IC Package (suffix SI)**

## Typical Application Circuit




| | |
|---|---|
| $R_H$, $R_L$ | Sets resistor divider reference for $V_{OC}$ |
| $C_F$ | Noise and bandwidth limiting filter capacitor |
| $C_{OC}$ | Fault delay setting capacitor, 22 nF maximum |
| Ⓐ | Use of capacitor required |
| Ⓑ | Use of resistor optional, 330 kΩ recommended. If used, resistor must be connected between $\overline{\text{FAULT}}$ pin and $V_{CC}$. |

## General Description

The SEC™ SC212KSIT current sensor provides economical and precise means for current sensing applications in industrial, commercial, and communications systems. The device is offered in a small footprint surface mount package that allows easy implementation in customer applications.

The SC212KSIT consists of a precision linear Hall sensor integrated circuit with a copper conduction path located near the surface of the silicon die. Applied current flows through the copper conduction path, and the analog output voltage from the Hall sensor linearly tracks the magnetic field generated by the applied current. The accuracy of the SC212KSIT is maximized with this patented packaging configuration because the Hall element is situated in extremely close proximity to the current to be measured.

High level immunity to current conductor dV/dt and stray electric fields, offered by SEC proprietary integrated shield technology, results in low ripple on the output and low offset drift in high-side, high voltage applications.

The voltage on the Overcurrent Input ($V_{OC}$ pin) allows customers to define an overcurrent fault threshold for the device. When the current flowing through the copper conduction path (between the $I_P$+ and $I_P$– pins) exceeds this threshold, the open drain Overcurrent Fault pin will transition to a logic low state. Factory programming of the linear Hall sensor inside of the SC212KSIT results in exceptional accuracy in both analog and digital output signals.

The internal resistance of the copper path used for current sensing is typically 1 mΩ, for low power loss. Also, the current conduction path is electrically isolated from the low voltage sensor inputs and outputs. This allows the SC212KSIT family of sensors to be used in applications requiring electrical isolation, without the use of opto-isolators or other costly isolation techniques. The SC212KSIT is provided in a small, surface mount SOIC16 package. The lead frame is plated with 100% matte tin, which is compatible with standard lead (Pb) free printed circuit board assembly processes. Internally, the device is Pb-free, except for flip-chip high-temperature Pb-based solder balls, currently exempt from RoHS. The device is fully calibrated prior to shipment from the factory.

## Applications

1. Motor control and protection
2. Load management and overcurrent detection
3. Power conversion and battery monitoring / UPS systems

## General Package Inform

| Part Number | $I_P$(A) | Sens (typ) at V= 5 V (mV/A) | Latched Fault | $T_A$(°C) | Packing |
|---|---|---|---|---|---|
| **SC212KSIT** | ±25 | 56 | Yes | –40 to 125 | Tape and Reel, 1000 pieces per reel |

## Absolute Maximum Ratings

| Characteristic | Symbol | Notes | Rating | Unit |
|---|---|---|---|---|
| **Supply Voltage** | $V_{CC}$ | | 8 | V |
| **Filter Pin** | $V_{FILTER}$ | | 8 | V |
| **Analog Output Pin** | $V_{IOUT}$ | | 32 | V |
| **Overcurrent Input Pin** | $V_{OC}$ | | 8 | V |
| **Overcurrent $\overline{\text{FAULT}}$ Pin** | $V_{\overline{FAULT}}$ | | 8 | V |
| **Fault Enable (FAULT_EN) Pin** | $V_{FAULTEN}$ | | 8 | V |
| **Voltage Reference Output Pin** | $V_{ZCR}$ | | 8 | V |
| **DC Reverse Voltage: $V_{CC}$, FILTER, $V_{IOUT}$, $V_{OC}$, FAUL, $\overline{\text{FAULT}}$_EN, and $V_{ZCR}$ Pins** | $V_{Rdcx}$ | | –0.5 | V |
| **Excess to Supply Voltage: FILTER, $V_{IOUT}$, $V_{OC}$, $\overline{\text{FAULT}}$, FAULT_EN, and $V_{ZCR}$ Pins** | $V_{EX}$ | Voltage by which pin voltage can exceed the $V_{CC}$ pin voltage | 0.3 | V |
| **Output Current Source** | $I_{IOUT(Source)}$ | | 3 | mA |
| **Output Current Sink** | $I_{IOUT(Sink)}$ | | 1 | mA |
| **Operating Ambient Temperature** | $T_A$ | Range K | –40 to 125 | °C |
| **Junction Temperature** | $T_{J(max)}$ | | 165 | °C |
| **Storage Temperature** | $T_{stg}$ | | –65 to 170 | °C |

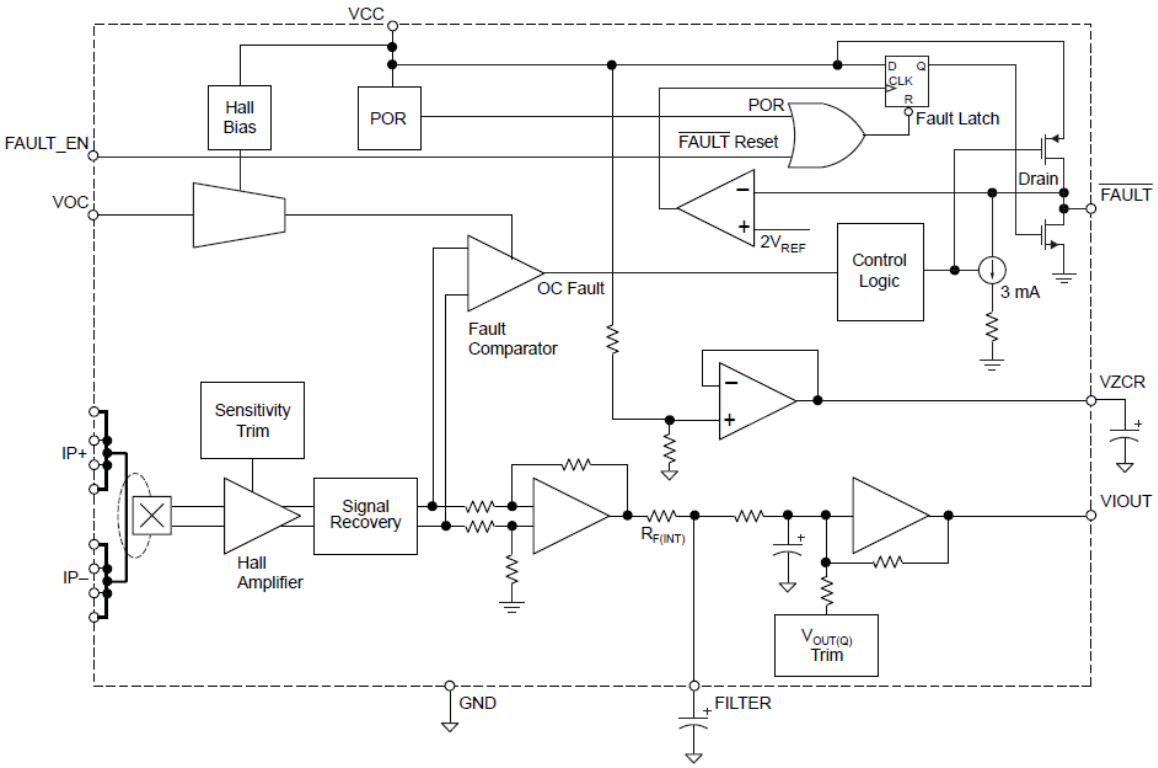
## Isolation Characteristics

| Characteristic | Symbol | Notes | Rating | Unit |
|---|---|---|---|---|
| **Dielectric Strength Test Voltage*** | $V_{ISO}$ | Agency type-tested for 60 seconds per UL standard 1577 | 3000 | VAC |
| **Working Voltage for Basic Isolation** | $V_{WFSI}$ | For basic (single) isolation per UL standard 1577; for higher continuous voltage ratings, please contact SEC | 277 | VAC |

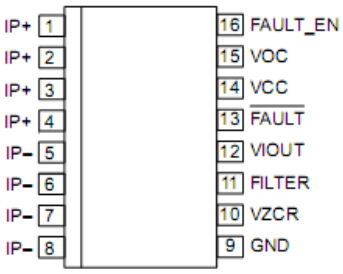
## Thermal Characteristics

| Characteristic | Symbol | Test Conditions | Value | Unit |
|---|---|---|---|---|
| **Package Thermal Resistance** | $R_{\theta JA}$ | When mounted on SEC demo board with 1332 mm2 (654 mm2 on component side and 678 mm2 on opposite side) of 2 oz. copper connected to the primary lead frame and | 17 | °C/W |

## Functional Block Diagram




## Terminal List Table, Latching Version




| Number | Name | Description |
|---|---|---|
| 1 through 4 | $I_P+$ | Sensed current copper conduction path pins. Terminals for current being sensed; fused internally, loop to $I_P–$ pins; unidirectional or bidirectional current flow. |
| 5 through 8 | $I_P–$ | Sensed current copper conduction path pins. Terminals for current being sensed; fused internally, loop to $I_P+$ pins; unidirectional or bidirectional current flow. |
| 9 | GND | Device ground connection. |
| 10 | $V_{ZCR}$ | Voltage Reference Output pin. Zero current (0 A) reference; output voltage on this pin scales with $V_{CC}$ . (Not a highly accurate reference.) |
| 11 | FILTER | Filter pin. Terminal for an external capacitor connected from this pin to GND to set the device bandwidth. |
| 12 | $V_{IOUT}$ | Analog Output pin. Output voltage on this pin is proportional to current flowing through the loop between the $I_P+$ pins and $I_P–$ pins. |
| 13 | $\overline{\text{FAULT}}$ | Overcurrent Fault pin. When current flowing between IP+ pins and IP– pins exceeds the overcurrent fault threshold, this pin transitions to a logic low state. |
| 14 | $V_{CC}$ | Supply voltage. |
| 15 | $V_{OC}$ | Overcurrent Input pin. Analog input voltage on this pin sets the overcurrent fault threshold. |
| 16 | FAULT_EN | Enables overcurrent faulting when high. Resets $\overline{\text{FAULT}}$ when low. |

## COMMON OPERATING CHARACTERISTICS

Valid at $T_A$ = –40°C to 125°C, $V_{CC}$ = 5 V, unless otherwise specified

| Characteristic | Symbol | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **ELECTRICAL CHARACTERISTICS** | | | | | | |
| Supply Voltage[1] | $V_{CC}$ | | 3 | – | 5.5 | V |
| Nominal Supply Voltage | $V_{CCN}$ | | – | 5 | – | V |
| Supply Current | $I_{CC}$ | $V_{IOUT}$ open, $\overline{FAULT}$ pin high | – | 11 | 14.5 | mA |
| Output Capacitance Load | $C_{LOAD}$ | $V_{IOUT}$ pin to GND | – | – | 10 | nF |
| Output Resistive Load | $R_{LOAD}$ | $V_{IOUT}$ pin to GND | 10 | – | – | kΩ |
| Magnetic Coupling from Device Conductor to Hall Element | $MC_{HALL}$ | Current flowing from $I_P$+ to $I_P$– pins | – | 9.5 | – | G/A |
| Internal Filter Resistance[2] | $R_{F(INT)}$ | | – | 1.7 | – | kΩ |
| Primary Conductor Resistance | $R_{PRIMARY}$ | $T_A$ = 25°C | – | 1 | – | mΩ |
| **ANALOG OUTPUT SIGNAL CHARACTERISTICS** | | | | | | |
| Full Range Linearity[3] | $E_{LIN}$ | $I_P = \pm I_{P0A}$ | –0.75 | ±0.25 | 0.75 | % |
| Symmetry[4] | $E_{SYM}$ | $I_P = \pm I_{P0A}$ | 99.1 | 100 | 100.9 | % |
| Bidirectional Quiescent Output | $V_{OUT(QBI)}$ | $I_P$ = 0 A, $T_A$ = 25°C | – | $V_{CC}$/2 | – | V |
| **TIMING PERFORMANCE CHARACTERISTICS** | | | | | | |
| $V_{IOUT}$ Signal Rise Time | $t_r$ | $T_A$ = 25°C, Swing $I_P$ from 0 A to $I_{P0A}$, no capacitor on FILTER pin, 100 pF from$V_{IOUT}$ to GND | – | 3 | – | µs |
| $V_{IOUT}$ Signal Propagation Time | $t_{PROP}$ | TA = 25°C, no capacitor on FILTER pin,100 pF from $V_{IOUT}$ to GND | – | 1 | – | µs |
| $V_{IOUT}$ Signal Response Time | $t_{RESPONSE}$ | $T_A$ = 25°C, Swing $I_P$ from 0 A to $I_{P0A}$, no capacitor on FILTER pin, 100 pF from$V_{IOUT}$ to GND | – | 4 | – | µs |
| $V_{IOUT}$ Large Signal Bandwidth | $f_{3dB}$ | –3 dB, Apply $I_P$ such that $V_{IOUT}$ = 1 Vpk-pk, no capacitor on FILTER pin, 100 pF from $V_{IOUT}$ to GND | – | 120 | – | kHz |
| Power-On Time | $t_{PO}$ | Output reaches 90% of steady-state level, no capacitor on FILTER pin, $T_A$ = 25°C | – | 35 | – | µs |
| **OVERCURRENT CHARACTERISTICS** | | | | | | |
| Setting Voltage for Overcurrent Switchpoint[5] | $V_{OC}$ | | $V_{CC}$×0.25 | – | $V_{CC}$×0.4 | V |
| Signal Noise at Overcurrent Comparator Input | $I_{NCOMP}$ | | – | ±1 | – | A |
| Overcurrent Fault Switchpoint Error[6,7] | $E_{OC}$ | Switchpoint in $V_{OC}$ safe operating area; assumes $I_{NCOMP}$ = 0 A | – | ±5 | – | % |
| Overcurrent $\overline{FAULT}$ Pin Output Voltage | $V_{\overline{FAULT}}$ | 1 mA sink current at $\overline{FAULT}$ pin | – | – | 0.4 | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| Fault Enable (FAULT_EN Pin) Input Low Voltage Threshold | $V_{IL}$ | | – | – | $0.1 \times V_{CC}$ | V |
| Fault Enable (FAULT_EN Pin) Input High Voltage Threshold | $V_{IH}$ | | $0.8 \times V_{CC}$ | – | – | V |
| Fault Enable (FAULT_EN Pin) Input Resistance | $R_{FEI}$ | | – | 1 | – | MΩ |
| **OVERCURRENT CHARACTERISTICS** | | | | | | |
| Fault Enable (FAULT_EN Pin) Delay[8] | $t_{FED}$ | Set FAULT_EN to low, $V_{OC} = 0.25 \times V_{CC}$, $C_{OC}$ = 0 F; then run a DC $I_P$ exceeding the corresponding overcurrent threshold; then reset FAULT_EN from low to high and measure the delay from the rising edge of FAULT_EN to the falling edge of $\overline{FAULT}$ | – | 15 | – | µs |
| Fault Enable (FAULT_EN Pin) Delay(Non-Latching versions)[9] | $t_{FED(NL)}$ | Set FAULT_EN to low, $V_{OC} = 0.25 \times V_{CC}$, $C_{OC}$ = 0 F; then run a DC $I_P$ exceeding the corresponding overcurrent threshold; then reset FAULT_EN from low to high and measure the delay from the rising edge of FAULT_EN to the falling edge of $\overline{FAULT}$ | – | 150 | – | ns |
| Overcurrent Fault Response Time | $t_{OC}$ | FAULT_EN set to high for a minimum of 20 µs before the overcurrent event; switchpoint set at $V_{OC} = 0.25 \times V_{CC}$; delay from Ip exceeding overcurrent fault threshold to $V_{\overline{FAULT}} < 0.4$ V, | – | 1.9 | – | µs |
| Undercurrent Fault Response Time(Non-Latching versions) | $t_{UC}$ | FAULT_EN set to high for a minimum of 20 µs before the undercurrent event; switchpoint set at $V_{OC} = 0.25 \times V_{CC}$; delay from $I_P$ falling below the overcurrent faultthreshold to $V_{\overline{FAULT}} > 0.8 \times V_{CC}$, without external $C_{OC}$ capacitor, $R_{PU}$ = 330 kΩ | – | 3 | – | µs |
| Overcurrent Fault Reset Delay | $t_{OCR}$ | Time from $V_{FAULTEN} < V_{IL}$ to $V_{\overline{FAULT}} > 0.8 \times V_{CC}$, $R_{PU}$ = 330 kΩ | – | 500 | – | ns |
| Overcurrent Fault Reset Hold Time | $t_{OCH}$ | Time from $V_{FAULTEN} < V_{IL}$ to rising edge of $V_{\overline{FAULT}}$ | – | 250 | – | ns |
| Overcurrent Input Pin Resistance | $R_{OC}$ | $T_A$ = 25°C, $V_{OC}$ pin to GND | 2 | – | – | MΩ |
| **VOLTAGE REFERENCE CHARACTERISTICS** | | | | | | |
| Voltage Reference Output | $V_{ZCR}$ | $T_A$ = 25 °C (Not a highly accurate reference) | $0.48 \times V_{CC}$ | $0.5 \times V_{CC}$ | $0.51 \times V_{CC}$ | V |
| Voltage Reference Output Load Current | $I_{ZCR}$ | Source current | 3 | – | – | mA |
| | | Sink current | 50 | – | – | µA |
| Voltage Reference Output Drift | $\Delta V_{ZCR}$ | | – | ±10 | – | mV |

1. **Devices are programmed for maximum accuracy at $V_{CC}$ = 5 V. The device contains ratiometry circuits that accurately alter the 0 A Output Voltage and Sensitivity level of the device in proportion to the applied $V_{CC}$ level. However, as a result of minor nonlinearities in the ratiometry circuit, additional output error will result when $V_{CC}$ varies from the $V_{CC}$ level at which the device was programmed. Customers that plan to operate the device at a $V_{CC}$ level other than the $V_{CC}$ level at which the device was programmed should contact their local SEC sales representative regarding expected device accuracy levels**
2. **Under these bias conditions.**
3. **RF(INT) forms an RC circuit via the FILTER pin.**
4. **This parameter can drift by as much as 0.8% over the lifetime of this product.**
5. **This parameter can drift by as much as 1% over the lifetime of this product.**
6. **See page 8 on how to set overcurrent fault switch point.**
7. **Switchpoint can be lower at the expense of switch point accuracy.**
8. **This error specification does not include the effect of noise. See the INCOMP specification in order to factor in the additional influence of noise on the fault switch point.**
9. **Fault Enable Delay is designed to avoid false tripping of an Overcurrent (OC) fault at power-up. A 15 µs (typical) delay will always be needed, every time FAULT_EN is raised from low to high, before the device is ready for responding to any overcurrent event.**
10. **During power-up, this delay is 15 µs in order to avoid false tripping of an Overcurrent (OC) fault.**

## PERFORMANCE CHARACTERISTICS

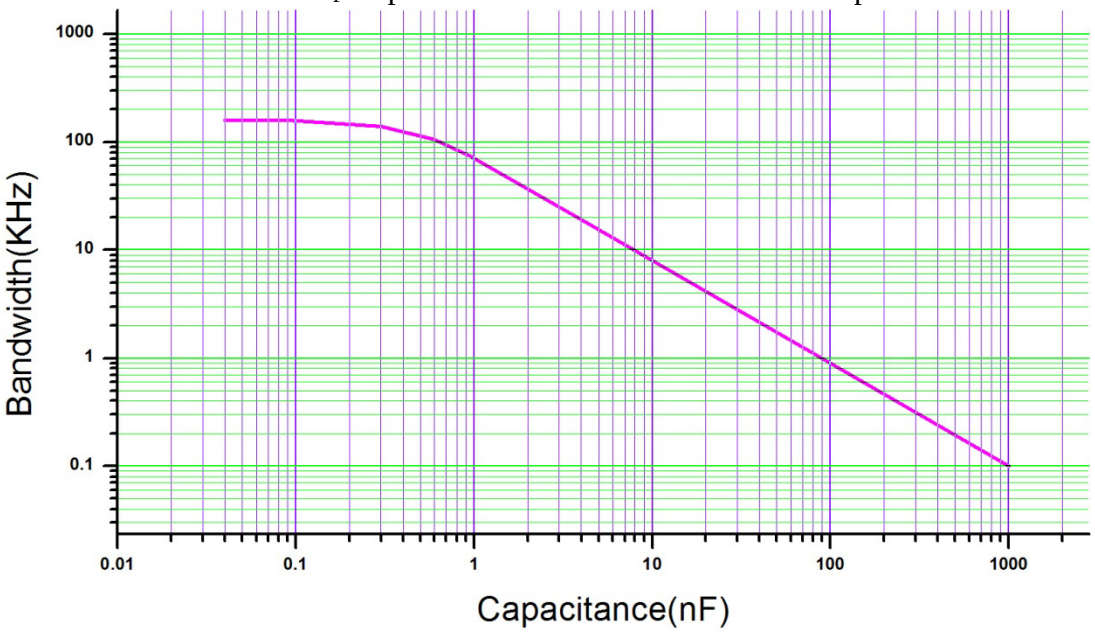
TA Range K, valid at $T_A$ = – 40°C to 125°C, $V_{CC}$ = 5 V, unless otherwise specified

| Characteristic | Symbol | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Optimized Accuracy Range**[1] | $I_{POA}$ | | –12.5 | – | 12.5 | A |
| **Linear Sensing Range** | $I_R$ | | –37.5 | – | 37.5 | A |
| **Noise**[2] | $V_{NOISE}$(rms) | $T_A$ = 25°C, Sens = 56 mV/A, $C_f$ = 0, $C_{LOAD}$ = 4.7 nF, $R_{LOAD}$ open | – | 1.50 | – | mV |
| **Sensitivity**[3] | Sens | $I_P$ = 12.5 A, $T_A$ = 25°C | – | 56 | – | mV/A |
| | | $I_P$ = 12.5 A, $T_A$ = 25°C to 125°C | – | 56 | – | mV/A |
| | | $I_P$ = 12.5 A, $T_A$ = –40°C to 25°C | – | 57 | – | mV/A |
| **Electrical Offset Voltage Variation Relative to $V_{out}$**[4] | $V_{OE}$ | $I_P$ = 0 A, $T_A$ = 25°C | – | ±4 | – | mV |
| | | $I_P$ = 0 A, $T_A$ = 25°C to 125°C | – | ±14 | – | mV |
| | | $I_P$ = 0 A, $T_A$ = –40°C to 25°C | – | ±23 | – | mV |
| **Total Output Error**[5] | $E_{TOT}$ | Over full scale of $I_{POA}$, $I_P$ applied for 5 ms, $T_A$ = 25°C to 125°C | – | ±2.2 | – | % |
| | | Over full scale of $I_{POA}$, $I_P$ applied for 5 ms, $T_A$ = –40°C to 25°C | – | ±3.9 | – | % |

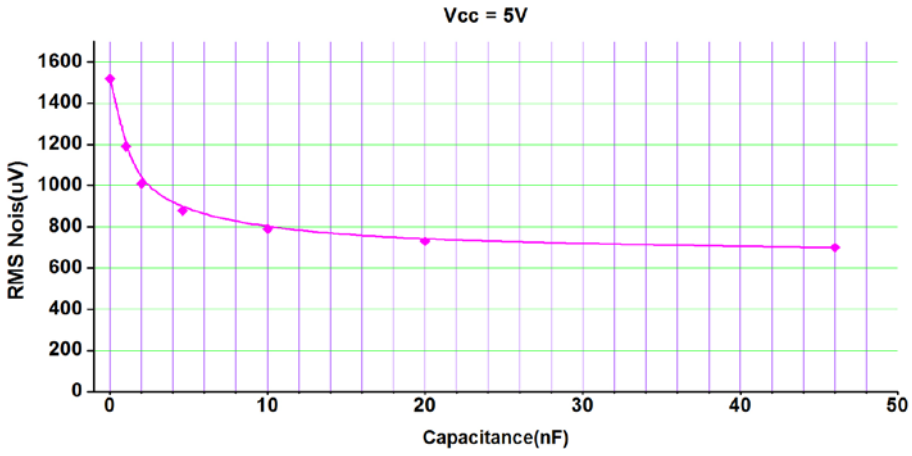
1. **Although the device is accurate over the entire linear range, the device is programmed for maximum accuracy over the range defined by $I_{POA}$ .The reason for this is that in many applications, such as motor control, the start-up current of the motor is approximately three times higher than the running current.**
2. **$V_{pk-pk}$ noise (6 sigma noise) is equal to 6 × $V_{NOISE}$(rms). Lower noise levels than this can be achieved by using $C_f$ for applications requiring narrower bandwidth. See Characteristic Performance page for graphs of noise versus $C_f$ and bandwidth versus $C_f$.**
3. **This parameter can drift by as much as 2.4% over the lifetime of this product.**
4. **This parameter can drift by as much as 13 mV over the lifetime of this product.**
5. **This parameter can drift by as much as 2.5% over the lifetime of this product.**

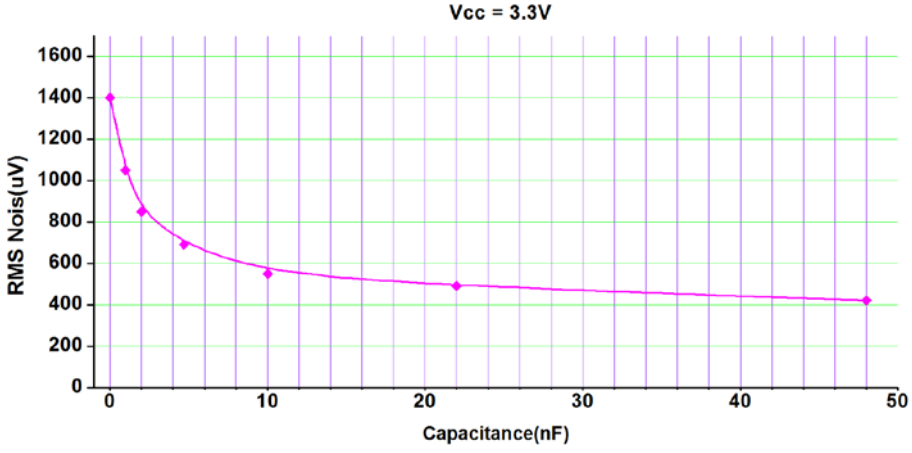
## Characteristic Performance

Bandwidth value，$C_F$ Capacitor connected between FILTER pin and GND



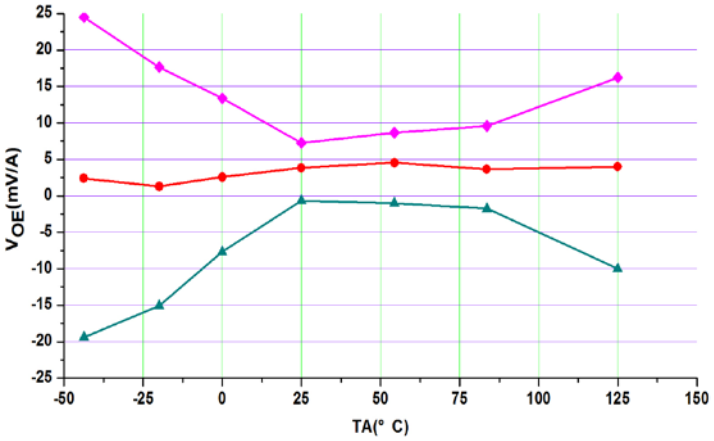

Noise versus External Capacitor Value
$C_F$ Capacitor connected between FILTER pin and GND



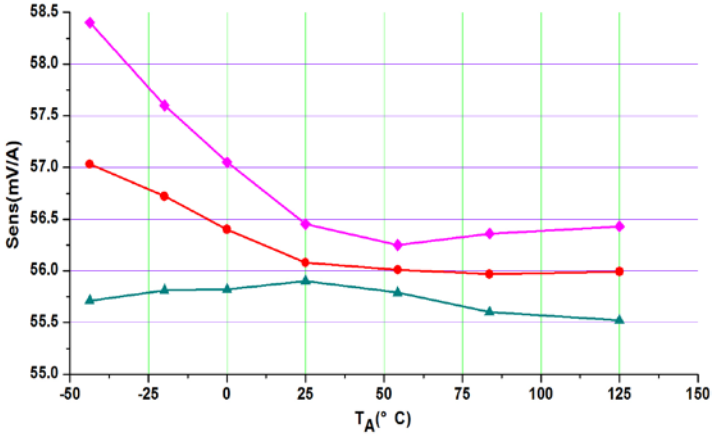



## Characteristic Performance Data
## Accuracy Data

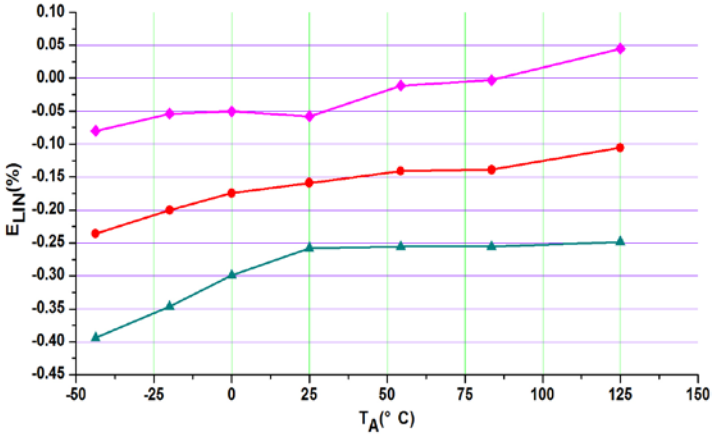
### Electrical Offset Voltage versus Ambient Temperature



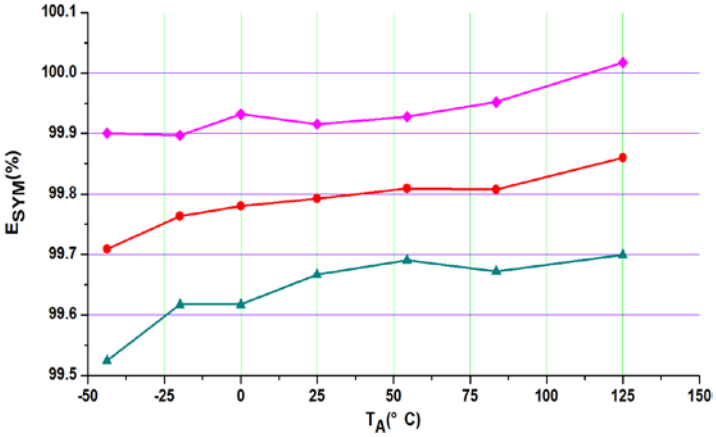

### Sensitivity versus Ambient Temperature



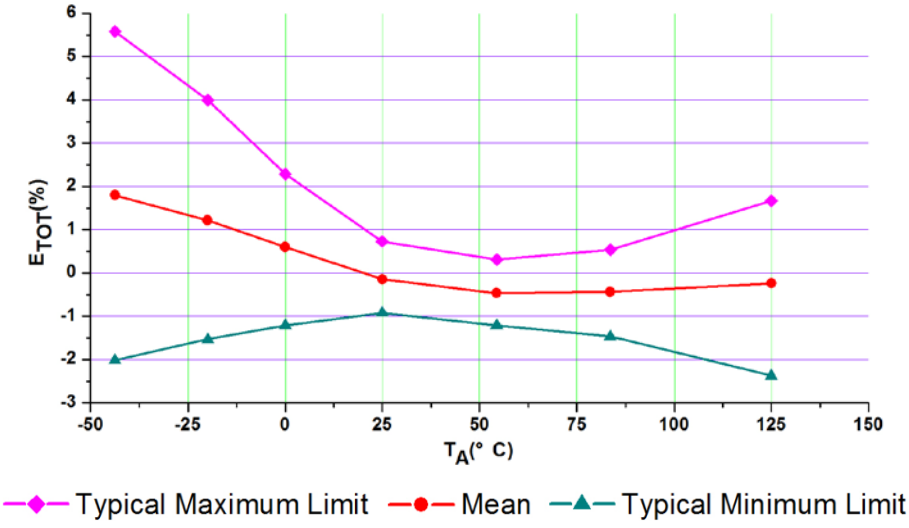

### Nonlinearity versus Ambient Temperature




### Symmetry versus Ambient Temperature




### Total Output Error versus Ambient Temperature

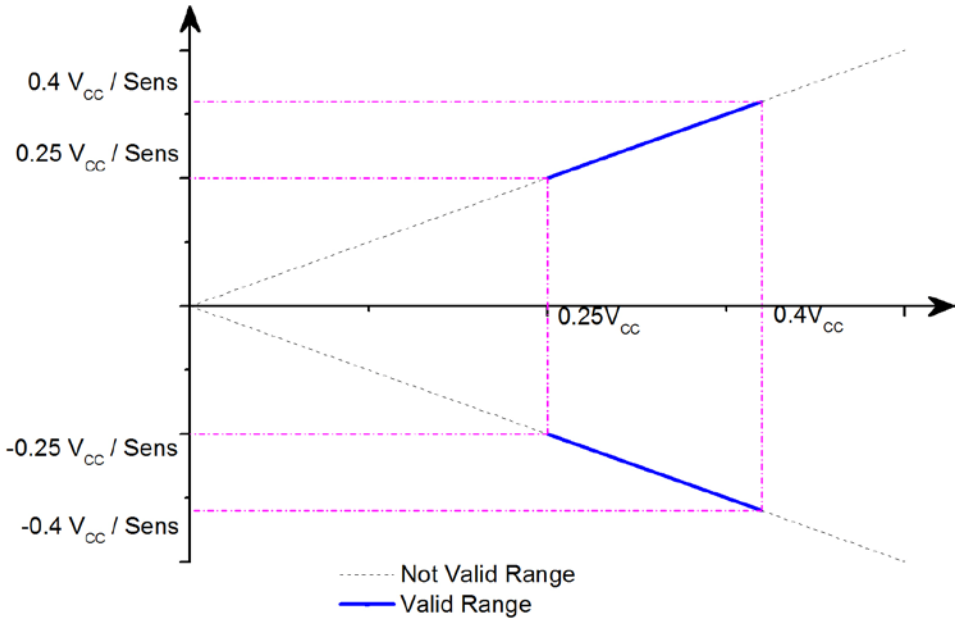


**Setting Overcurrent Fault Switchpoint**

The $V_{OC}$ needed for setting the overcurrent fault switchpoint can be calculated as follows:

$$V_{OC} = \text{Sens} \times | I_{OC} | ,$$

where $V_{OC}$ is in mV, Sens in mV/A, and $I_{OC}$ (overcurrent fault switchpoint) in A.
| Ioc | is the overcurrent fault switchpoint for a bidirectional (AC) current, which means a bi-directional sensor will have two symmetrical overcurrent fault switchpoints, $+I_{OC}$ and $-I_{OC}$ .
See the following graph for $I_{OC}$ and $V_{OC}$ ranges:




**Example:For SC212KSIT, if required overcurrent fault switchpoint is 25 A, and $V_{CC}$ = 5 V, then the required $V_{OC}$ can be calculated as follows:**

$$V_{OC} = \text{Sens} \times I_{OC} = 56 \times 25 = 1400 \text{ (mV)}$$

**Overcurrent Fault Operation**

The primary concern with high-speed fault detection is that noise may cause false tripping. Various applications have or need to be able to ignore certain faults that are due to switching noise or other parasitic phenomena, which are application dependant. The problem with simply trying to filter out this noise in the main signal path is that in high-speed applications, with asymmetric noise, the act of filtering introduces an error into the measurement.

To get around this issue, and allow the user to prevent the fault signal from being latched by noise, a circuit was designed to slew the $\overline{\text{FAULT}}$ pin voltage based on the value of the capacitor from that pin to ground. Once the voltage on the pin falls below 2 V, as established by an internal reference, the fault output is latched and pulled to ground quickly with an internal N-channel MOSFET.

**Fault Walk-through**

The following walk-through references various sections and attributes in the figure below. This figure shows different fault set/reset scenarios and how they relate to the voltages on the $\overline{\text{FAULT}}$ pin, FAULT_EN pin, and the internal Overcurrent (OC) Fault node, which is invisible to the customer.

1. Because the device is enabled (FAULT_EN is high for a minimum period of time, the Fault Enable Delay, tFED , 15 µs typical) and there is an OC fault condition, the device $\overline{\text{FAULT}}$ pin

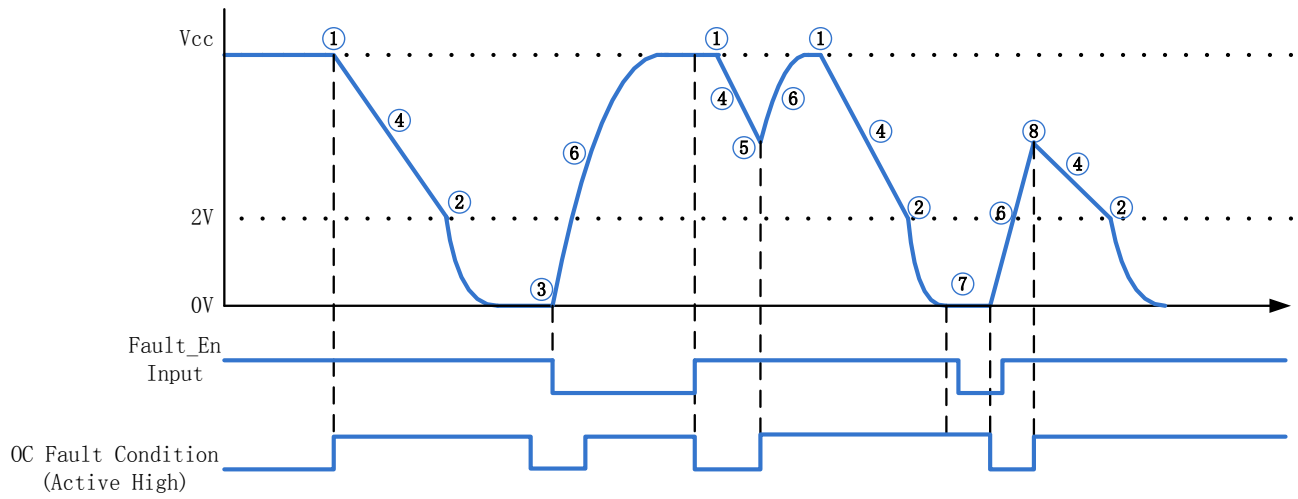
starts discharging.

2. When the $\overline{\text{FAULT}}$ pin voltage reaches approximately 2 V, the fault is latched, and an internal NMOS device pulls the $\overline{\text{FAULT}}$ pin voltage to approximately 0 V. The rate at which the $\overline{\text{FAULT}}$ pin slews downward (see [4] in the figure) is dependent on the external capacitor, $C_{OC}$, on the $\overline{\text{FAULT}}$ pin.
3. When the FAULT_EN pin is brought low, the $\overline{\text{FAULT}}$ pin starts resetting if no OC fault condition exists, and if FAULT_EN is low for a time period greater than $t_{OCH}$. The internal NMOS pull-down turns off and an internal PMOS pullup turns on (see [7] if the OC fault condition still exists).
4. The slope, and thus the delay to latch the fault is controlled by the capacitor, $C_{OC}$, placed on the $\overline{\text{FAULT}}$ pin to ground. During this portion of the fault (when the $\overline{\text{FAULT}}$ pin is between $V_{CC}$ and 2 V), there is a 3 mA constant current sink, which discharges $C_{OC}$. The length of the fault delay, t is equal to:

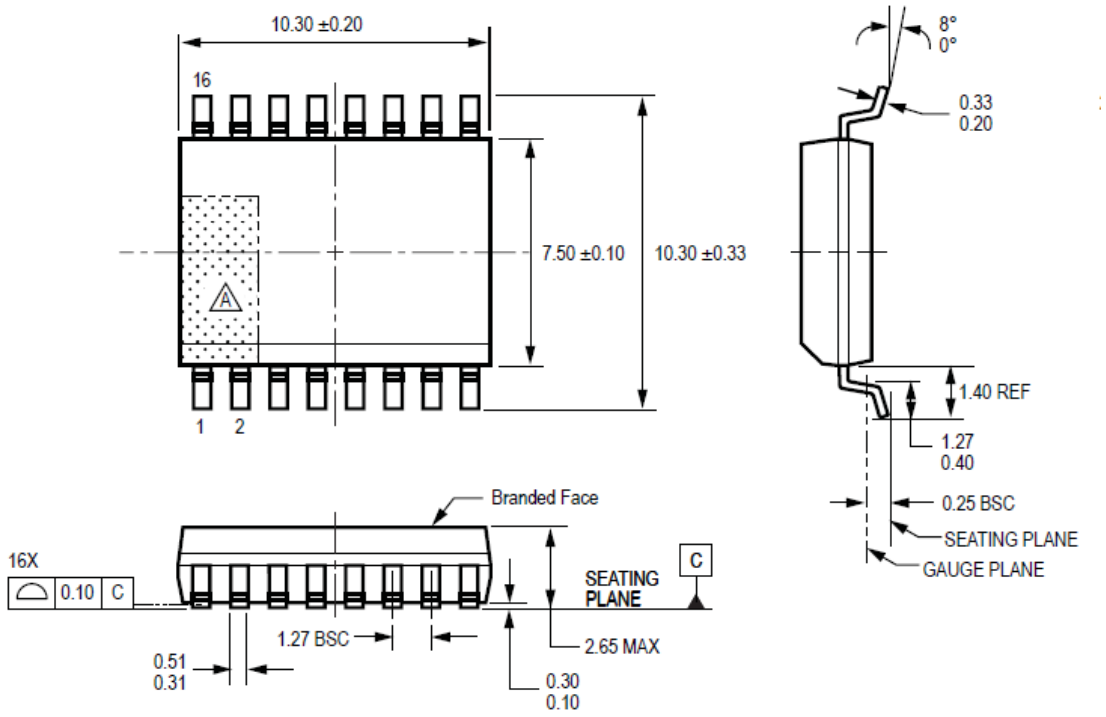
$$t = \frac{C_{OC} \times (V_{CC} - 2V)}{3mA}$$

where $V_{CC}$ is the device power supply voltage in volts, t is in seconds and $C_{OC}$ is in Farads. This formula is valid for $R_{PU}$ equal to or greater than 330 kΩ. For lower-value resistors, the current flowing through the $R_{PU}$ resistor during a fault event, IPU , will be larger. Therefore, the current discharging the capacitor would be 3 mA – IPU and equation 1 may not be valid.

5. The $\overline{\text{FAULT}}$ pin did not reach the 2 V latch point before the OC fault condition cleared. Because of this, the fixed 3 mA current sink turns off, and the internal PMOS pull-up turns on to recharge $C_{OC}$ through the $\overline{\text{FAULT}}$ pin.
6. This curve shows $V_{CC}$ charging external capacitor $C_{OC}$ through the internal PMOS pull-up. The slope is determined by $C_{OC}$.
7. When the FAULT_EN pin is brought low, if the fault condition still exists, the latched $\overline{\text{FAULT}}$ pin will be pulled low by the internal 3mA current source. When fault condition is removed then the Fault pin charges as shown in step 6.
8. At this point there is a fault condition, and the part is enabled before the $\overline{\text{FAULT}}$ pin can charge to $V_{CC}$. This shortens the user-set delay, so the fault is latched earlier. The new delay time can be calculated by equation 1, after substituting the voltage seen on the $\overline{\text{FAULT}}$ pin for $V_{CC}$.



## Package 16-pin SOICW




A Terminal #1 mark area

B Branding scale and appearance at supplier discretion

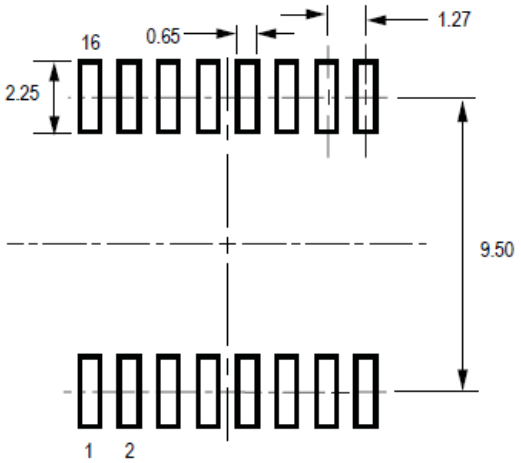
C Reference land pattern layout (reference IPC7351 SOIC127P600X175-8M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

**For Reference Only; not for tooling use (reference MS-013AA)**

**Dimensions in millimeters**

**Dimensions exclusive of mold flash, gate burrs, and dambar protrusions**

**Exact case and lead configuration at supplier discretion within limits shown**




C PCB Layout Reference View