SC16312(文件编号：S&CIC0208) 1/4 to 1/11 Duty VFD Controller

Features

- Logic voltage:5V
- High-voltage output:VDD-30Vmax
- Multiple display (11-segment & 11-digit to 16-segment &4-digit)
- 6×4 matrix key scanning
- 8 steps dimmer circuit
- 4 LED output ports
- 4-bit general purpose input port
- No external resistors necessary for driver output (provides PMOS open-drain and pull-low resistor output)
- Serial interface with MCU (CLK, CS, DI, DO)

Applications

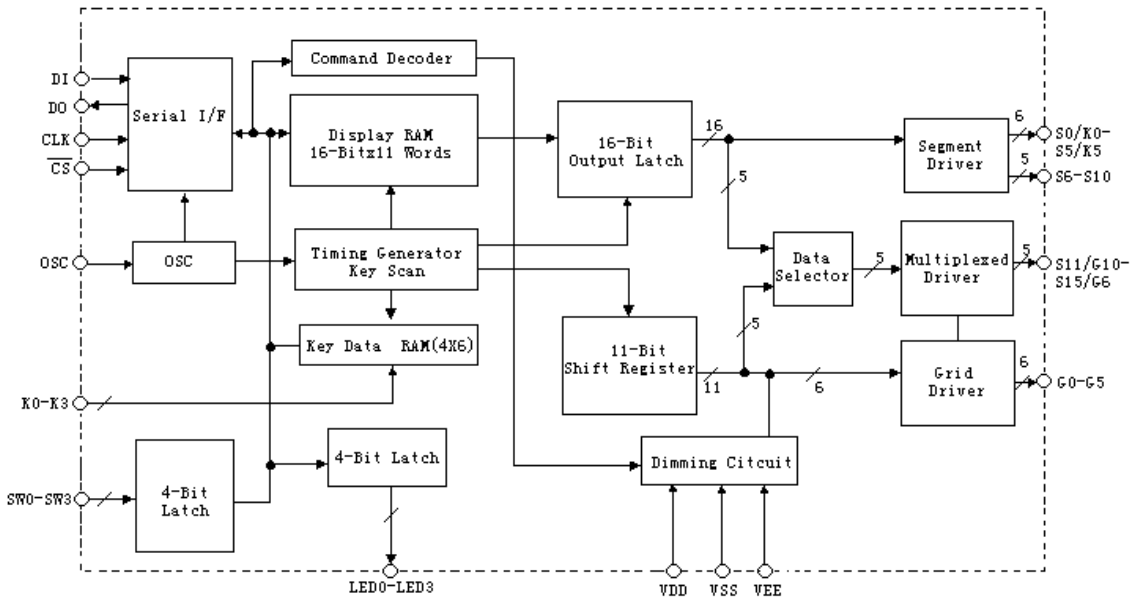
- Consumer products panel function control
- Other similar application panel function control
- Industrial measuring instrument panel unction control

General Description

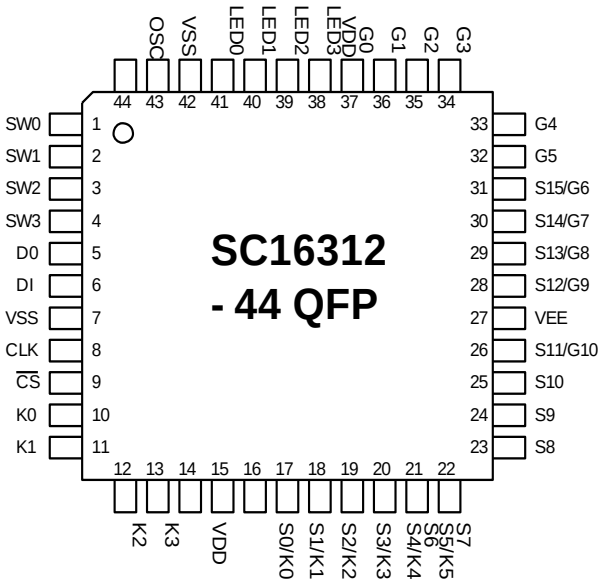
SC16312 is a VFD (Vacuum Fluorescent Display) controller driver that is driven on a 1/4 to 1/11 duty factor. It consists of 11 segment output lines, 6 grid output lines, 5 segment/grid output drives,4 LED output ports, a control circuit, a display memory, and a key scancircuit.

Serial data inputs to the SC16312 through a three-line serial interface. This VFD controller/driver is ideal as a peripheral device for an MCU.

Block Diagram



Pin Assignment

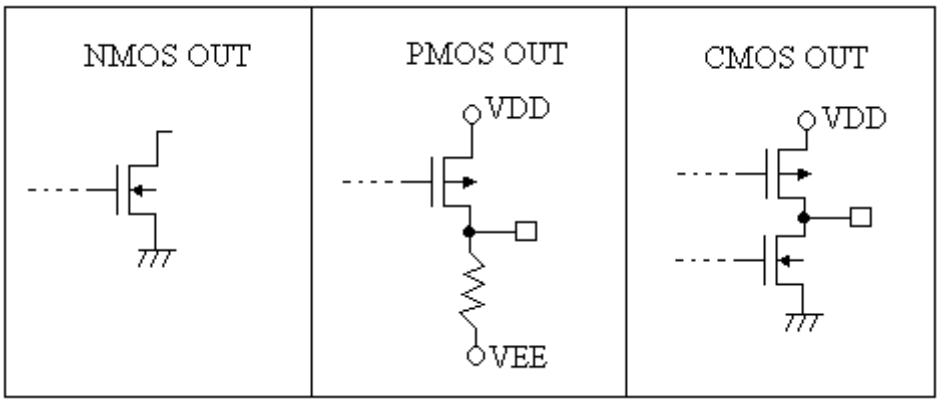


Pin Description

Pin No.	Pin Name	I/O	Description
1~4	SW0~SW3	I	4-bit general purpose input port
5	DO	O	Output serial data at the falling edge of the shift clock, Starting from low order bit. This is an NMOS open-drain Output pin.
6	DI	I	Input serial data at the rising edge of the shift clock, starting from the low order bit.
7,43	VSS	—	Power supply, ground
8	CLK	I	Reads serial data at the rising edge ,and outputs data at the Falling edge.
9	CS	I	Initializes serial interface at the rising or falling edge of the SC16312. Then it waits to receive a command. Data input After CS has fallen is processed as a command. While command data is processed, current processing is stopped, and the serial interface is initialized. While CS is high, CLK is ignored.
10 ~13	K0~K3	I	Keying data input to these pins is latched at the end of the display cycle.
14, 38	VDD	—	Posistive power supply
15~20	S0/K0~S5/K5	O	Segment or key source output pins (dual function). This is PMOS open-drain and pull-low resistor output.
21~25	S0/K0~S5/K5	O	Segment or key source output pins (dual function).This is PMOS open-drain and pull-low resistor output.
Pin No.	**Pin Name**	**I/O**	**Description**

26, 28~31	S11/G10~S15/G6	O	Segment or Grid driver output pins. These pins are selectable for segment or grid driving. This is PMOS open-drain and pull-low resistor output.
27	VEE	—	VFD power supply
37~32	G0~G5	O	Grid driver output pins (Grid only). This is PMOS open-drain and pull-low resistor output.
42~39	LED0~LED3	O	LED driver output ports. This is a CMOS output pin
44	OSC	I	Connected to an external resistor or an RC oscillator circuit.

Approximate internal connections



Absolute Maximum Ratings

Supply Voltage ---------- -0.3v to 5.5v
Input Voltage ---------- vss-0.3v to VDD+0.3v
Operating Temperature ---------- -25℃ to 75℃
Storage Temperature ---------- -50℃ to 125℃

Note: These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Function of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D. C. Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD	Conditions				
VDD	Logic Supply Voltage	-	-	4.5	5	5.5	V
VEE	VFD Supply Voltage	-	-	0	-	VDD-30	V
fOSC	Output Pull-low Resistor	5V	ROSS=51kΩ	350	500	650	KHz
RPL	Output Pull-low Resistor	5V	Driver output	50	100	150	KΩ
IDD	Operating Current	5V	No load, VFD display off	-	-	5	MA
IOL	Driver Leakage Current	5V	Vo=VDD-30V VFD driver off	-	-	-10	UA
IOL1	LED Sink Current	5V	VOL=1V LED0~LED3	20	-	-	mA
IOH1	LED Source Current	5V	VOH=0.9VDD LED0~LED3	-1	-	-	mA
IOH21	Segment/Key Source Current	5V	VOH=VDD-2V S0/K0~S5/K5, S6~S10	-3	-	-	mA
IoH22	Segment/Grid Source Current	5V	VoH=VDD-2V G0~G5, S11/G10~S1/G6	-15	-	-	mA
IoL3	DO Sink Current	5V	VOL=0.4V	4	-	-	mA
VIH	“H” Input Voltage	-	-	0.7VDD	-	VDD	V
VIL	“L” Input Voltage	-	-	0	-	0.3VDD	V
VoH1	High-level Output Voltage	5V	LED0~LED3, IoH1=-1mA	0.9VDD	-	VDD	V
VoL1	Low-level Output Voltage	5V	LED0~LED3, IoL1=20MA	0	-	1	V
VoL2	Low-level Output Voltage	5V	DO, IOL2=4mA	0	-	0.4	V

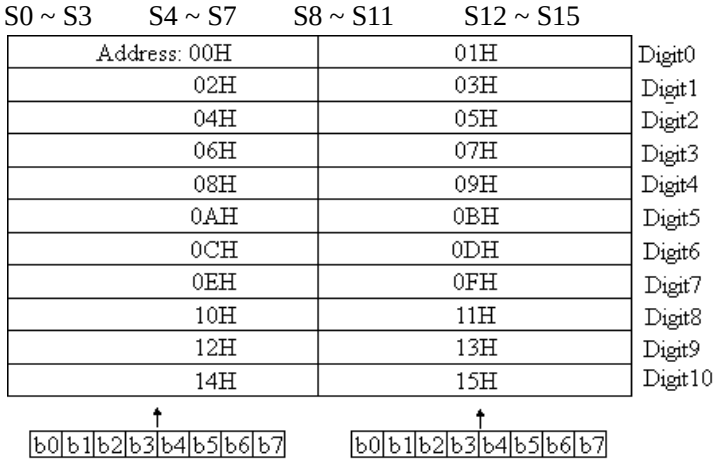
A. C. Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		VDD	Conditions				
tPHL	Propagation Delay Time	5V	CL→DO	-	-	300	ns
tPLH		5V	CL=15pF,RL=10kΩ	-	-	100	ns
tr1	Rise TIme	5V	CL=300PF, S0~S10	-	-	2	us
Tr2		5V	CL=300PF, Go~G5, S11/G10~S15/G6	-	-	0.5	us
tf	Fall Time	5V	CL=300pF, Sn, Gn	-	-	120	us
tmax	Maximum Clock Frequency	5V	Duty=50%	1	-	-	MHz
Ci	Input Capacitance	5V	-	-	-	15	pF
tcw	Clock Pulse Width	5V	-	400	-	-	ns
tsw	Strobe Pulse Width	5V	-	1	-	-	ns
tSU	Data Setup Time	5V	-	100	-	-	ns
th	Data Hold Time	5V	-	100	-	-	ns
tcs	Clock-Strobe Time	5V	CLK rising edge to CS rising edge	1	-	-	us
tw	Wait Time	5V	CLK rising edge to CS rising edge	1	-	-	us

Functional Description

Display RAM and display mode

The static display RAM is organized into 22×8 bits and stores the data transmitted from an external device to the SC16312 through a serial interface. The contents of the RAM are directly mapped to the contents of the VFD driver. Data in the RAM can be accessed through the data setting, address setting and display control commands. It is assigned addresses in 8-bitunit as follows:



Dimming Control

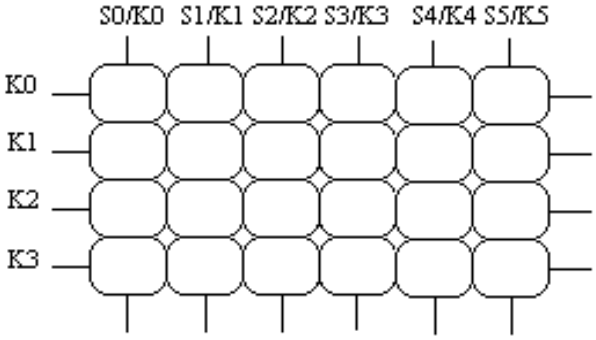
SC16312 porvides 8-step dimmer function on display by controlling the 3-bit binary command code. The full pulse width of grid signal is divides into 16 uniform sections by PWM(pulse width modulation)technology.

The 16 uniform sections available form 8 steps dimmer via 3-bit binary code. The 8-step dimmer includes 1/16, 2/16, 4/16, 10/16, 11/16, 12/16, 13/16, and 14/16. The 1/16 pulse width indicates minimum lightness. The 14/16 pulse width represents maximum lightness. The 14/16 pulse width represents maximum lightness. (Refer to the display control command).

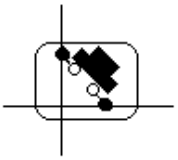
Key matrix and key-input data storage RAM

The key matrix scans the series key states at each level of the key strobe signal (S0/K0~S5/K5)output of the :SC16312. The key strobe signal outputs are time-multiplexed signals from S0/K0~S5/K5. The states of inputs K0~K3 are sampled by strobe signal S0/K0~S5/K5 and latched into the register.

The key matrix is made up of a 6x4 matrix, as shown below.

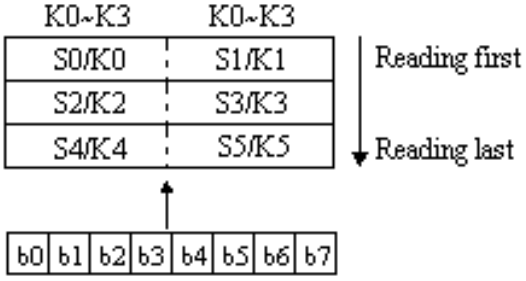


Detail



Key matrix

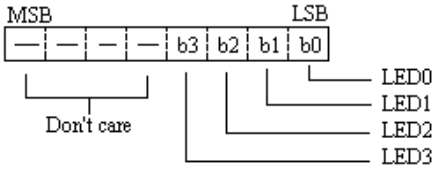
The data of each key is stored as illustrated below. And is read with the read command, starting form the least significant bit.



LED port

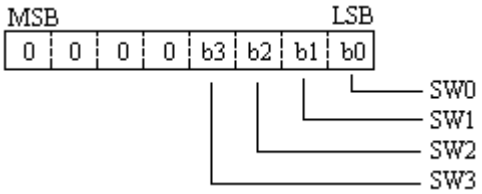
The LED port belongs to the CMOS output configuration.

Data is written to the LED port with the write command, starting from the least port's least significant bit. In out application (see application circuits). The user adopts an internal NMOS device to a driver LED component by connecting VDD. When a bit of this port is 0, the corresponding LED lights; when the bit is 1,the LED turns off. The data of bits 5 through 8 are ignored.



SW data

SC16312 provides an extra 4-bit general input port. The SW data is provided with available binary code. The SW data is read with the read command. Starting from the least significant bit. Bits 5 through 8 of the SW data are 0.



Commands

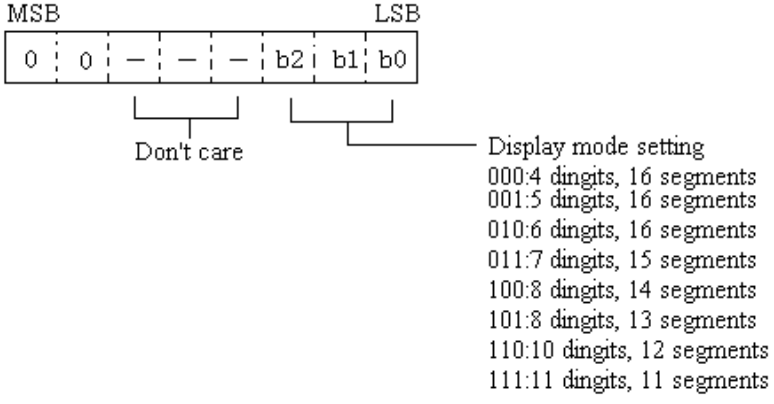
Commands set the display mode and status of the VFD driver.

The first 1 byte input to the SC16312 through the DI pin after the $\overline{CS}$ pin has fallen, is regarded as a command. If $\overline{CS}$ is set high while commands/data are transmitted. Serial communication is initialized, and the commands/data being transmitted are not valid (however, the commands/data previously transmitted remains valid).

• Display mode setting commands

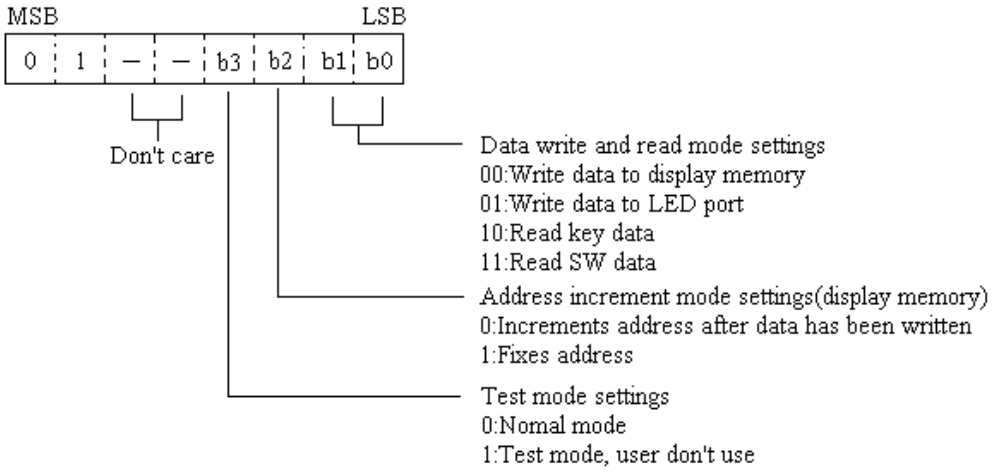
These commands initialize the SC16312 and select the number of segments and the number of grids (1/4~1/11 duty, 11 segments to 16 segments).

When these commands are executed, the display is forcibly turned off, and key scanning is selected, nothing happens.



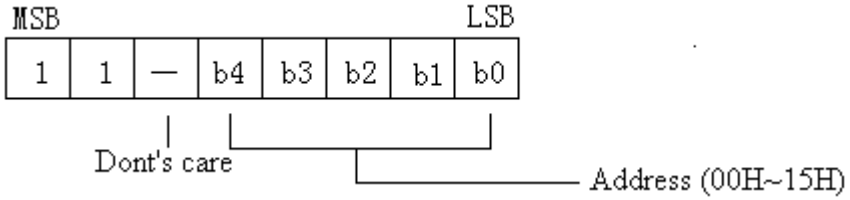
• Data setting commands

These commands set the data write and data read modes.



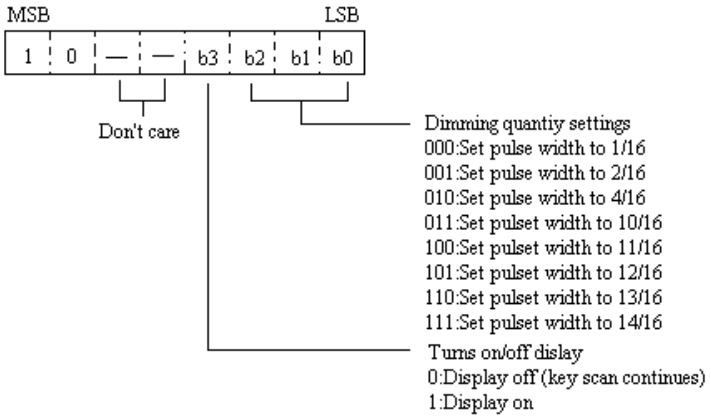
• Address setting commands

These commands set the address of the display memory.

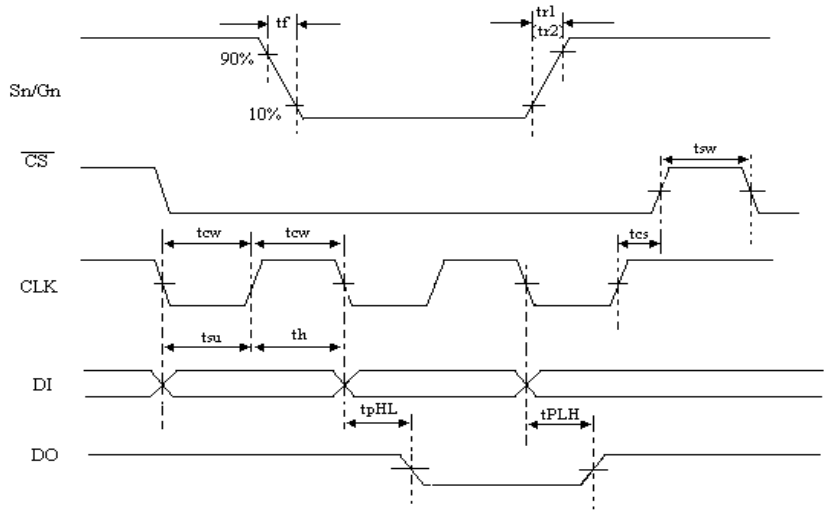


If address 16H or higher is set, data is ignored until a valid address is set.

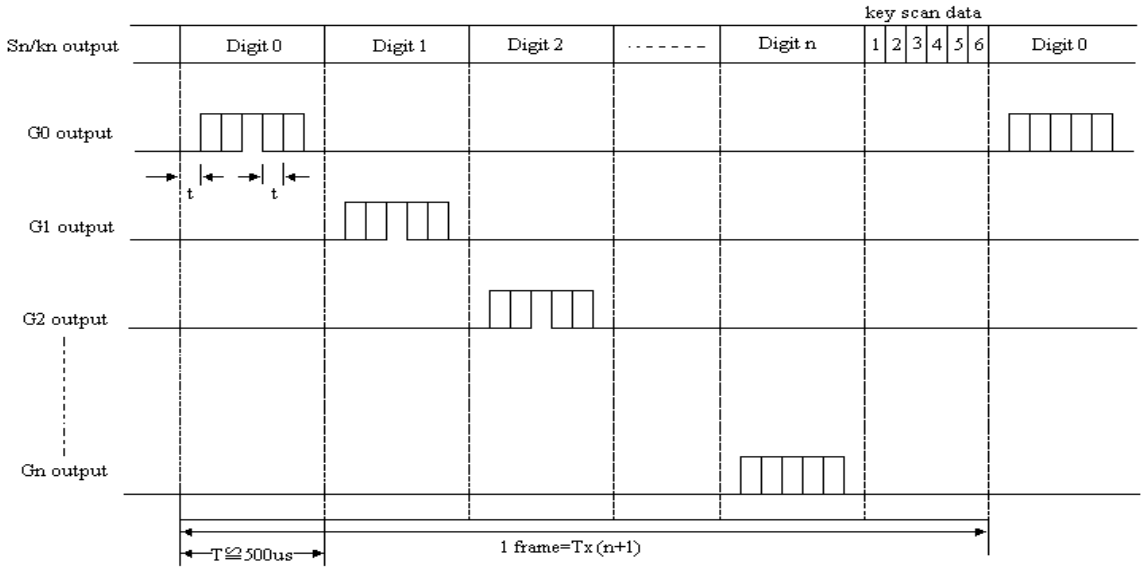
• Display control commands



Timing Diagrams



Key scanning and display timing



Note: n=0~5

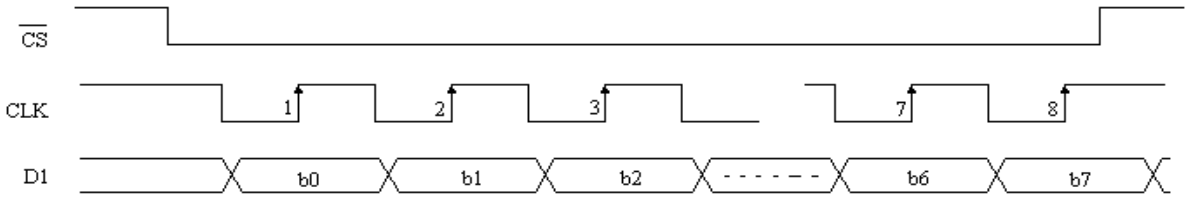
T=1/16T

T: pulse width of segment signal is decided by oscillator frequency

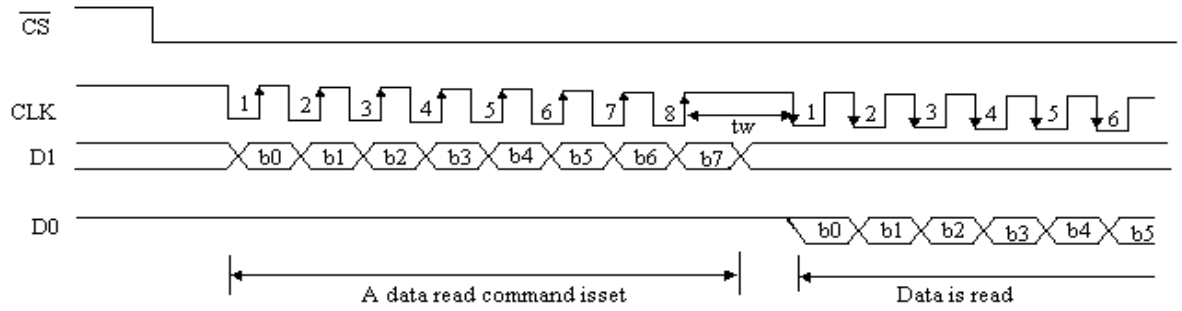
One cycle of key scanning consists of one frame.

Serial communication format

Reception (command/data write)

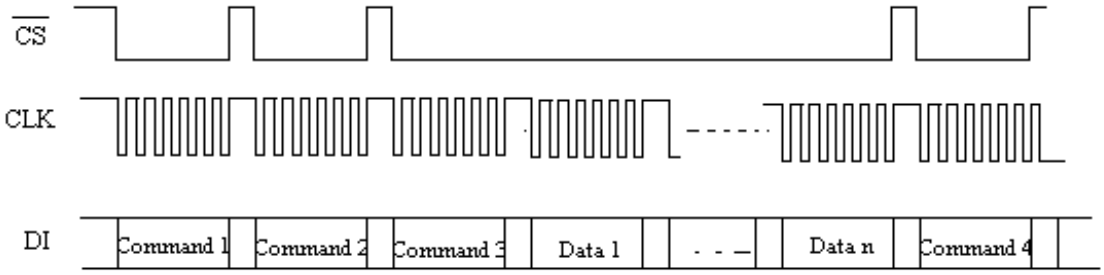


Transmission (data read)



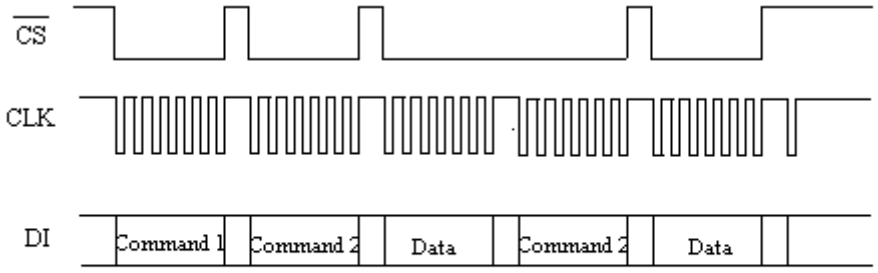
DO must be sure to connect an external pull-high resistor to this pin (1kΩ to 10kΩ).
Note: When data is read, a wait time "tw" of 1 μs is necessary.

Updating display memory by incrementing address



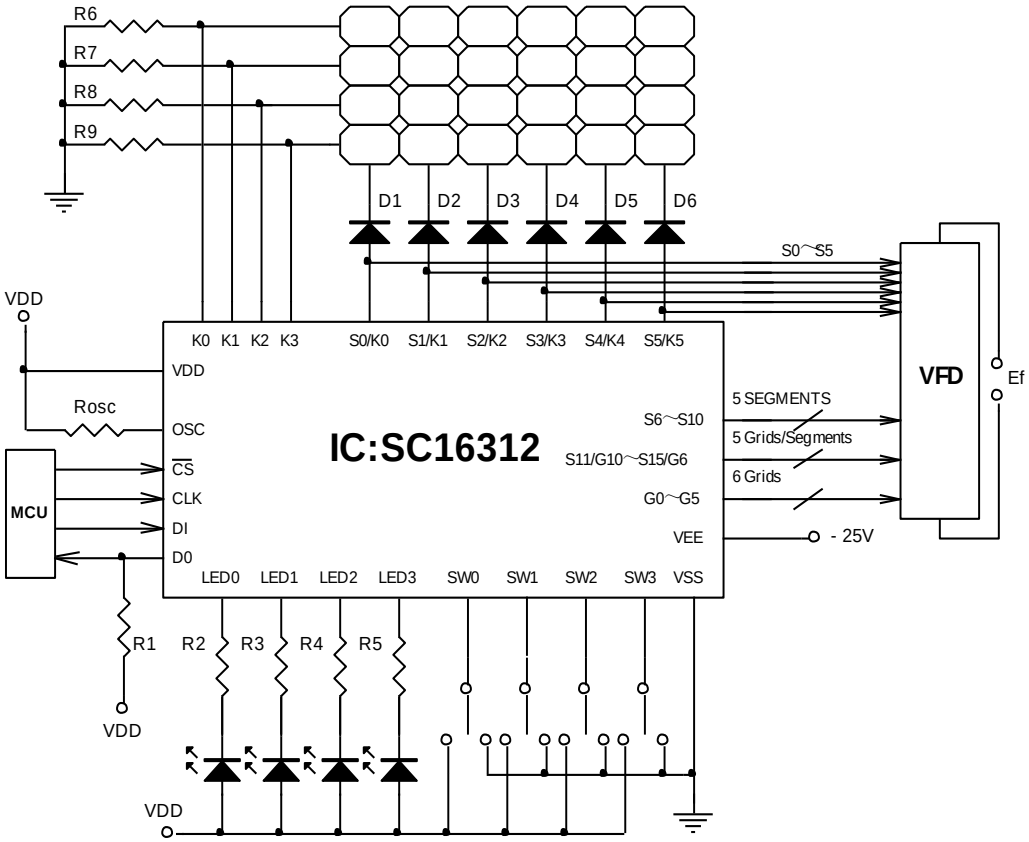
Command 1:sets display mode
Command 2:sets data
Command 3:sets address
Data 1 to n:transfers display data (22 bytes max.)
Command 4:controls diplay

Updating specific addresses



Command 1:sets data
Command 2:sets address
Data: display data

Application Circuits



Note: Rosc=51kΩ for oscillator resistor

R1=1~10 kΩ for external pull-high resistor

R2~R5=750 Ω ~1.2 Ω

R6~R9=10 kΩ for external pull-low resistor

D1~D6=1N4001

Ef=Fiament voltage for VFD