SAM R30 Summary

IEEE 802.15.4 Sub-GHz System-in-Package Summary Datasheet

Introduction

The SAM R30 is a series of Ultra low-power microcontrollers equipped with an IEEE® 802.15.4-2003/2006/2011 compliant RF interface for the sub-1GHz frequency bands such as 780 MHz (China), 868 MHz (Europe) and 915 MHz (North America). It uses the 32-bit ARM® Cortex®-M0+ processor at max. 48MHz (2.46 CoreMark®/MHz) and offers 256KB of Flash and 40KB of SRAM in both 32- and 48-pin packages. Sophisticated power management technologies, such as power domain gating, SleepWalking, Ultra low-power peripherals and more, allow for very low current consumptions.

The highly configurable peripherals include a touch controller supporting capacitive interfaces with proximity sensing. The sub-GHz RF interface supports BPSK and O-QPSK modulation schemes according to the IEEE standard and offers output power values of more than +8dBm and receiver sensitivities below -108 dBm.

Features

- Processor
  - ARM Cortex-M0+ CPU running at up to 48MHz
    - Single-cycle hardware multiplier
    - Micro Trace Buffer (MTB)
- Memories
  - 256KB in-system self-programmable Flash
  - 32KB SRAM
  - 8KB low power RAM
- System
  - Power-on reset (POR) and brown-out detection (BOD)
  - Internal and external clock options with 48MHz Digital Frequency Locked Loop (DFLL48M) and 48MHz to 96MHz Fractional Digital Phase Locked Loop (FDPLL96M)
  - External Interrupt Controller (EIC)
  - Up to 15 external interrupts
  - One non-maskable interrupt
  - Two-pin Serial Wire Debug (SWD) programming, test and debugging interface
- Low Power
  - Idle and standby sleep modes
  - SleepWalking peripherals
- Integrated Ultra Low Power Transceiver for 700/800/900MHz ISM Band:
  - Chinese WPAN band from 779 to 787MHz

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  - European SRD band from 863 to 870MHz
  - North American ISM band from 902 to 928MHz
  - Japanese band from 915 to 930MHz
- Direct Sequence Spread Spectrum with different modulation and data rates:
  - BPSK with 20 and 40kb/s, compliant to IEEE® 802.15.4-2003/2006/2011
  - O-QPSK with 100 and 250kb/s, compliant to IEEE 802.15.4-2006/2011
  - O-QPSK with 250kb/s, compliant to IEEE 802.15.4-2011
  - O-QPSK with 200, 400, 500, and 1000kb/s PSDU data rate
  - Industry leading link budget:
    - RX Sensitivity up to -110 dBm
    - TX Output Power up to +11 dBm
  - Hardware Assisted MAC
    - Auto-Acknowledge
    - Auto-Retry
    - CSMA-CA and Listen Before Talk (LBT)
    - Automatic address filtering and automated FCS check
  - Special IEEE 802.15.4™-2011 hardware support:
    - FCS computation and Clear Channel Assessment
    - RSSI measurement, Energy Detection and Link Quality Indication
  - Antenna Diversity and PA/LNA Control
  - 128 Byte TX/RX Frame Buffer
  - Integrated 16MHz Crystal Oscillator (external crystal needed)
  - Fully integrated, fast settling Transceiver PLL to support Frequency Hopping
  - Hardware Security (AES, True Random Generator)
- Peripherals
  - 12-channel Direct Memory Access Controller (DMAC)
  - 12-channel Event System
  - Up to three 16-bit Timer/Counters (TC), configurable as either:
    - One 16-bit TC with compare/capture channels
    - One 8-bit TC with compare/capture channels
    - One 32-bit TC with compare/capture channels, by using two TCs
  - Three 16-bit Timer/Counters for Control (TCC), with extended functions:
    - Up to four compare channels with optional complementary output
    - Generation of synchronized pulse width modulation (PWM) pattern across port pins
    - Deterministic fault protection, fast decay and configurable dead-time between complementary output
    - Dithering that increase resolution with up to 5 bit and reduce quantization error
  - 32-bit Real Time Counter (RTC) with clock/calendar function
  - Watchdog Timer (WDT)
  - CRC-32 generator
  - One full-speed (12Mbps) Universal Serial Bus (USB) 2.0 interface
    - Embedded host and device function
    - Eight endpoints

  - Up to five Serial Communication Interfaces (SERCOM), each configurable to operate as either:
    - USART with full-duplex and single-wire half-duplex configuration
    - I^2C up to 3.4MHz
    - SPI
    - LIN slave
  - One 12-bit, 350ksps Analog-to-Digital Converter (ADC) with up to eight external channels
    - Differential and single-ended input
    - 1/2x to 16x programmable gain stage
    - Automatic offset and gain error compensation
    - Oversampling and decimation in hardware to support 13-, 14-, 15- or 16-bit resolution
  - Two Analog Comparators (AC) with window compare function
  - Peripheral Touch Controller (PTC)
    - 48-Channel capacitive touch and proximity sensing
- I/O and Package
  - 16/28 programmable I/O pins
  - 32-pin and 48-pin QFN
- Operating Voltage
  - 1.8V – 3.6V
- Temperature Range
  - -40°C to 85°C Industrial
- Power Consumption
  - Transceiver with microcontroller in idle mode (TX output power +5dBm):
    - RX_ON = 9.4mA
    - BUSY_TX = 18.2mA
  - Active mode for the microcontroller down to 60µA/MHz
  - Standby mode for the microcontroller down to 1.4µA/MHz

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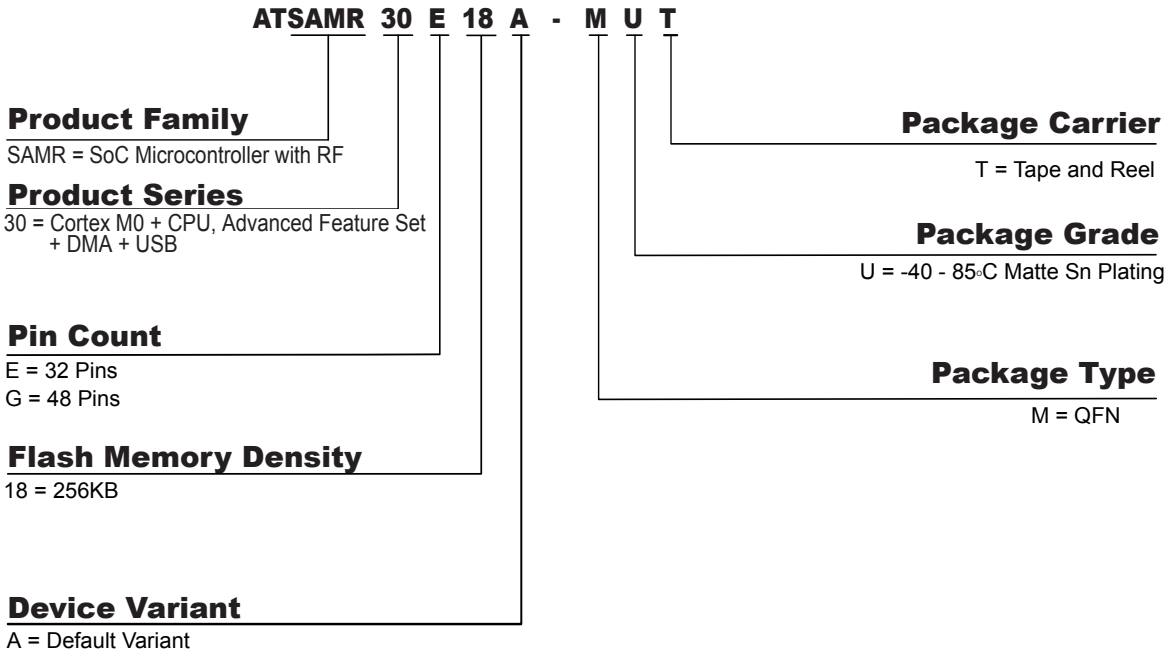
1. Configuration Summary

	SAM R30G	SAM R30E
Pins	48	32
General Purpose I/O-pins (GPIOs)	28	16
Flash	256KB	256KB
Flash RWW section	8KB	8KB
System SRAM	32KB	32KB
Low Power SRAM	8KB	8KB
Timer Counter (TC) instances	3	2
Waveform output channels per TC instance	2	2
Timer Counter for Control (TCC) instances	3	3
Waveform output channels per TCC	4/2/2	4/2/2
USB interface	1	1
Serial Communication Interface (SERCOM) instances	5+1 (1)	4+1 (1)
Inter-IC Sound (I²S) interface	No	No
Analog-to-Digital Converter (ADC) channels	8	4
Analog Comparators (AC)	2	2
Digital-to-Analog Converter (DAC) channels	No	No
Real-Time Counter (RTC)	Yes	Yes
RTC alarms	1	1
RTC compare values	1 32-bit value or 2 16-bit values	1 32-bit value or 2 16-bit values
External Interrupt lines	15	14
Peripheral Touch Controller (PTC) X and Y lines	8x6	6x2
Maximum CPU frequency	48MHz	
Packages	QFN	QFN
32.768kHz crystal oscillator (XOSC32K)	Yes	No
Oscillators	16MHz crystal oscillator for TRX (XOSCRF) 0.4-32MHz crystal oscillator (XOSC) 32.768kHzinternal oscillator (OSC32K) 32kHz ultra-low-power internal oscillator (OSCULP32K)	

	SAM R30G	SAM R30E
	8MHz high-accuracy internal oscillator (OSC8M) 48MHz Digital Frequency Locked Loop (DFLL48M) 96MHz Fractional Digital Phased Locked Loop (FDPLL96)	
Event System channels	12	12
SW Debug Interface	Yes	Yes
Watchdog Timer (WDT)	Yes	Yes

1. SERCOM4 is internally connected to the AT86RF212B.

2. Ordering Information



2.1 SAM R30E

Table 2-1. SAM R30E

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMR30E18A-MU	256K	32K	QFN32	Tray
ATSAMR30E18A-MUT	256K	32K	QFN32	Tape & Reel

2.2 SAM R30G

Table 2-2. SAM R30G

Ordering Code	FLASH (bytes)	SRAM (bytes)	Package	Carrier Type
ATSAMR30G18A-MU	256K	32K	QFN48	Tray
ATSAMR30G18A-MUT	256K	32K	QFN48	Tape & Reel

2.3 Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The SAM R30 variants have a reset value of DID=0x1081drxx, with the LSB identifying the die number ('d'), the die revision ('r') and the device selection ('xx').

Table 2-3. SAM R30 Device Identification Values

DEVSEL (DID[7:0])	Device
0x1081021E	SAM R30G18A
0x1081021F	SAM R30E18A

Note: The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

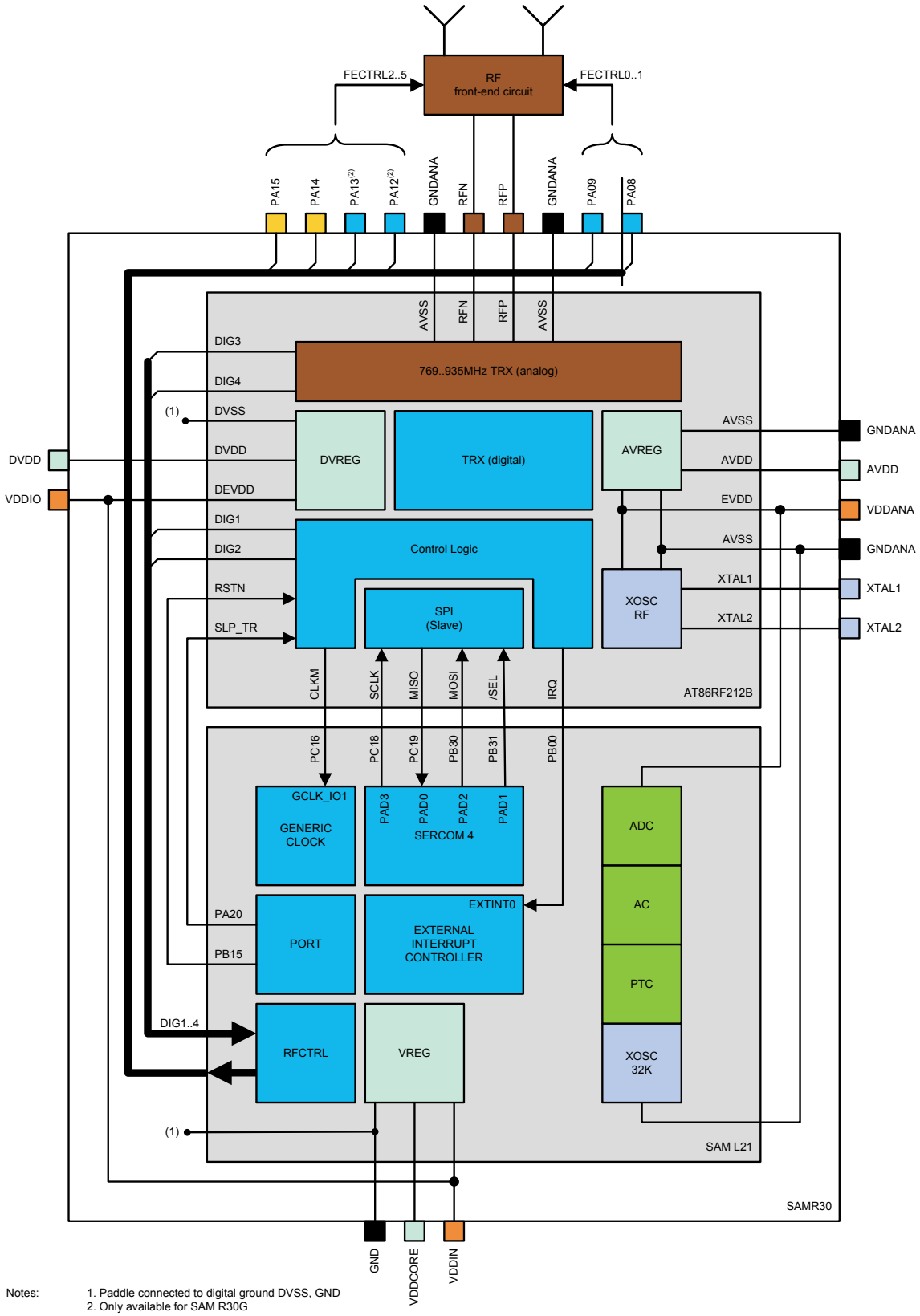
3. System Introduction

The SAM R30 SIP consists of two vertically integrated silicon dies:

- SAM L21 ARM® Cortex® M0+ based microcontroller.
- AT86RF212B low-power, low-voltage 700/800/900MHz transceiver

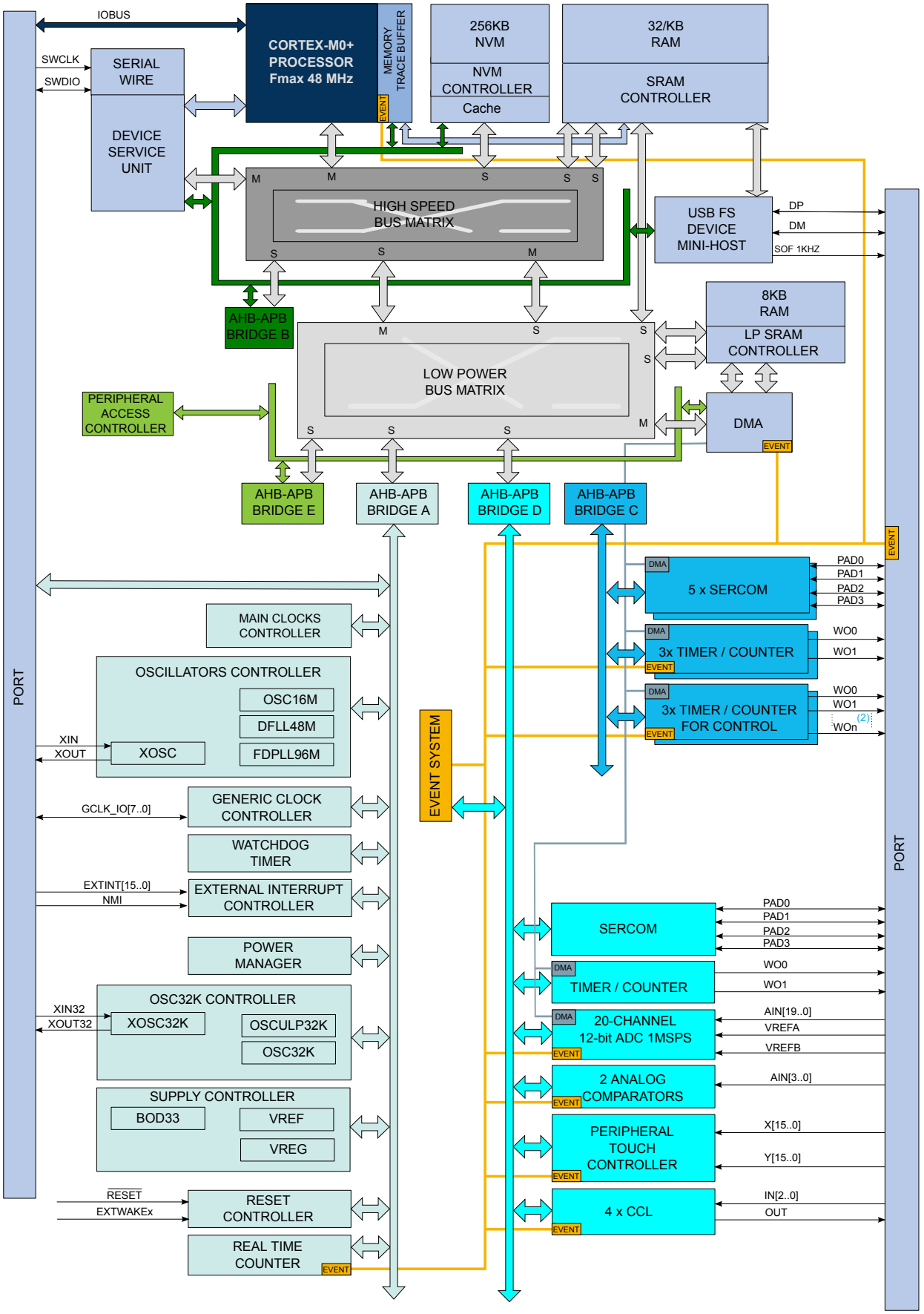
The local communication and control interface is wired within the package. Key I/O external signals are exposed as I/O pins. .

3.1 Interconnection Diagram



Notes:
1. Paddle connected to digital ground DVSS, GND
2. Only available for SAM R30G

3.2 MCU Block Diagram



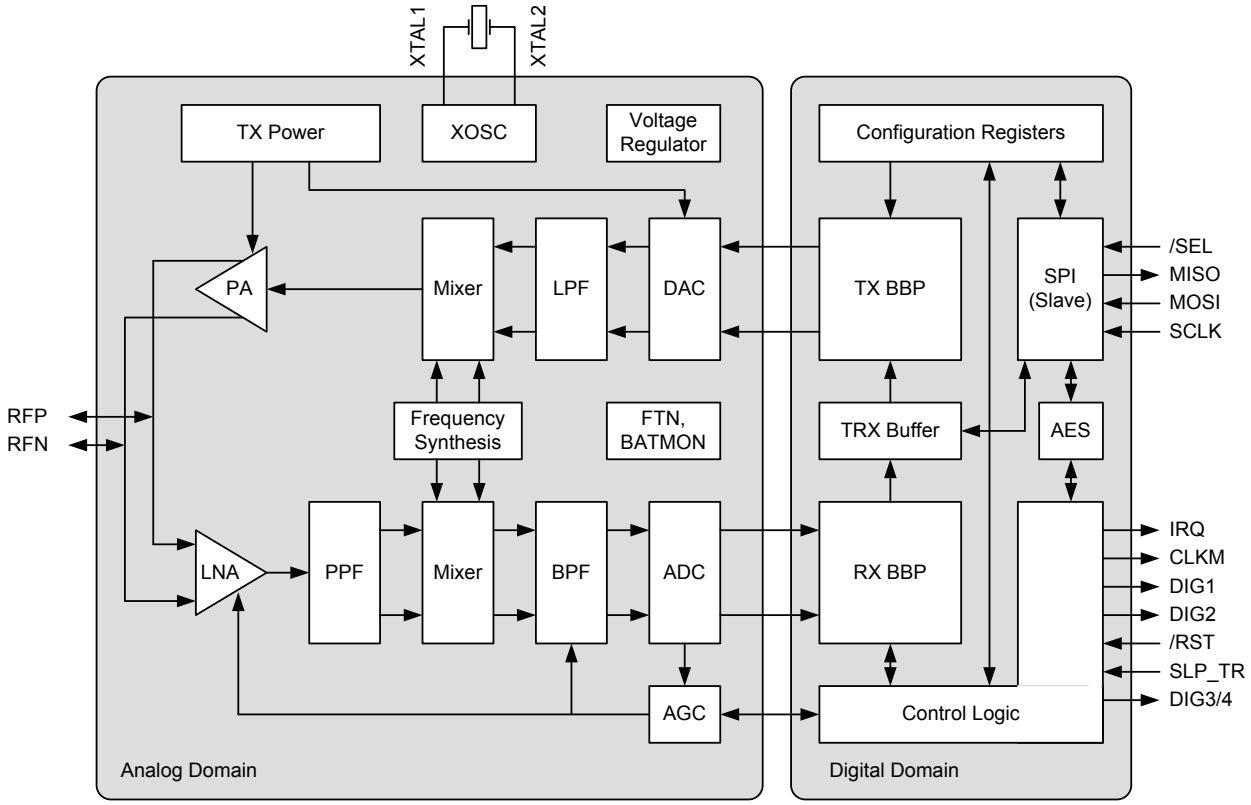
Note:

1. Some products have different number of SERCOM instances, Timer/Counter instances, PTC signals and ADC signals.
2. The three TCC instances have different configurations, including the number of Waveform Output (WO) lines.

3.3 Transceiver Circuit Description

The AT86RF212B single-chip radio transceiver provides a complete radio transceiver interface between radio frequency signals and baseband microcontroller. It comprises a bidirectional analog RF front end, direct-conversion mixers, low-noise fractional-n PLL, quadrature digitizer, DSP modem and baseband packet-handler optimized for IEEE 802.15.4 MAC/PHY automation and low-power. An SPI accessible 128-byte TRX buffer stores receive or transmit data. Radio communication between transmitter and receiver is based on DSSS Spread Spectrum with OQPSK or BPSK modulation schemes as defined by the IEEE 802.15.4 standard. Additional proprietary modulation modes include high-data rate payload encoding and wideband BPSK-40-ALT.

Figure 3-1. AT86RF212B Block Diagram



The number of required external components is minimal. The basic requirements are an antenna, a balun, harmonic filter, local oscillator and bypass capacitors. The RF Ports are bidirectional 100Ω differential signals that do not require external TX/RX switches. Hardware control signals are automatically generated for TX/RX arbitration of high-powered PA/LNA frontends and transmitter diversity for systems with dual antennas.

The AT86RF212B supports the IEEE 802.15.4-2006 [2] standard mandatory BPSK modulation and optional O-QPSK modulation in the 868.3MHz and 915MHz bands. In addition, it supports the O-QPSK modulation defined in IEEE 802.15.4-2011 [4] for the Chinese 780MHz band. For applications not targeting IEEE compliant networks, the radio transceiver supports proprietary High Data Rate Modes

based on O-QPSK. Additionally the AT86RF212B provides BPSK-40-ALT wideband BPSK mode for compliance with FCC rule 15.247 and backward compatibility with legacy BPSK networks.

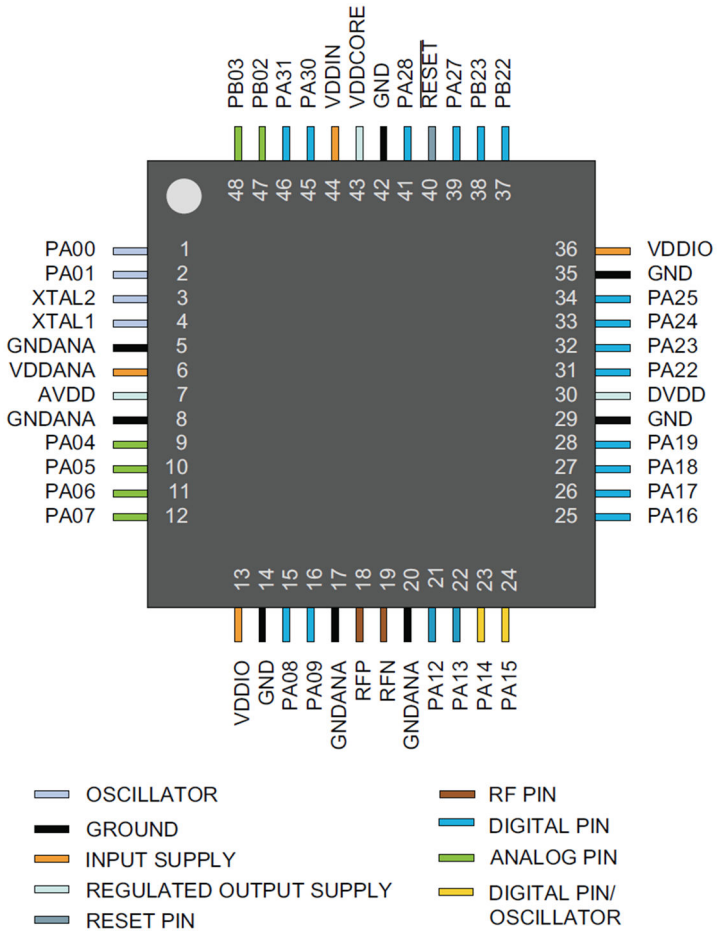
The AT86RF212B features hardware supported 128-bit security operation. The standalone AES encryption/decryption engine can be accessed in parallel to all PHY operational modes. Configuration of the AT86RF212B, reading and writing of data memory, as well as the AES hardware engine are controlled by the SPI interface and additional control signals.

On-chip low-dropout linear regulators provide clean 1.8 V_{DC} power for critical analog and digital sub-systems. To conserve power, these rails are automatically sequenced by the transceiver's state machine. This feature greatly improves EMC in the RF domain and reduces external power supply complexity to the simple addition of frequency compensation capacitors on the AVDD and DVDD pins.

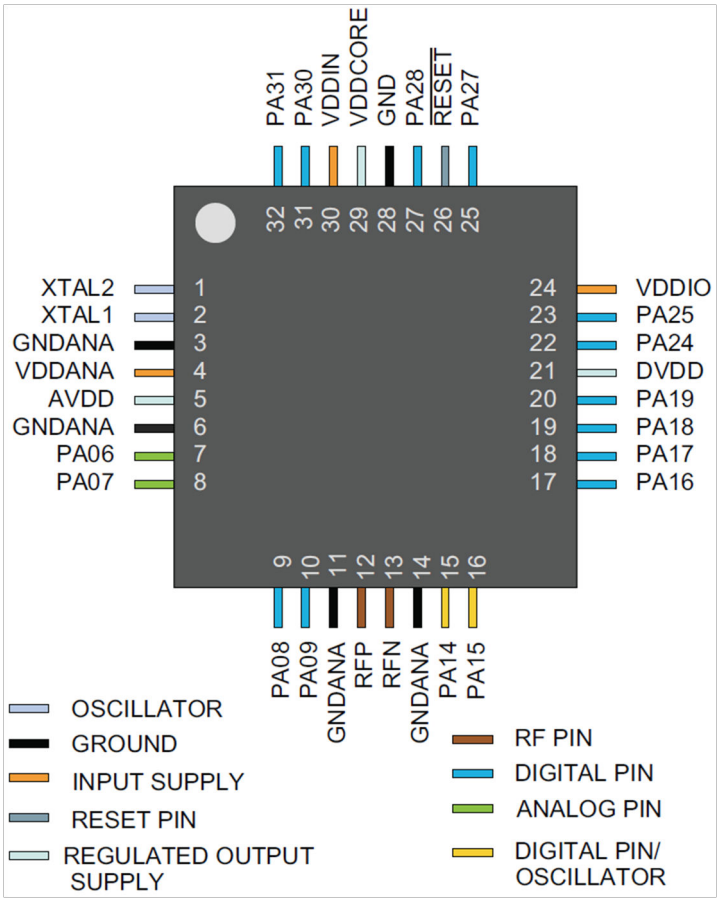
Additional features of the Extended Feature Set are provided to simplify the interaction between radio transceiver and microcontroller.

4. Pinout

4.1 SAM R30G



4.2 SAM R30E


PA31
PA30
VDDIN
VDDCORE
GND
PA28
RESET
PA27
32
31
30
29
28
27
26
25
XTAL2 1
XTAL1 2
GNDANA 3
VDDANA 4
AVDD 5
GNDANA 6
PA06 7
PA07 8
24 VDDIO
23 PA25
22 PA24
21 DVDD
20 PA19
19 PA18
18 PA17
17 PA16
9
10
11
12
13
14
15
16
PA08
PA09
GNDANA
RFP
RFN
GNDANA
PA14
PA15
OSCILLATOR
GROUND
INPUT SUPPLY
RESET PIN
REGULATED OUTPUT SUPPLY
RF PIN
DIGITAL PIN
ANALOG PIN
DIGITAL PIN/ OSCILLATOR

5. Signal Description

The following table gives details on signal names classified by peripheral.

Table 5-1. Signal Descriptions List

Signal Name	Function	Type	Active Level
Analog Comparators - AC			
AIN[3:0]	AC Analog Inputs	Analog	
CMP[1:0]	AC Comparator Outputs	Digital	
Analog Digital Converter - ADC			
AIN[19:0]	ADC Analog Inputs	Analog	
VREFB	ADC Voltage External Reference B	Analog	
External Interrupt Controller - EIC			
EXTINT[15:0]	External Interrupts inputs	Digital	
NMI	External Non-Maskable Interrupt input	Digital	
Reset Controller - RSTC			
EXTWAKE[7:0]	External wake-up inputs	Digital	
Generic Clock Generator - GCLK			
GCLK_IO[7:0]	Generic Clock (source clock inputs or generic clock generator output)	Digital	
Custom Control Logic - CCL			
IN[11:0]	Logic Inputs	Digital	
OUT[3:0]	Logic Outputs	Digital	
Supply Controller - SUPC			
VBAT	External battery supply Inputs	Analog	
PSOK	Main Power Supply OK input	Digital	
OUT[1:0]	Logic Outputs	Digital	
Power Manager - PM			
RESETN	Reset input	Digital	Low
Serial Communication Interface - SERCOMx			
PAD[3:0]	SERCOM Inputs/Outputs Pads	Digital	
Oscillators Control - OSCCTRL			
XIN	Crystal or external clock Input	Analog/Digital	

Signal Name	Function	Type	Active Level
XOUT	Crystal Output	Analog	
32KHz Oscillators Control - OSC32KCTRL			
XIN32	32KHz Crystal or external clock Input	Analog/Digital	
XOUT32	32KHz Crystal Output	Analog	
Timer Counter - TCx			
WO[1:0]	Waveform Outputs	Digital	
Timer Counter - TCCx			
WO[7:0]	Waveform Outputs	Digital	
Peripheral Touch Controller - PTC			
X[15:0]	PTC Input	Analog	
Y[15:0]	PTC Input	Analog	
General Purpose I/O - PORT			
PA01 - PA00	Parallel I/O Controller I/O Port A	Digital	
PA09 - PA04	Parallel I/O Controller I/O Port A	Digital	
PA19 - PA12	Parallel I/O Controller I/O Port A	Digital	
PA25 - PA22	Parallel I/O Controller I/O Port A	Digital	
PA28 - PA27	Parallel I/O Controller I/O Port A	Digital	
PA03 - PB02	Parallel I/O Controller I/O Port B	Digital	
PA23 - PB22	Parallel I/O Controller I/O Port B	Digital	
Universal Serial Bus - USB			
DP	DP for USB	Digital	
DM	DM for USB	Digital	
SOF 1kHz	USB Start of Frame	Digital	

6. I/O Multiplexing and Considerations

6.1 Multiplexed Signals

Each pin is by default controlled by the PORT as a general purpose I/O and alternatively it can be assigned to one of the peripheral functions A, B, C, D, E, F, G, H or I. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0..31) in the PORT must be written to '1'. The selection of peripheral function A to H is done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) in the PORT.

This table describes the peripheral signals multiplexed to the PORT I/O pins.

Table 6-1. Port Function Multiplexing

PIN		I/O Pin	Supply	A		B[1][2]					C	D	E	F	G	H	I
SAMR30E	SAMR30G			EIC	RSTC	AC	ADC	REF	PTC X-lines	PTC Y-lines	SERCOM[1][2]	SERCOM-ALT	TC/ TCC	TCC	COM	AC/ GCLK/ SUPC	CCL
	1	PA00	VSWOUT	EXTINT[0]	EXTWAKE[0]							SERCOM1/ PAD[0]	TCC2/ WO[0]				
	2	PA01	VSWOUT	EXTINT[1]	EXTWAKE[1]							SERCOM1/ PAD[1]	TCC2/ WO[1]				
	9	PA04	VDDANA	EXTINT[4]	EXTWAKE[4]	AIN[0]	AIN[4]	ADC/ VREFP				SERCOM0/ PAD[0]	TCC0/ WO[0]				CCL0/ IN[0]
	10	PA05	VDDANA	EXTINT[5]	EXTWAKE[5]	AIN[1]	AIN[5]					SERCOM0/ PAD[1]	TCC0/ WO[1]				CCL0/ IN[1]
7	11	PA06	VDDANA	EXTINT[6]	EXTWAKE[6]	AIN[2]	AIN[6]			Y[4]		SERCOM0/ PAD[2]	TCC1/ WO[0]				CCL0/ IN[2]
8	12	PA07	VDDANA	EXTINT[7]	EXTWAKE[7]	AIN[3]	AIN[7]					SERCOM0/ PAD[3]	TCC1/ WO[1]				CCL0/O UT
9	15	PA08	VDDIO	NMI			AIN[16]		X[0]	Y[6]	SERCOM0/ PAD[0]	SERCOM2/ PAD[0]	TCC0/ WO[0]	TCC1/ WO[2]			CCL1/ IN[0]
10	16	PA09	VDDIO	EXTINT[9]			AIN[17]		X[1]	Y[7]	SERCOM0/ PAD[1]	SERCOM2/ PAD[1]	TCC0/ WO[1]	TCC1/ WO[3]			CCL1/ IN[1]
	21	PA12	VDDIO	EXTINT[12]							SERCOM2/ PAD[0]	SERCOM4/ PAD[0]	TCC2/ WO[0]	TCC0/ WO[6]		AC/ CMP[0]	
	22	PA13	VDDIO	EXTINT[13]							SERCOM2/ PAD[1]	SERCOM4/ PAD[1]	TCC2/ WO[1]	TCC0/ WO[7]		AC/ CMP[1]	
15	23	PA14	VDDIO	EXTINT[14]							SERCOM2/ PAD[2]	SERCOM4/ PAD[2]	TC4/ WO[0]	TCC0/ WO[4]		GCLK/ IO[0]	
16	24	PA15	VDDIO	EXTINT[15]							SERCOM2/ PAD[3]	SERCOM4/ PAD[3]	TC4/ WO[1]	TCC0/ WO[5]		GCLK/ IO[1]	
17	25	PA16	VDDIO	EXTINT[0]					X[4]		SERCOM1/ PAD[0]	SERCOM3/ PAD[0]	TCC2/ WO[0]	TCC0/ WO[6]		GCLK/ IO[2]	CCL0/ IN[0]
18	26	PA17	VDDIO	EXTINT[1]					X[5]		SERCOM1/ PAD[1]	SERCOM3/ PAD[1]	TCC2/ WO[1]	TCC0/ WO[7]		GCLK/ IO[3]	CCL0/ IN[1]
19	27	PA18	VDDIO	EXTINT[2]					X[6]		SERCOM1/ PAD[2]	SERCOM3/ PAD[2]	TC4/ WO[0]	TCC0/ WO[2]		AC/ CMP[0]	CCL0/ IN[2]
20	28	PA19	VDDIO	EXTINT[3]					X[7]		SERCOM1/ PAD[3]	SERCOM3/ PAD[3]	TC4/ WO[1]	TCC0/ WO[3]		AC/ CMP[1]	CCL0/O UT
	31	PA22	VDDIO	EXTINT[6]					X[10]		SERCOM3/ PAD[0]	SERCOM5/ PAD[0]	TC0/ WO[0]	TCC0/ WO[4]		GCLK/ IO[6]	CCL2/ IN[0]
	32	PA23	VDDIO	EXTINT[7]					X[11]		SERCOM3/ PAD[1]	SERCOM5/ PAD[1]	TC0/ WO[1]	TCC0/ WO[5]	USB/ SOF_1KHZ	GCLK/ IO[7]	CCL2/ IN[1]
22	33	PA24	VDDIO	EXTINT[12]							SERCOM3/ PAD[2]	SERCOM5/ PAD[2]	TC1/ WO[0]	TCC1/ WO[2]	USB/DM		CCL2/ IN[2]
23	34	PA25	VDDIO	EXTINT[13]							SERCOM3/ PAD[3]	SERCOM5/ PAD[3]	TC1/ WO[1]	TCC1/ WO[3]	USB/DP		CCL2/O UT
	37	PB22	VDDIO	EXTINT[6]								SERCOM5/ PAD[2]				GCLK/ IO[0]	CCL0/ IN[0]

PIN		I/O Pin	Supply	A		B[1][2]					C	D	E	F	G	H	I
SAMR30E	SAMR30G			EIC	RSTC	AC	ADC	REF	PTC X-lines	PTC Y-lines	SERCOM[1][2]	SERCOM-ALT	TC/ TCC	TCC	COM	AC/ GCLK/ SUPC	CCL
	38	PB23	VDDIO	EXTINT[7]								SERCOM5/ PAD[3]				GCLK/ IO[1]	CCL0/OUT
25	39	PA27	VDDIN	EXTINT[15]												GCLK/ IO[0]	
27	41	PA28	VDDIN	EXTINT[8]												GCLK/ IO[0]	
31	45	PA30	VDDIN	EXTINT[10]								SERCOM1/ PAD[2]	TCC1/ WO[0]		CM0P/ SWCLK	GCLK/ IO[0]	CCL1/ IN[0]
32	46	PA31	VDDIN	EXTINT[11]								SERCOM1/ PAD[3]	TCC1/ WO[1]		SWDIO[3]		CCL1/OUT
	47	PB02	VSWOUT	EXTINT[2]			AIN[10]					SERCOM5/ PAD[0]				SUPC/ OUT[1]	CCL0/OUT
	48	PB03	VSWOUT	EXTINT[3]			AIN[11]					SERCOM5/ PAD[1]				SUPC/ VBAT	

1. All analog pin functions are on peripheral function B. Peripheral function B must be selected to disable the digital control of the pin.
2. Only some pins can be used in SERCOM I^2C mode. See also SERCOM I2C Pins.
3. This function is only activated in the presence of a debugger.
4. When an analog peripheral is enabled, the analog output of the peripheral will interfere with the alternative functions of this pin. This is also true even when the peripheral is used for internal purposes.
5. Clusters of multiple GPIO pins are sharing the same supply pin.

6.2 Internal Multiplexed Signals

PA20, PB00, PB15, PB30, PB31, PC16, PC18 and PC19 are by default controlled by the PORT as general purpose I/O and alternatively may be assigned to one of the peripheral functions A, B, C, D, E, F, G or H. To enable a peripheral function on a pin, the Peripheral Multiplexer Enable bit in the Pin Configuration register corresponding to that pin (PINCFGn.PMUXEN, n = 0-31) in the PORT must be written to one. The selection of peripheral functions A to H are done by writing to the Peripheral Multiplexing Odd and Even bits in the Peripheral Multiplexing register (PMUXn.PMUXE/O) in the PORT.

PA10, PA11, PB16 and PB17 cannot be configured as output ports. These ports are always connected to the RFCTRL inputs.

Table 6-2. Internal Multiplexed Signals

				A	A	B	B	B	B	B	B	C	D	E	F	G	H	I
Internal Signal	IO Pin	Supply	Type	EIC	RSTC	REF	ADC	AC	PTC X-lines	PTC Y-lines	OPAMP	SERCOM	SERCOM-ALT	TC/ TCC	FECTRL/ TCC/ SERCOM	COM	AC/ GCLK	CCL
DIG3	PA10	VDDIO	Input	EXTINT[10]			AIN[18]		X[2]	Y[8]		SERCOM0/ PAD[2]	SERCOM2/ PAD[2]	TCC1/ WO[0]	TCC0/WO[2]		GCLK_IO[4]	CCL1/ IN[5]
DIG4	PA11	VDDIO	Input	EXTINT[11]			AIN[19]		X[3]	Y[9]		SERCOM0/ PAD[3]	SERCOM2/ PAD[3]	TCC1/ WO[1]	TCC0/WO[3]		GCLK_IO[5]	CCL1/ OUT[1]
SLP_TR	PA20	VDDIO	I/O	EXTINT[4]					X[8]			SERCOM5/ PAD[2]	SERCOM3/ PAD[2]	TC3/WO[0]	TCC0/WO[6]		GCLK_IO[4]	
IRQ	PB00	VDDANA	I/O	EXTINT[0]			AIN[8]						SERCOM5/ PAD[2]	TC3/WO[0]			SUPC/PSOK	CCL0/ IN[1]
RSTN	PB15	VDDIO	I/O	EXTINT[15]					X[15]			SERCOM4/ PAD[3]		TC1/WO[1]			GCLK_IO[1]	CCL3/ IN[10]
DIG1	PB16	VDDIO	Input	EXTINT[0]								SERCOM5/ PAD[0]		TC2/WO[0]	TCC0/WO[4]		GCLK_IO[2]	CCL3/ IN[11]
DIG2	PB17	VDDIO	Input	EXTINT[1]								SERCOM5/ PAD[1]		TC2/WO[1]	TCC0/WO[5]		GCLK_IO[3]	CCL3/ OUT[3]

				A	A	B	B	B	B	B	B	C	D	E	F	G	H	I
Internal Signal	IO Pin	Supply	Type	EIC	RSTC	REF	ADC	AC	PTC X-lines	PTC Y-lines	OPAMP	SERCOM	SERCOM-ALT	TC/ TCC	FECTRL/ TCC/ SERCOM	COM	AC/ GCLK	CCL
MOSI	PB30	VDDIO	I/O	EXTINT[14]									SERCOM5/ PAD[0]	TCC0/ WO[0]	SERCOM4/ PAD[2]			
SEL	PB31	VDDIO	I/O	EXTINT[15]									SERCOM5/ PAD[1]	TCC0/ WO[1]	SERCOM4/ PAD[1]			
CLKM	PC16	VDDIO	I/O														GCLK_IO[1]	
SCLK	PC18	VDDIO	I/O												SERCOM4/ PAD[3]			
MISO	PC19	VDDIO	I/O												SERCOM4/ PAD[0]			

6.3 Other Functions

6.3.1 Oscillator Pinout

The oscillators are not mapped to the normal PORT functions and their multiplexing are controlled by registers in the Oscillators Controller (OSCCTRL) and in the 32KHz Oscillators Controller (OSC32KCTRL).

Table 6-3. Oscillator Pinout

Oscillator	Supply	Signal	I/O pin
XOSC	VDDIO	XIN	PA14
		XOUT	PA15
XOSC32K	VSWOUT	XIN32	PA00
		XOUT32	PA01

Note: To improve the cycle-to-cycle jitter of XOSC32, it is recommended to keep the neighboring pins of XIN32 and XOUT32 following pins as static as possible.

Table 6-4. XOSC32 Jitter Minimization

Package Pin Count	Static Signal Recommended
48	PB02, PB03, PA02, PA03
32	PA02, PA03

6.3.2 Serial Wire Debug Interface Pinout

Only the SWCLK pin is mapped to the normal PORT functions. A debugger cold-plugging or hot-plugging detection will automatically switch the SWDIO port to the SWDIO function.

Table 6-5. Serial Wire Debug Interface Pinout

Signal	Supply	I/O pin
SWCLK	VDDIN	PA30
SWDIO	VDDIN	PA31

6.3.3 SERCOM I²C Pins

Table 6-6. SERCOM Pins Supporting I²C

Device	Pins Supporting I²C Hs mode
SAMR30E	PA08, PA09, PA16, PA17, PA22, PA23
SAMR30G	PA08, PA09, PA12, PA13, PA16, PA17, PA22, PA23

6.3.4 TCC Configurations

The SAM R30 has three instances of the Timer/Counter for Control applications (TCC) peripheral, , TCC[2:0]. The following table lists the features for each TCC instance.

Table 6-7. TCC Configuration Summary

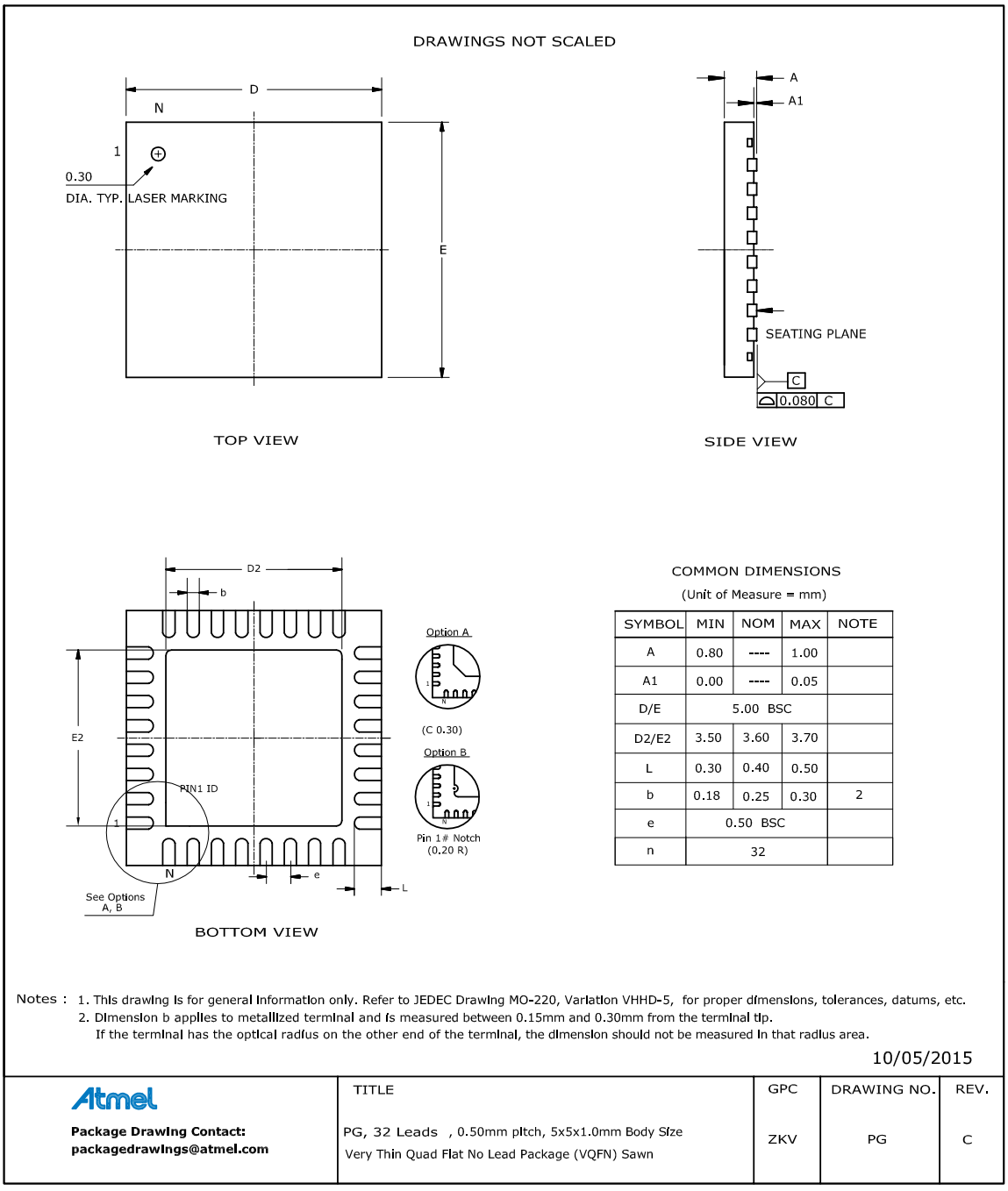
TCC#	Channels (CC_NUM)	Waveform Output (WO_NUM)	Counter size	Fault	Dithering	Output matrix	Dead Time Insertion (DTI)	SWAP	Pattern generation
0	4	8	24-bit	Yes	Yes	Yes	Yes	Yes	Yes
1	2	4	24-bit	Yes	Yes				Yes
2	2	2	16-bit	Yes					

Note: The number of CC registers (CC_NUM) for each TCC corresponds to the number of compare/capture channels, so that a TCC can have more Waveform Outputs (WO_NUM) than CC registers.

7. Packaging Information

7.1 Package Drawings

7.1.1 32 pin QFN



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	----	1.00	
A1	0.00	----	0.05	
D/E		5.00 BSC		
D2/E2	3.50	3.60	3.70	
L	0.30	0.40	0.50	
b	0.18	0.25	0.30	2
e		0.50 BSC		
n		32		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VHHD-5, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

10/05/2015

	TITLE	GPC	DRAWING NO.	REV.
Atmel **Package Drawing Contact:** **packagedrawings@atmel.com**	PG, 32 Leads , 0.50mm pitch, 5x5x1.0mm Body Size Very Thin Quad Flat No Lead Package (VQFN) Sawn	ZKV	PG	C

Note: The exposed die attach pad is connected inside the device to GND and GNDANA.

Table 7-1. Device and Package Maximum Weight

90	mg

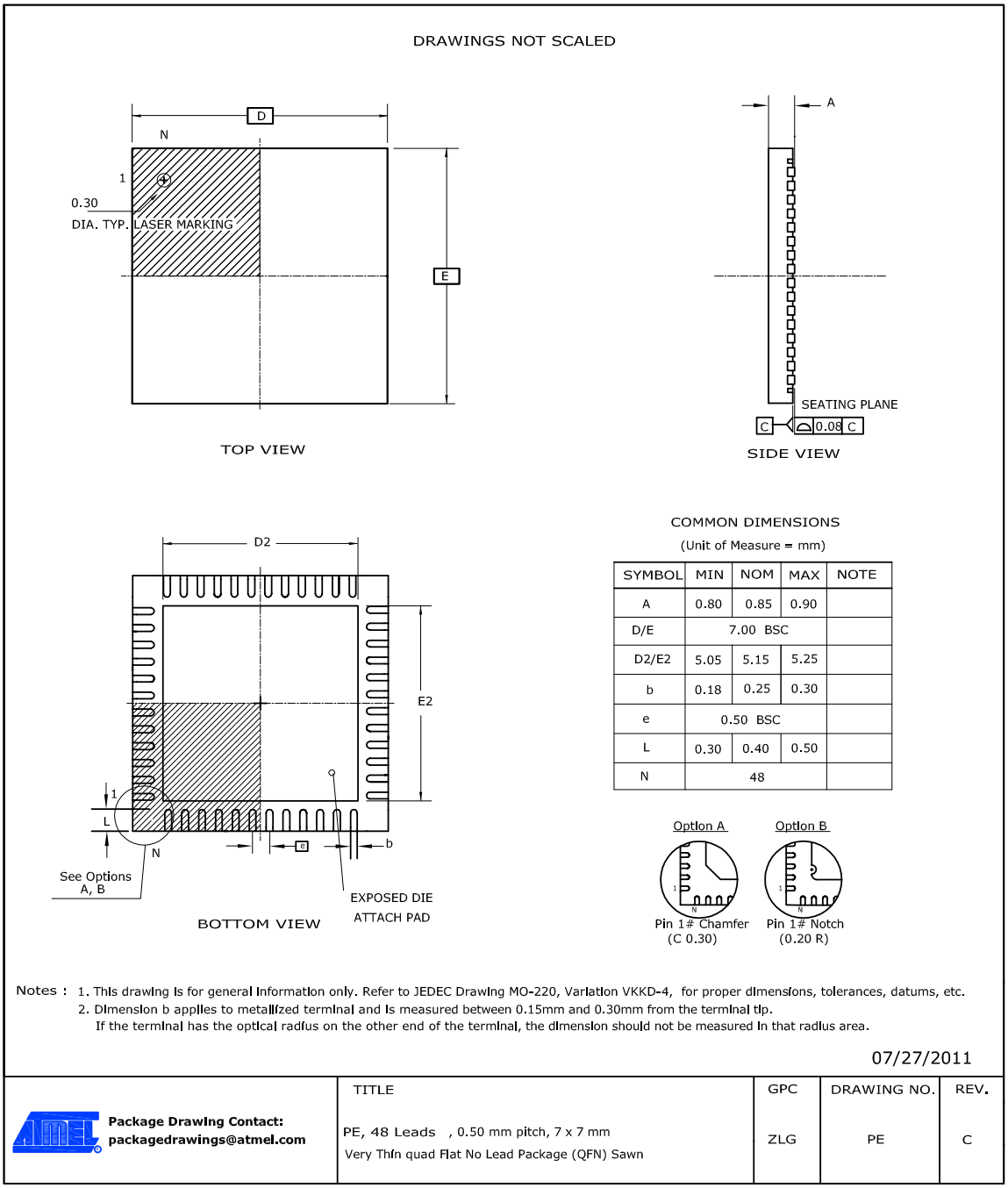
Table 7-2. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 7-3. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

7.1.2 48 pin QFN



SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.85	0.90	
D/E		7.00 BSC		
D2/E2	5.05	5.15	5.25	
b	0.18	0.25	0.30	
e		0.50 BSC		
L	0.30	0.40	0.50	
N		48		

Note: The exposed die attach pad is not connected electrically inside the device.

Table 7-4. Device and Package Maximum Weight

140	mg

Table 7-5. Package Characteristics

Moisture Sensitivity Level	MSL3

Table 7-6. Package Reference

JEDEC Drawing Reference	MO-220
JESD97 Classification	E3

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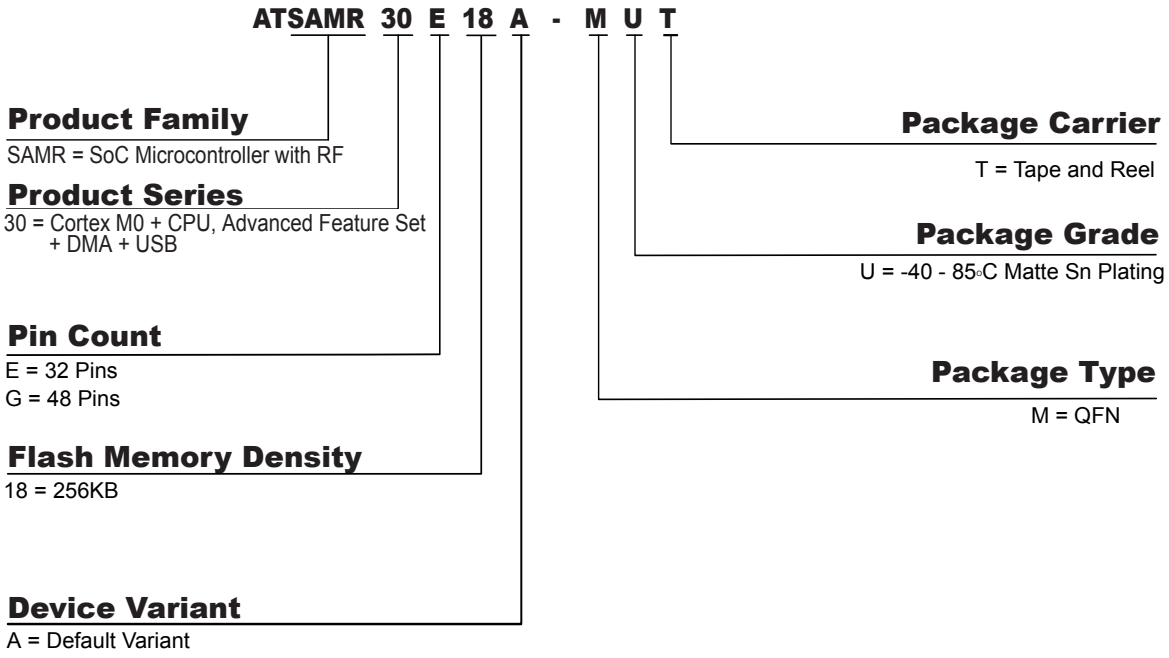
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