SAM L22 Family

SAM L22 Family Silicon Errata and Data Sheet Clarification

SAM L22 Family

The SAM L22 family of devices that you have received conform functionally to the current Device Data Sheet (DS60001465A), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1.

The errata described in this document will be addressed in future revisions of the SAM L22 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in 2. Data Sheet Clarifications, following the discussion of silicon issues.

Table 1. SAM L22 Silicon Device Identification

Part Number	Device Identification (DID[31:0])	Revision ID (DID.REVISION[3:0])	
		A	B
ATSAML22N18A	0x10820x00	0x0	0x1
ATSAML22N17A	0x10820x01		
ATSAML22N16A	0x10820x02		
ATSAML22J18A	0x10820x05		
ATSAML22J17A	0x10820x06		
ATSAML22J16A	0x10820x07		
ATSAML22G18A	0x10820x0A		
ATSAML22G17A	0x10820x0B		
ATSAML22G16A	0x10820x0C		

Note: Refer to the “Device Services Unit” chapter in the current Device Data Sheet (DS60001465A) for detailed information on Device Identification and Revision IDs for your specific device.

Silicon Errata Summary

Table 2. Silicon Errata Summary

Module	Feature	Errata #	Issue Summary	Affected Revisions	
				A	B
AC	AC0 with PA02 Input	1.1.1	After a Power-on Reset (POR), the capacitance on PA02 is offset by an amount that slowly decays during 5 seconds, making any touch-related measurements on this pin is unreliable.	X	X
PM	Low-Power Configuration	1.2.1	If the PM.STDBYCFG.VREGSMOD field is set to 2 (low-power configuration), the oscillator source driving the GCLK_MAIN clock will still be running in Standby mode causing extra consumption.	X	
DFLL48M	Write Access to DFLL Register	1.3.1	The DFLL clock must be requested before being configured, otherwise a write access to a DFLL register can freeze the device.	X	X
DFLL48M	Out of Bounds Interrupt	1.3.2	If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated.	X	X
DFLL48M	DFLL Status Bit in USB Clock Recovery Mode	1.3.3	The DFLL status bits in the STATUS register during the USB Clock Recovery mode can be wrong after a USB suspend state.	X	X
DMAC	Disable a Trigger From the Module	1.4.1	A write from DMAC to a register in a module to disable a trigger from the module to DMAC, does not work in Standby mode.	X	
DMAC	Linked Descriptor	1.4.2	When using many DMA channel and if one of these DMA channels has a linked descriptor, a fetch error can appear on this channel.	X	X
DMAC	Linked Descriptors	1.4.3	When at least one channel using linked descriptors is already active, enabling another DMA channel (with or without linked descriptors) can result in a channel Fetch Error (FERR), or an incorrect descriptor fetch.	X	X
FDPLL	FDPLL Jitter	1.5.1	Maximum FDPLL input reference clock frequency (fGCLK_DPLL) does not meet the published specification.	X	
FDPLL	DPLLRATIO Register	1.5.2	When FDPLL ratio value in DPLLRATIO register is changed on the fly, STATUS.DPLLLDRTO will not be set even though the ratio is updated.	X	X
PORT	PORT Read/Write on Non-Implemented Register	1.6.1	PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB), do not generate a PAC protection error.	X	X
SUPC	Buck Converter Mode	1.7.1	Digital Phase-Locked Loop (FDPLL96M) and Digital Frequency-Locked Loop (DFLL48M) PLL's cannot be used with main voltage regulator in Buck converter mode.	X	X
SUPC	Buck Converter as a Main Voltage Regulator	1.7.2	When Buck converter is set as main voltage regulator (SUPC.VREG.SEL=1), the microcontroller can freeze when leaving Standby mode.	X	X
Device	VBAT in Battery Back Up Mode	1.8.1	When VBAT>VDDANA, in battery Backup mode or in battery Forced mode (SUPC.BBPS.CONF=FORCED) an over consumption appears due to high voltage on PC00, PC01, PB00, PB01, PB02 pins.	X	
Device	Excess Current Consumption and SLCD	1.8.2	When LCD feature is enable and (VLCD - VDD) > 0.7V, an extra consumption occurs.	X	
Device	Excess Current Consumption	1.8.3	When ABS (VLCD - VDD) < 50 mV, an extra consumption can occur on VLCD (if VLCD generated externally) or on VDD (if VLCD generated internally).	X	

.....continued

Module	Feature	Errata #	Issue Summary	Affected Revisions	
				A	B
PM	Regulator in Standby Mode	1.9.1	Writing PM.STDBYCFG.VREGSMOD to one does not set the main voltage regulator in Standby mode, the low-power regulator is still used in Standby mode.	X	X
PTC	PTC Lines Incorrect Mapping	1.10.1	Five PTC lines are mapped on PC00, PC01, PB00, PB01, PB02 instead of PC05, PC06, PA11, PA10, PA09.	X	
ADC	ADC Result in Unipolar Mode	1.11.1	The LSB of ADC result is stuck at zero in Unipolar mode for 8-bit and 10-bit resolutions.	X	X
ADC	Synchronized Event During ADC Conversion	1.11.2	If a synchronized event is received during an ADC conversion, the ADC will not acknowledge the event, causing a stall of the event channel.	X	X
ADC	Free Running Mode	1.11.3	In Standby Sleep mode, when the ADC is in Free-Running mode (CTRLC.FREERUN=1) and the RUNSTDBY bit is set to 0 (CTRLA.RUNSTDBY=0), the ADC keeps requesting its generic clock.	X	X
ADC	SYNCBUSY.SWTRIG Bit	1.11.4	ADC SYNCBUSY.SWTRIG get stuck to one after wake up from Standby Sleep mode.	X	X
ADC	Effective Number of Bits	1.11.5	The ADC effective number of bits (ENOB) is 9.2 in this revision.	X	
ADC	Power Consumption	1.11.6	Power consumption for up to 1.6 seconds on VDDANA when the ADC is disabled manually or automatically.	X	
TC	SYNCBUSY Flag	1.12.1	When clearing the STATUS.PERBUFV/ STATUS.CCBUFVx flags, the SYNCBUSY.PER/ SYNCBUSY.CCx flags are released before the PERBUF/ CCBUFx registers are restored to their expected value.	X	X
RTC	RTC Tamper Interrupt	1.13.1	When the tamper controller is configured for asynchronous detection, an RTC tamper interrupt can occur while the RTC is disabled.	X	
RTC	Tamper Interrupt and Timestamp	1.13.2	When the tamper controller is configured for time stamp capture, the RTC tamper interrupt occurs before the TIMESTAMP register is updated.	X	
RTC	Active Layer Mode and DMA	1.13.3	When the tamper controller is configured for ACTL, the mismatch signal used to qualify the DMA and interrupt triggers produces different results.	X	
RTC	Active Layer Mode and Timestamp	1.13.4	When the tamper controller is configured for Active Layer mode, the RTC tamper interrupt occurs before the TIMESTAMP register is updated.	X	
RTC	Active Layer Mode with Input 4 and Timestamp	1.13.5	When the tamper input 4 action is configured for Active Layer mode (TAMPCTRL.IN4ACT=3), the RTC tamper interrupt occurs before the TIMESTAMP register is updated.		X
RTC	Active Layer Mode with Input 4 and DMA	1.13.6	When the tamper input 4 action is configured for Active Layer mode (TAMPCTRL.IN4ACT=3), the mismatch signal used to qualify the DMA and interrupt triggers produces different results.		X
RTC	RTC with PB01 IO	1.13.7	If PB01 is multiplexed to RTC peripheral (RTC/IN2), the system will always see this input pin as logic '0' when Backup mode is entered. If the detection transition TAMPCTRL.TAMLVL2 = 0, it might falsely wake up the system.	X	X
RTC	Tamper Detection When RTC Disabled	1.13.8	When the tamper controller is configured for CAPTURE while the RTC is disabled, there is a noisy pin.	X	X

.....continued

Module	Feature	Errata #	Issue Summary	Affected Revisions	
				A	B
TCC	Advance Capture Mode	1.14.1	Advance capture mode (CAPTMIN CAPTMAX LOCMIN LOCMAX DERIV0) does not work if an upper channel is not in one of these modes, for example, when CC[0]=CAPTMIN, CC[1]=CAPTMAX, CC[2]=CAPTEN, and CC[3]=CAPTEN, CAPTMIN and CAPTMAX do not work.	X	X
TCC	SYNCBUSY Flag	1.14.2	When clearing the STATUS.xxBUFV flag, the SYNCBUSY is released before the register is restored to its appropriate value.	X	X
TCC	MAX Capture Mode	1.14.3	In Capture mode using MAX Capture mode, timer set in up counting mode, if an input event occurred within 2 cycles before TOP, the value captured is zero instead of TOP.	X	X
TCC	Dithering Mode	1.14.4	Using TCC in Dithering mode with external retrigger events, can lead to unexpected stretch of right aligned pulses or shrink of left aligned pulses.	X	X
SERCOM	USART in Auto-baud Mode	1.15.1	In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.	X	X
SERCOM	SERCOM Instances	1.15.2	SAML22G devices delivered before date code 1716 only have 3 SERCOMs available (0,1,2) instead of 4 (0,1,2,3).	X	X
SERCOM	Parity Error in ISO7816 T0 Mode	1.15.3	In ISO7816 T0 mode when start of frame detect is enabled (CTRLB.SFDE=1), if there is a parity error, receive start (INTFLAG.RXS) can be erroneously set.	X	X
SERCOM	SDA and SCL Fall Time	1.15.4	When configured in HS or FastMode+, SDA and SCL fall times are shorter than I^2C specification requirement and can lead to reflection.	X	X
EIC	EIC_ASYNCH Register	1.16.1	Access to EIC_ASYNCH register in 8-bit or16-bit mode is not functional.	X	X
EIC	Low Level or Rising Edge or Both Edges	1.16.2	When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag might appear for the dedicated pin on the INTFLAG.EXTINT[x] register as soon as the EIC is enabled using the CTRLA ENABLE bit.	X	X
EIC	NMI Configuration	1.16.3	Changing the NMI configuration (CONFIGn.SENSEx) on the fly may lead to a false NMI interrupt.	X	X
EIC	Asynchronous Edge Detection	1.16.4	When the asynchronous edge detection is enabled, and the system is in Standby mode, only the first edge will generate an event. The following edges won't generate events until the system wakes up.	X	X
TRNG	Power Consumption in Standby Mode	1.17.1	When TRNG is disabled, some internal logic could continue to operate causing an over consumption.	X	X
EVSYS	Synchronous Path	1.18.1	Using synchronous, spurious overrun can appear with generic clock for the channel always on.	X	X
EVSYS	Overrun Flag	1.18.2	The acknowledge between an event user and the EVSYS, clears the CHSTATUS.CHBUSYn bit before this information is fully propagated in the EVSYS one GCLK_EVSYS_CHANNEL_n clock cycle later.	X	X

Table of Contents

1. Silicon Errata Issues

The following issues apply to the SAM L22 family of devices.

Note: The silicon errata listed in this document supersedes the Errata Chapter 49 in SAM L22 product data sheet (DS60001465A).

1.1 Analog Comparator (AC)

1.1.1 AC0 with PA02 Input Reference:15745

After a Power-on Reset (POR), the capacitance on PA02 is offset by an amount that slowly decays during 5 seconds, making any touch-related measurements on this pin is unreliable.

Workaround

To get rid of this offset, reconfigure the AC0 input muxes to use internal inputs instead of AC0 pin 0 (default reset value) before starting any touch-related measurements (COMPCTRL0.MUXPOS=4,COMPCTRL0.MUXNEG=5).

Affected Silicon Revisions

A	B						
X	X						

1.2 Power Manager

1.2.1 Low-Power Configuration Reference:14539

If the PM.STDBYCFG.VREGSMOD field is set to 2 (low-power configuration), the oscillator source driving the GCLK_MAIN clock will still be running in Standby mode causing extra consumption.

Workaround

Before entering in Standby mode, switch the GCLK_MAIN to the OSCULP32K clock. After wake-up, switch back to the GCLK_MAIN clock.

Affected Silicon Revisions

A	B						
X							

1.3 48 MHz Digital Frequency-Locked Loop (DFLL48M)

1.3.1 Write Access to DFLL Register Reference:9905

The DFLL clock must be requested before being configured, otherwise a write access to a DFLL register can freeze the device.

Workaround
Write a zero to the DFLL ONDEMAND bit in the DFLLCTRL register before configuring the DFLL module.

Affected Silicon Revisions

A	B						
X	X						

1.3.2 Out of Bounds Interrupt Reference:16192

If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. These interrupts will be generated even if the final calibration values at DFLL48M lock are not at maximum or minimum, and might therefore be false out of bounds interrupts.

Workaround
Check the lock bits, DFLLLCKC and DFLLLCKF, in the OSCCTRL Interrupt Flag Status and Clear register (INTFLAG) are both set before enabling the DFLLOOB interrupt.

Affected Silicon Revisions

A	B						
X	X						

1.3.3 DFLL Status Bit in USB Clock Recovery Mode Reference:16193

The DFLL status bits in the STATUS register during the USB Clock Recovery mode can be wrong after a USB suspend state.

Workaround
Do not monitor the DFLL status bits in the STATUS register during the USB Clock Recovery mode.

Affected Silicon Revisions

A	B						
X	X						

1.4 Direct Memory Access Controller (DMAC)

1.4.1 Disable a Trigger From the Module Reference:14648

A write from DMAC to a register in a module to disable a trigger from the module to DMAC, does not work in Standby mode, for example, DAC, LCD, and SERCOM in transmission mode.

Workaround
If the module generating the trigger also generates event, use event interface instead of triggers with DMAC, for example, SLCD.

Affected Silicon Revisions

A	B						
X							

1.4.2 Linked Descriptor Reference:15670

When using many DMA channel and if one of these DMA channels has a linked descriptor, a fetch error can appear on this channel.

Workaround

Do not use linked descriptors, instead make a software link.

1. Replace the channel which used linked descriptor by two channels DMA (with linked descriptor disabled) handled by two channels event system:
   - DMA channel 0 transfer completion can send a conditional event for DMA channel 1 (through event system with configuration of BTCTRL.EVOSEL=BLOCK for channel 0 and configuration CHCTRLB.EVACT=CBLOCK for channel 1)
   - On the transfer complete reception of the DMA channel 0, immediately re-enable the channel 0
   - Then DMA channel 1 transfer completion can send a conditional event for DMA channel 0 (through event system with configuration of BTCTRL.EVOSEL=BLOCK for channel 1 and configuration CHCTRLB.EVACT=CBLOCK for channel 0)
   - On the transfer complete reception of the DMA channel 1, immediately re-enable the channel 1
   - The mechanism can be launched by sending a software event on the DMA channel 0

Affected Silicon Revisions

A	B						
X	X						

1.4.3 Linked Descriptors Reference:15683

When at least one channel using linked descriptors is already active, enabling another DMA channel (with or without linked descriptors) can result in a channel Fetch Error (FERR), or an incorrect descriptor fetch.

Workaround

This happens if the channel number of the channels being enabled is lower than the channels already active.

When enabling a DMA channel while other channels using linked descriptors are already active, the channel number of the new channel enabled must be greater than the other channel numbers.

Affected Silicon Revisions

A	B						
X	X						

1.5 96 MHz Fractional Digital Phase Locked Loop (FDPLL)

1.5.1 FDPLL Jitter Reference:14784

Maximum FDPLL input reference clock frequency (fGCLK_DPLL) does not meet the published specification. The maximum supported input reference clock is 1MHz.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

1.5.2 DPLLRATIO Register Reference:15753

When FDPLL ratio value in DPLLRATIO register is changed on the fly, STATUS.DPLLLDRTO will not be set even though the ratio is updated.

Workaround

Monitor the INTFLAG.DPLLLDRTO instead of STATUS.DPLLLDRTO to get the status for DPLLRATIO update.

Affected Silicon Revisions

A	B						
X	X						

1.6 PORT - I/O Pin Controller

1.6.1 PORT Read/Write on Non-Implemented Register Reference:15611

PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB), do not generate a PAC protection error.

Workaround

None.

Affected Silicon Revisions

A	B						
X	X						

1.7 Supply Controller (SUPC)

1.7.1 Buck Converter Mode Reference: CHIP003-311 & CHIP003-314

Buck Converter mode is not supported when using Digital Phase-Locked Loop (FDPLL96M) and Digital Frequency-Locked Loop (DFLL48M). As a result, Table 45-7 “Active Current Consumption - Active Mode” data for Buck Converter mode with FDPLL96M configuration is not valid and must be disregarded.

Workaround

Use the LDO Regulator mode when using FDPLL and DFLL.

Affected Silicon Revisions

A	B						
X	X						

1.7.2 Buck Converter as a Main Voltage Regulator Reference:15264

When Buck converter is set as main voltage regulator (SUPC.VREG.SEL=1), the microcontroller can freeze when leaving Standby mode.

Workaround

Enable the main voltage regulator in Standby mode (SUPC.VREG.RUNSTDBY=1) and set the Standby in PL0 bit to one (SUPC.VREG.STDBYPL0=1).

Note: When SUPC.VREG.STDBYPL0=1, In Standby Sleep mode, the voltage regulator is used in PL0.

Affected Silicon Revisions

A	B						
X	X						

1.8 Device

1.8.1 VBAT in Battery Back Up Mode Reference:14643

When VBAT>VDDANA, in battery Backup mode or in battery Forced mode (SUPC.BBPS.CONF=FORCED) an over consumption appears due to high voltage on PC00, PC01, PB00, PB01, PB02 pins.

Workaround

PC00, PC01, PB00, PB01, PB02 should be tied to GND.

Affected Silicon Revisions

A	B						
X							

1.8.2 Excess Current Consumption and SLCD Reference:14696

When LCD feature is enable and (VLCD - VDD) > 0.7V, an extra consumption occurs. In case of VLCD internally generated, the VLCD voltage will be out of specification.

Workaround

The LCD feature must be used only when (VLCD - VDD) < 0.7V

Affected Silicon Revisions

A	B						
X							

1.8.3 Excess Current Consumption Reference:14742

When ABS (VLCD - VDD) < 50 mV, an extra consumption can occur on VLCD (if VLCD generated externally) or on VDD (if VLCD generated internally).

Workaround

ABS (VLCD - VDD) should be greater than 50 mV.

Affected Silicon Revisions

A	B						
X							

1.9 Power Manager

1.9.1 Regulator in Standby Mode Reference:14543

Writing PM.STDBYCFG.VREGSMOD to one does not set the main voltage regulator in Standby mode, the low-power regulator is still used in Standby mode.

Workaround

Set SUPC.VREG.RUNSTDBY to one.

Affected Silicon Revisions

A	B						
X	X						

1.10 Peripheral Touch Controller (PTC)

1.10.1 PTC Lines Incorrect Mapping Reference:14792

Five PTC lines are mapped on PC00, PC01, PB00, PB01, PB02 instead of PC05, PC06, PA11, PA10, PA09.

Workaround

None.

Affected Silicon Revisions

A	B						
X							

1.11 Analog-to-Digital Converter (ADC)

1.11.1 ADC Result in Unipolar Mode Reference:14431

The LSB of ADC result is stuck at zero in Unipolar mode for 8-bit and 10-bit resolutions.

Workaround

Use 12-bit resolution and take only least 8 bits or 10 bits, if necessary.

Affected Silicon Revisions

A	B						
X	X						

1.11.2 Synchronized Event During ADC Conversion Reference:14795

If a synchronized event is received during an ADC conversion, the ADC will not acknowledge the event, causing a stall of the event channel.

Workaround

When using events with the ADC, only the asynchronous path from the event system must be used.

Affected Silicon Revisions

A	B						
X	X						

1.11.3 Free Running Mode Reference:15463

In Standby Sleep mode, when the ADC is in Free-Running mode (CTRLC.FREERUN=1) and the RUNSTDBY bit is set to 0 (CTRLA.RUNSTDBY=0), the ADC keeps requesting its generic clock.

Workaround

Stop the free-running mode (CTRLC.FREERUN=0) before entering Standby Sleep mode

Affected Silicon Revisions

A	B						
X	X						

1.11.4 SYNCBUSY.SWTRIG Bit Reference:16027

ADC SYNCBUSY.SWTRIG get stuck to one after wake up from Standby Sleep mode.

Workaround
Ignore ADC SYNCBUSY.SWTRIG status when waking up from Standby Sleep mode. ADC result can be read after INTFLAG.RESRDY is set. To start the next conversion, write a '1' to SWTRIG.START.

Affected Silicon Revisions

A	B						
X	X						

1.11.5 Effective Number of Bits Reference:13850

The ADC effective number of bits (ENOB) is 9.2 in this revision.

Workaround
None.

Affected Silicon Revisions

A	B						
X							

1.11.6 Power Consumption Reference:14349

Power consumption for up to 1.6 seconds on VDDANA when the ADC is disabled manually or automatically.

Workaround
None

Affected Silicon Revisions

A	B						
X							

1.12 Timer/Counter (TC)

1.12.1 SYNCBUSY Flag Reference:15056, TMR100-12

When clearing the STATUS.PERBUFV/STATUS.CCBUFVx flags, the SYNCBUSY.PER/SYNCBUSY.CCx flags are released before the PERBUF/CCBUFx registers are restored to their expected value.

Workaround
Successively clear the STATUS.PERBUFV/STATUS.CCBUFVx flags twice to ensure that the PERBUF/CCBUFx registers value is properly restored before updating it.

Affected Silicon Revisions

A	B						
X	X						

1.13 Real-Time Counter (RTC)

1.13.1 RTC Tamper Interrupt Reference:14653

When the tamper controller is configured for asynchronous detection, an RTC tamper interrupt can occur while the RTC is disabled.

Workaround

Set the tamper interrupt enable only when the RTC is enabled.

- Program INTEN.TAMPER=1 after setting the CTRLA.ENABLE register and clearing the INTFLAG.TAMPER register
- Program INTEN.TAMPER=0 before clearing the CTRLA.ENABLE register

Affected Silicon Revisions

A	B						
X							

1.13.2 Tamper Interrupt and Timestamp Reference:14654

When the tamper controller is configured for time stamp capture, the RTC tamper interrupt occurs before the TIMESTAMP register is updated.

Workaround

Two workarounds are available:

1. Use the DMA trigger to determine when the TIMESTAMP value is registered. The DMA trigger sets after the TIMESTAMP register update.
2. Implement a wait loop to create a delay when the tamper interrupt handler routine begins to when the TIMESTAMP register is read. The delay must be long enough to wait for 3x CLK_RTC period. For example,
   - If CLK_RTC frequency is 1 kHz, the delay must be at least 3 ms
   - If CLK_RTC frequency is 32 kHz, the delay must be at least 92 us

Affected Silicon Revisions

A	B						
X							

1.13.3 Active Layer Mode and DMA Reference:14692

When the tamper controller is configured for ACTL, the mismatch signal used to qualify the DMA and interrupt triggers produces different results. The DMA implements a level-detection whereas the interrupt implements an edge-detection. The result is that the DMA may trigger frequently from the same mismatch compared to the interrupt which will only trigger once.

Workaround

If no other tamper configurations are implemented (that is, other TAMPCTRL.INxACT != WAKE/CAPTURE and EVCTRL.EVEI=0), do not enable the DMA if possible to prevent performance degradation.

Affected Silicon Revisions

A	B						
X							

1.13.4 Active Layer Mode and Timestamp Reference:14810

When the tamper controller is configured for Active Layer mode, the RTC tamper interrupt occurs before the TIMESTAMP register is updated.

Workaround

Two workarounds are available:

1. Use the DMA trigger to determine when the TIMESTAMP value is registered. The DMA trigger sets after the TIMESTAMP register update.
2. Implement a wait loop to create a delay when the tamper interrupt handler routine begins to when the TIMESTAMP register is read. The delay must be long enough to wait for 3x CLK_RTC period. For example,
   – If CLK_RTC frequency is 1 kHz, the delay must be at least 3 ms
   – If CLK_RTC frequency is 32 kHz, the delay must be at least 92 us

Affected Silicon Revisions

A	B						
X							

1.13.5 Active Layer Mode with Input 4 and Timestamp Reference:14819

When the tamper input 4 action is configured for Active Layer mode (TAMPCTRL.IN4ACT=3), the RTC tamper interrupt occurs before the TIMESTAMP register is updated.

Workaround

The following two workarounds are available:

1. Use the DMA trigger to determine when the TIMESTAMP value is registered. The DMA trigger sets after the TIMESTAMP register update. Refer Errata 1.13.6.
2. Implement a wait loop to create a delay, when the tamper interrupt handler routine begins, to when the TIMESTAMP register is read. The delay must be long enough to wait for 3x CLK_RTC period.

For example,

- If CLK_RTC frequency is 1 kHz, the delay must be at least 3 ms
- If CLK_RTC frequency is 32 kHz, the delay must be at least 92 us

Affected Silicon Revisions

A	B							
	X							

1.13.6 Active Layer Mode with Input 4 and DMA Reference:14820

When the tamper input 4 action is configured for Active Layer mode (TAMPCTRL.IN4ACT=3), the mismatch signal used to qualify the DMA and interrupt triggers produces different results. The DMA implements a level-detection whereas the interrupt implements an edge-detection. The result is that the DMA may trigger frequently from the same mismatch compared to the interrupt which will only trigger once.

Workaround

The following three workarounds are available:

1. Tamper inputs 0, 1, 2 and 3 can be configured for active layer with DMA.
2. Tamper input 4 can be configured with DMA for any mode other than active layer.
3. If Tamper input 4 is to be used in active layer, do not enable the DMA, to prevent performance degradation.

Affected Silicon Revisions

A	B							
	X							

1.13.7 RTC with PB01 IO Reference:15010

If PB01 is multiplexed to RTC peripheral (RTC/IN2), the system will always see this input pin as logic ‘0’ when Backup mode is entered. If the detection transition TAMPCTRL.TAMLVL2 = 0, it might falsely wake up the system.

Workaround

If the system is expected to enter Backup mode, use other tamper pins (IN0/IN1/IN3/IN4) for tamper detection.

Affected Silicon Revisions

A	B						
X	X						

1.13.8 Tamper Detection When RTC Disabled Reference:15092

When the tamper controller is configured for CAPTURE while the RTC is disabled, a noisy pin can trigger the following once the RTC is enabled:

- The timestamp capture
- The tamper interrupt if enabled
- The DMA trigger if enabled

Workaround

1. Set the tamper interrupt enable only when the RTC is enabled:
   – Clear the tamper interrupt flags and ID registers (INTFLAG.TAMPER & TAMPID.TAMPIDx registers)
   – Enable RTC (CTRLA.ENABLE = 1)
   – Enable the tamper interrupt (INTEN.TAMPER = 1)

To disable the RTC, disable the Tamper interrupts before disabling the RTC.

- Disable Tamper interrupts (INTEN.TAMPER=0)
- Disable the RTC (CTRLA.ENABLE=0)

2. Issue a CPU read of the TIMESTAMP register immediately after the RTC is enabled. This releases the register lock allowing the capture of the next and valid tamper. This releases the DMA trigger of the erroneous capture tamper.

Affected Silicon Revisions

A	B						
X	X						

1.14 Timer/Counter for Control Applications (TCC)

1.14.1 Advance Capture Mode Reference:14817

Advance capture mode (CAPTMIN CAPTMAX LOCMIN LOCMAX DERIV0) does not work if an upper channel is not in one of these modes, for example, when CC[0]=CAPTMIN, CC[1]=CAPTMAX, CC[2]=CAPTEN, and CC[3]=CAPTEN, CAPTMIN and CAPTMAX do not work.

Workaround

Basic Capture mode must be set in lower channel, and advance Capture mode in upper channel, for example, CC[0]=CAPTEN , CC[1]=CAPTEN , CC[2]=CAPTMIN, CC[3]=CAPTMAX.

All capture will be done as expected.

Affected Silicon Revisions

A	B						
X	X						

1.14.2 SYNCBUSY Flag Reference:15057

When clearing the STATUS.xxBUFV flag, the SYNCBUSY is released before the register is restored to its appropriate value.

Workaround

To ensure that the register value is restored before updating this same register through xx or xxBUF with a new value, the STATUS.xxBUFV flag must be cleared twice.

Affected Silicon Revisions

A	B						
X	X						

1.14.3 MAX Capture Mode Reference:15059

In Capture mode using MAX Capture mode, timer set in up counting mode, if an input event occurred within 2 cycles before TOP, the value captured is zero instead of TOP.

Workaround
Two possible options are as follows:

- If event is controllable, capture event should not occur when counter is within 2 cycles before TOP value.
- Use timer in down Counter mode and capture MIN value instead of MAX.

Affected Silicon Revisions

A	B						
X	X						

1.14.4 Dithering Mode Reference:15625

Using TCC in Dithering mode with external retrigger events, can lead to unexpected stretch of right aligned pulses or shrink of left aligned pulses.

Workaround
Do not use retrigger events or actions when TCC is configured in Dithering mode.

Affected Silicon Revisions

A	B						
X	X						

1.15 Serial Communication Interface (SERCOM)

1.15.1 USART in Auto-baud Mode Reference:13852

In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.

Workaround
None.

Affected Silicon Revisions

A	B						
X	X						

1.15.2 SERCOM Instances Reference:15511

SAML22G devices delivered before date code 1716 only have 3 sercoms available (0,1,2) instead of 4 (0,1,2,3).

Workaround
None.

Affected Silicon Revisions

A	B						
X	X						

1.15.3 Parity Error in ISO7816 T0 Mode Reference:14694

In ISO7816 T0 mode when start of frame detect is enabled (CTRLB.SFDE=1), if there is a parity error, receive start (INTFLAG.RXS) can be erroneously set. This is because the transmitted parity low is also seen by the receiver and looks like a start of frame.

Workaround

Clear INTFLAG.RXS when received on parity error.

Affected Silicon Revisions

A	B						
X	X						

1.15.4 SDA and SCL Fall Time Reference:16225

When configured in HS or FastMode+, SDA and SCL fall times are shorter than I^2C specification requirement and can lead to reflection.

Workaround

When reflection is observed a 100 ohms serial resistor can be added on the impacted line.

Affected Silicon Revisions

A	B						
X	X						

1.16 External Interrupt Controller (EIC)

1.16.1 EIC_ASYNCH Register Reference:14417

Access to EIC_ASYNCH register in 8-bit or16-bit mode is not functional.

- Writing in 8-bit mode will also write this byte in all bytes of the 32-bit word
- Writing higher 16-bits will also write the lower 16-bits
- Writing lower 16-bits will also write the higher 16-bits

Workaround

Two workarounds are available:

- Use 32-bit write mode
- Write only lower 16-bits (This will write upper 16-bits also, but does not impact the application)

Affected Silicon Revisions

A	B						
X	X						

1.16.2 Low Level or Rising Edge or Both Edges Reference:15278

When the EIC is configured to generate an interrupt on a low level or rising edge or both edges (CONFIGn.SENSEx) with the filter enabled (CONFIGn.FILTENx), a spurious flag might appear for the dedicated pin on the INTFLAG.EXTINT[x] register as soon as the EIC is enabled using the CTRLA ENABLE bit.

Workaround

Clear the INTFLAG bit once the EIC is enabled and before enabling the interrupts.

Affected Silicon Revisions

A	B						
X	X						

1.16.3 NMI Configuration Reference:15279

Changing the NMI configuration (CONFIGn.SENSEx) on the fly may lead to a false NMI interrupt.

Workaround

Clear the NMIFLAG bit once the NMI has been modified.

Affected Silicon Revisions

A	B						
X	X						

1.16.4 Asynchronous Edge Detection Reference:16103

When the asynchronous edge detection is enabled, and the system is in Standby mode, only the first edge will generate an event. The following edges won’t generate events until the system wakes up.

Workaround

Asynchronous edge detection doesn’t work, instead use the synchronous edge detection (ASYNCH.ASYNCH[x]=0). To reduce power consumption when using synchronous edge detection, either set the GCLK_EIC frequency as low as possible or select the ULP32K clock (EIC CTRLA.CKSEL=1).

Affected Silicon Revisions

A	B						
X	X						

1.17 True Random Number Generator (TRNG)

1.17.1 Power Consumption in Standby Mode Reference:14827, MATH100-7

When TRNG is disabled, some internal logic could continue to operate causing an over consumption.

Workaround

Disable the TRNG module twice:

- TRNG -> CTRLA.reg = 0;
- TRNG -> CTRLA.reg = 0;

Affected Silicon Revisions

A	B						
X	X						

1.18 Event System (EVSYS)

1.18.1 Synchronous Path Reference:14532

Using synchronous, spurious overrun can appear with generic clock for the channel always on.

Workaround

- Request the generic clock on demand by setting the CHANNEL.ONDEMAND bit to 1
- No penalty is introduced

Affected Silicon Revisions

A	B						
X	X						

1.18.2 Overrun Flag Reference:14835

The acknowledge between an event user and the EVSYS, clears the CHSTATUS.CHBUSYn bit before this information is fully propagated in the EVSYS one GCLK_EVSYS_CHANNEL_n clock cycle later. As a consequence, any generator event occurring on that channel before that extra GCLK_EVSYS_CHANNEL_n clock cycle will trigger the overrun flag.

Workaround

For applications using event generators other than the software event, monitor the OVR flag.

For applications using the software event generator, wait one GCLK_EVSYS_CHANNEL_n clock cycle after the CHSTATUS.CHBUSYn bit is cleared before issuing a software event.

Affected Silicon Revisions

A	B						
X	X						

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001465A).

Note: Corrections in tables, registers, and text are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

No clarifications to report at this time.

3. Appendix A: Revision History

Rev B Document 05/2019)

The following Errata have been updated:

- SUPC: 1.7.1 Buck Converter Mode Reference: CHIP003-311 & CHIP003-314
- 1.12.1 SYNCBUSY Flag Reference:15056, TMR100-12
- 1.17.1 Power Consumption in Standby Mode Reference:14827, MATH100-7

ADC errata 1.16.1 and 1.16.2 were moved to 1.11.5 and 1.11.6 respectively for document clarity. This resulted in errata listed afterward to shift down by one in their number specification from the previous released document version.

Rev A Document (08/2018)

- This is the initial released version of this document that lists the silicon errata issues which were documented in the SAM L22 product data sheet DS60001465A (Chapter 49)
- Added silicon errata: FDPLL Jitter Reference: 14784
- Added silicon errata: Buck Converter Mode Reference: CHIP003-311 & CHIP003-314
- Added silicon errata: MAX Capture Mode Reference: 15059

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