DATA SHEET



SAA7120H; SAA7121H
Digital video encoder

Product specification
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1 FEATURES



- Monolithic CMOS 3.3 V device
- Digital PAL/NTSC encoder
- System pixel frequency 13.5 MHz
- Accepts MPEG decoded data on 8-bit wide input port; input data format C_B-Y-C_R (CCIR 656)
- Three Digital-to-Analog Converters (DACs) for Y, C and CVBS two times oversampled with 10-bit resolution
- Real-time control of subcarrier
- Cross-colour reduction filter
- Closed captioning encoding and World Standard Teletext (WST) and North-American Broadcast Text System (NABTS) teletext encoding including sequencer and filter
- Line 23 Wide Screen Signalling (WSS) encoding
- Fast I^2C-bus control port (400 kHz)
- Encoder can be master or slave
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- Internal Colour Bar Generator (CBG)
- 2×2 bytes in lines 20 (NTSC) for copy guard management system can be loaded via I^2C-bus
- Down mode of DACs
- Controlled rise/fall times of synchronization and blanking output signals
- Macrovision™(1) Pay-per-View copy protection system rev. 7.01 and rev. 6.1 as option; this applies to SAA7120H only. The device is protected by USA patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights. Use of the Macrovision anti-copy process in the device is licensed for non-commercial home use only. Reverse engineering or disassembly is prohibited. Please contact your nearest Philips Semiconductors sales office for more information
- QFP44 package.

2 GENERAL DESCRIPTION

The SAA7120H; SAA7121H encodes digital YUV video data to an NTSC or PAL CVBS or S-video signal.

The circuit accepts CCIR compatible YUV data with 720 active pixels per line in 4 : 2 : 2 multiplexed formats, for example MPEG decoded data. It includes a sync/clock generator and on-chip DACs.

(1) Macrovision™ is a trademark of the Macrovision Corporation.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7120H	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body $10 \times 10 \times 1.75$ mm	SOT307-2
SAA7121H			

4 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	3.1	3.3	3.5	V
V_{DDD}	digital supply voltage	3.0	3.3	3.6	V
I_{DDA}	analog supply current	–	55	62	mA
I_{DDD}	digital supply current	–	32	45	mA
V_i	input signal voltage levels	TTL compatible			
$V_{o(p-p)}$	analog output signal voltages Y, C and CVBS without load (peak-to-peak value)	–	1.35	–	V
R_L	load resistance	75	–	300	Ω
$LE_{lf(i)}$	low frequency integral linearity error	–	–	±3	LSB
$LE_{lf(d)}$	low frequency differential linearity error	–	–	±1	LSB
T_{amb}	ambient temperature	0	–	70	°C

5 BLOCK DIAGRAM

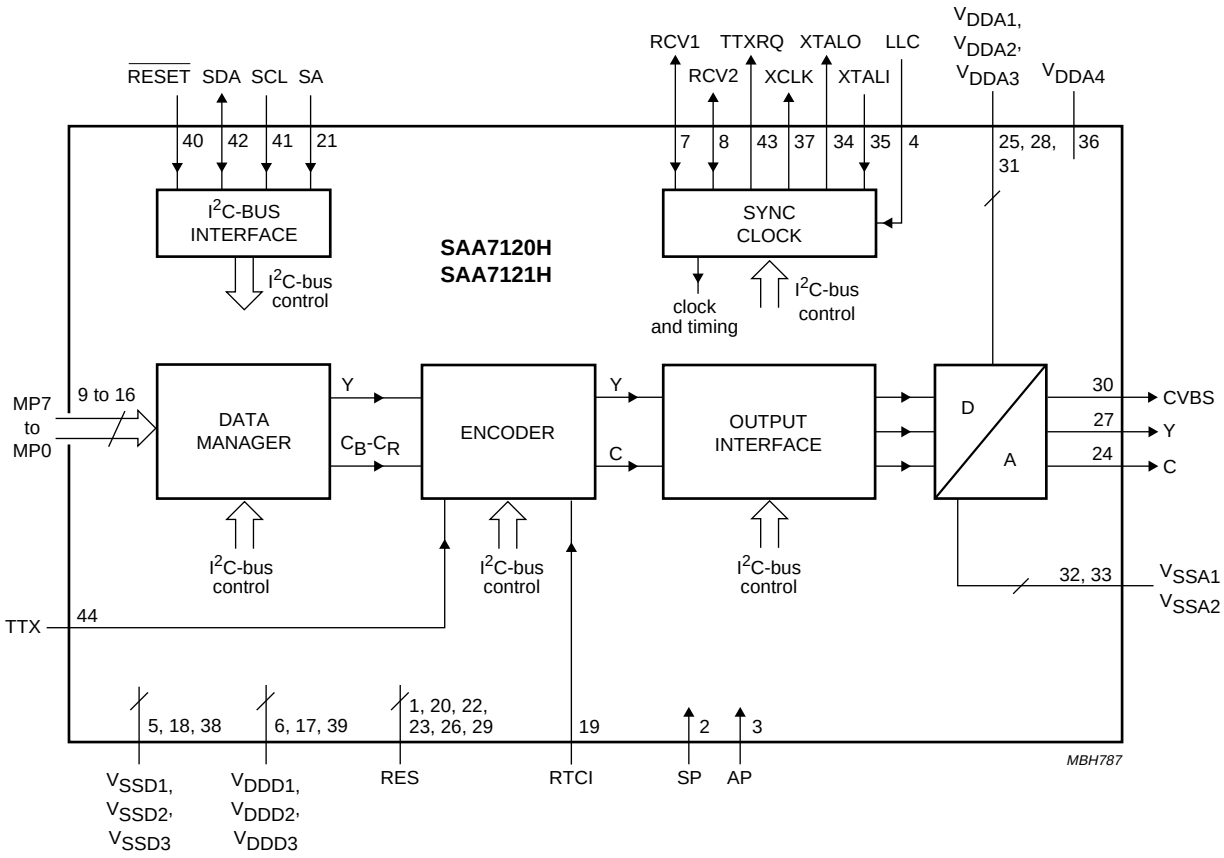


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
RES	1	–	reserved
SP	2	I	test pin; connected to digital ground for normal operation
AP	3	I	test pin; connected to digital ground for normal operation
LLC	4	I	line-locked clock; this is the 27 MHz master clock for the encoder
V_{SSD1}	5	supply	digital ground 1
V_{DDD1}	6	supply	digital supply voltage 1
RCV1	7	I/O	raster control 1 for video port; this pin receives/provides a VS/FS/FSEQ signal
RCV2	8	I/O	raster control 2 for video port; this pin provides an HS pulse of programmable length or receives an HS pulse
MP7	9	I	MPEG ports; inputs for *"CCIR 656"* style multiplexed C_B-Y-C_R data
MP6	10	I	
MP5	11	I	
MP4	12	I	
MP3	13	I	
MP2	14	I	
MP1	15	I	
MP0	16	I	
V_{DDD2}	17	supply	digital supply voltage 2
V_{SSD2}	18	supply	digital ground 2
RTCI	19	I	real-time control input; if the LLC clock is provided by an SAA7111 or SAA7151B, RTCI should be connected to the RTCO pin of the respective decoder to improve the signal quality
RES	20	–	reserved
SA	21	I	the I^2C-bus slave address select input pin; LOW: slave address = 88H, HIGH = 8CH
RES	22	–	reserved
RES	23	–	reserved
C	24	O	analog output of the chrominance signal
V_{DDA1}	25	supply	analog supply voltage 1 for the C DAC
RES	26	–	reserved
Y	27	O	analog output of VBS signal
V_{DDA2}	28	supply	analog supply voltage 2 for the Y DAC
RES	29	–	reserved
CVBS	30	O	analog output of the CVBS signal
V_{DDA3}	31	supply	analog supply voltage 3 for the CVBS DAC
V_{SSA1}	32	supply	analog ground 1 for the DACs
V_{SSA2}	33	supply	analog ground 2 for the oscillator and reference voltage
XTALO	34	O	crystal oscillator output
XTALI	35	I	crystal oscillator input; if the oscillator is not used, this pin should be connected to ground
V_{DDA4}	36	supply	analog supply voltage 4 for the oscillator and reference voltage

SYMBOL	PIN	TYPE	DESCRIPTION
XCLK	37	O	clock output of the crystal oscillator
V_{SSD3}	38	supply	digital ground 3
V_{DDD3}	39	supply	digital supply voltage 3
$\overline{RESET}$	40	I	Reset input, active LOW. After reset is applied, all digital I/Os are in input mode. The I^2C-bus receiver waits for the START condition.
SCL	41	I	I^2C-bus serial clock input
SDA	42	I/O	I^2C-bus serial data input/output
TTXRQ	43	O	teletext request output, indicating when bit stream is valid
TTX	44	I	teletext bit stream input

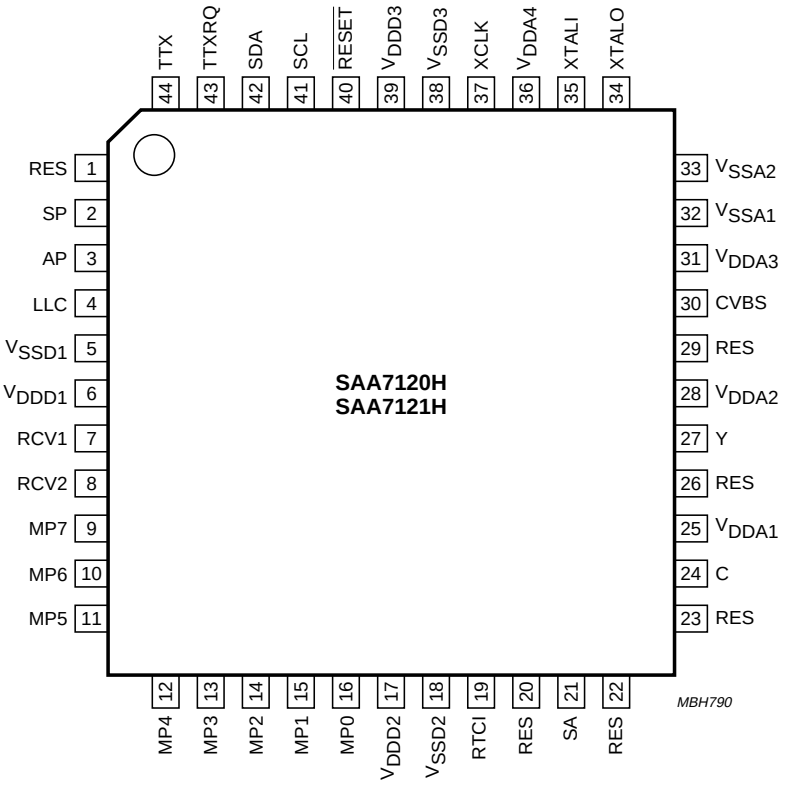


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

The digital video encoder encodes digital luminance and colour difference signals into analog CVBS and simultaneously S-video signals. NTSC-M, PAL-B/G and sub-standards are supported. Both interlaced and non-interlaced operation is possible for all standards.

The basic encoder function consists of subcarrier generation, colour modulation and insertion of synchronization signals. Luminance and chrominance signals are filtered in accordance with the standard requirements of *"RS-170-A"* and *"CCIR 624"*.

For ease of analog post filtering the signals are twice oversampled with respect to the pixel clock before digital-to-analog conversion.

The total filter transfer characteristics are illustrated in Figs 3 to 6. The DACs for Y, C and CVBS are realized with full 10-bit resolution.

The 8-bit multiplexed C_B-Y-C_R formats are *"CCIR 656"* (D1 format) compatible, but the SAV and EAV codes can be decoded optionally, when the device is operated in slave mode.

It is also possible to connect a Philips digital video decoder (SAA7111 or SAA7151B) to this encoder. By connecting pin RTCI to pin RTCO of a decoder, information about the actual subcarrier, PAL-ID and (with SAA7111 and newer types) definite subcarrier phase can be inserted.

The digital video encoder synthesizes all necessary internal signals, colour subcarrier frequency and synchronization signals from that clock.

Wide screen signalling data can be loaded via the I^2C-bus and is inserted into line 23 for standards using 50 Hz field rate.

The IC also contains closed caption and extended data services encoding (line 21), and supports anti-taping signal generation in accordance with Macrovision.

A number of possibilities are provided for setting different video parameters, such as:

- Black and blanking level control
- Colour subcarrier frequency
- Variable burst amplitude, etc.

During reset ($\overline{\text{RESET}}$ = LOW) and after reset is released, all digital I/O stages are set to input mode. A reset forces the I^2C-bus interface to abort any running bus transfer and sets register 3A to 03H, register 61 to 06H, registers 6BH and 6EH to 00H and bit TTX60 to 0. No other control registers are influenced by a reset.

7.1 Data manager

Real-time arbitration on the data stream to be encoded is performed in the data manager.

A pre-defined colour look-up table located in this block can be read out in a pre-defined sequence (8 steps per active video line), achieving a colour bar test pattern generator without the need for an external data source. The colour bar function is under software control only.

7.2 Encoder

7.2.1 VIDEO PATH

The encoder generates out of Y, U and V baseband signals luminance and colour subcarrier output signals, suitable for use as CVBS or separate Y and C signals.

Luminance is modified in gain and in offset (latter programmable in a certain range to enable different black level set-ups). A blanking level can be set after insertion of a fixed synchronization pulse tip level in accordance with standard composite synchronization schemes. Other manipulations used for the Macrovision anti-taping process such as additional insertion of AGC super-white pulses (programmable in height) are supported by the SAA7120H only.

In order to enable easy analog post filtering, luminance is interpolated from a 13.5 MHz data rate to a 27 MHz data rate, providing luminance in 10-bit resolution. This filter is also used to define smoothed transients for synchronization pulses and blanking period. The transfer characteristics of the luminance interpolation filter are illustrated in Figs 5 and 6.

Chrominance is modified in gain (programmable separately for U and V), standard dependent burst is inserted, before baseband colour signals are interpolated from a 6.75 MHz data rate to a 27 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher colour bandwidth, which can be made use of for Y and C output. The transfer characteristics of the chrominance interpolation filter are illustrated in Figs 3 and 4.

The amplitude, beginning and ending of the inserted burst, is programmable in a certain range that is suitable for standard signals and for special effects. Behind the succeeding quadrature modulator, colour in a 10-bit resolution is provided on the subcarrier.

The numeric ratio between Y and C outputs is in accordance with the respective standards.

7.2.2 TELETEXT INSERTION AND ENCODING

Pin TTX receives a WST or NABTS teletext bitstream sampled at the LLC clock. At each rising edge of output signal (TTXRQ) a single teletext bit has to be provided after a programmable delay at the input pin.

Phase variant interpolation is achieved on this bitstream in the internal teletext encoder, providing sufficient small phase jitter on the output text lines.

TTXRQ provides a fully programmable request signal to the teletext source, indicating the insertion period of bitstream at lines which are selectable independently for both fields. The internal insertion window for text is set to 360 (PAL-WST), 296 (NTSC-WST) or 288 (NABTS) teletext bits including clock run-in bits. The protocol and timing are illustrated in Fig.10.

7.2.3 CLOSED CAPTION ENCODER

Using this circuit, data in accordance with the specification of closed caption or extended data service, delivered by the control interface, can be encoded (line 21). Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number where data is to be encoded in, can be modified in a certain range.

The data clock frequency is in accordance with the definition for NTSC-M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode closed caption data for 50 Hz field frequencies at 32 times the horizontal line frequency.

7.2.4 ANTI-TAPING (SAA7120H ONLY)

For more information contact your nearest Philips Semiconductors sales office.

7.3 Output interface/DACs

In the output interface, encoded Y and C signals are converted from digital-to-analog in a 10-bit resolution. Y and C signals are also combined to a 10-bit CVBS signal.

The CVBS output occurs with the same processing delay as the Y and C outputs. Absolute amplitude at the input of the DAC for CVBS is reduced by $^{15}/_{16}$ with respect to Y and C DACs to make maximum use of conversion ranges.

Outputs of the DACs can be set together in two groups, via software control, to a minimum output voltage for either purpose.

7.4 Synchronization

The synchronization of the SAA7120H; SAA7121H is able to operate in two modes; slave mode and master mode.

In the slave mode, the circuit accepts synchronization pulses at the bidirectional RCV1 port. The timing and trigger behaviour related to RCV1 can be influenced by programming the polarity and the on-chip delay of RCV1. Active slope of RCV1 defines the vertical phase and optionally the odd/even and colour frame phase to be initialized, it also can be used to set the horizontal phase.

If the horizontal phase is not to be influenced by RCV1, a horizontal pulse needs to be applied to pin RCV2. Timing and trigger behaviour can also be influenced for the signal at pin RCV2.

If there are missing pulses at RCV1 and/or RCV2, the time base of the IC runs free, thus an arbitrary number of synchronization slopes may miss, but no additional pulses (with the incorrect phase) must occur.

If the vertical and horizontal phase is derived from RCV1, RCV2 can be used for horizontal or composite blanking input or output.

Alternatively, the device can be triggered by auxiliary codes in a *“CCIR 656”* data stream at the MP port.

In the master mode, the time base of the circuit continuously runs free. On the RCV1 port, the device can output:

- A Vertical Sync (VS) signal with 3 or 2.5 lines duration
- An odd/even signal which is LOW in odd fields
- A Field Sequence (FSEQ) signal which is HIGH in the first of 4 or 8 fields respectively.

On the RCV2 port, the IC can provide a horizontal pulse with programmable start and stop phase; this pulse can be inhibited in the vertical blanking period to build up, for example, a composite blanking signal.

The polarity of both RCV1 and RCV2 is selectable by software control.

The length of a field and the start and end of its active part can be programmed. The active part of a field always starts at the beginning of a line.

7.5 I²C-bus interface

The I²C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 400 kbits/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write only, except one readable status byte.

The I²C-bus slave address is defined as 88H with pin 21 (SA) tied LOW and as 8CH with pin 21 (SA) tied HIGH.

7.6 Input levels and formats

The SAA7120H; SAA7121H expects digital Y, C_B and C_R data with levels (digital codes) in accordance with *"CCIR 601"*.

For C and CVBS outputs, deviating amplitudes of the colour difference signals can be compensated by independent gain control setting, while gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

Reference levels are measured with a colour bar, 100% white, 100% amplitude and 100% saturation.

Table 1 *"CCIR 601"* signal component levels

COLOUR	SIGNALS		
	Y	C_B	C_R
White	235	128	128
Yellow	210	16	146
Cyan	170	166	16
Green	145	54	34
Magenta	106	202	222
Red	81	90	240
Blue	41	240	110
Black	16	128	128

Table 2 8-bit multiplexed format (similar to *"CCIR 601"*)

TIME	BITS							
	0	1	2	3	4	5	6	7
Sample	C_B0	Y0	C_R0	Y1	C_B2	Y2	C_R2	Y3
Luminance pixel number	0		1		2		3	
Colour pixel number	0				2			

7.7 Bit allocation map

Table 3 Slave receiver (slave address 88H or 8CH)

REGISTER FUNCTION	SUBADDR	DATA BYTE[1]							
		D7	D6	D5	D4	D3	D2	D1	D0
Null	00H to 25H	0	0	0	0	0	0	0	0
Wide screen signal	26H	WSS7	WSS6	WSS5	WSS4	WSS3	WSS2	WSS1	WSS0
Wide screen signal	27H	WSSON	0	WSS13	WSS12	WSS11	WSS10	WSS9	WSS8
Real-time control, burst start	28H	DECCOL	DECFIS	BS5	BS4	BS3	BS2	BS1	BS0
Burst end	29H	0	0	BE5	BE4	BE3	BE2	BE1	BE0
Copy guard odd 0	2AH	CGO07	CGO06	CGO05	CGO04	CGO03	CGO02	CGO01	CGO00
Copy guard odd 1	2BH	CGO17	CGO16	CGO15	CGO14	CGO13	CGO12	CGO11	CGO10
Copy guard even 0	2CH	CGE07	CGE06	CGE05	CGE04	CGE03	CGE02	CGE01	CGE00
Copy guard even 1	2DH	CGE17	CGE16	CGE15	CGE14	CGE13	CGE12	CGE11	CGE10
Copy guard enable	2EH	CGEN1	CGEN0	0	0	0	0	0	0
Null	2FH to 39H	0	0	0	0	0	0	0	0
Input port control	3AH	CBENB	0	0	SYMP	0	0	Y2C	UV2C
Chrominance phase	5AH	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0
Gain U	5BH	GAINU7	GAINU6	GAINU5	GAINU4	GAINU3	GAINU2	GAINU1	GAINU0
Gain V	5CH	GAINV7	GAINV6	GAINV5	GAINV4	GAINV3	GAINV2	GAINV1	GAINV0
Gain U MSB, real-time control, black level	5DH	GAINU8	DECOE	BLCKL5	BLCKL4	BLCKL3	BLCKL2	BLCKL1	BLCKL0
Gain V MSB, real-time control, blanking level	5EH	GAINV8	DECPH	BLNNL5	BLNNL4	BLNNL3	BLNNL2	BLNNL1	BLNNL0
CCR, blanking level VBI	5FH	CCRS1	CCRS0	BLNVB5	BLNVB4	BLNVB3	BLNVB2	BLNVB1	BLNVB0
Null	60H	0	0	0	0	0	0	0	0
Standard control	61H	0	DOWN	INPI	YGS	0	SCBW	PAL	FISE
RTC enable, burst amplitude	62H	RTCE	BSTA6	BSTA5	BSTA4	BSTA3	BSTA2	BSTA1	BSTA0
Subcarrier 0	63H	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
Subcarrier 1	64H	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
Subcarrier 2	65H	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
Subcarrier 3	66H	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
Line 21 odd 0	67H	L21O07	L21O06	L21O05	L21O04	L21O03	L21O02	L21O01	L21O00
Line 21 odd 1	68H	L21O17	L21O16	L21O15	L21O14	L21O13	L21O12	L21O11	L21O10

REGISTER FUNCTION	SUBADDR	DATA BYTE(1)							
		D7	D6	D5	D4	D3	D2	D1	D0
Line 21 even 0	69H	L21E07	L21E06	L21E05	L21E04	L21E03	L21E02	L21E01	L21E00
Line 21 even 1	6AH	L21E17	L21E16	L21E15	L21E14	L21E13	L21E12	L21E11	L21E10
RCV port control	6BH	SRCV11	SRCV10	TRCV2	ORCV1	PRCV1	CBLF	ORCV2	PRCV2
Trigger control	6CH	HTRIG7	HTRIG6	HTRIG5	HTRIG4	HTRIG3	HTRIG2	HTRIG1	HTRIG0
Trigger control	6DH	HTRIG10	HTRIG9	HTRIG8	VTRIG4	VTRIG3	VTRIG2	VTRIG1	VTRIG0
Multi control	6EH	SBLBN	0	PHRES1	PHRES0	0	0	FLC1	FLC0
Closed caption, teletext enable	6FH	CCEN1	CCEN0	TTXEN	SCCLN4	SCCLN3	SCCLN2	SCCLN1	SCCLN0
RCV2 output start	70H	RCV2S7	RCV2S6	RCV2S5	RCV2S4	RCV2S3	RCV2S2	RCV2S1	RCV2S0
RCV2 output end	71H	RCV2E7	RCV2E6	RCV2E5	RCV2E4	RCV2E3	RCV2E2	RCV2E1	RCV2E0
MSBs RCV2 output	72H	0	RCV2E10	RCV2E9	RCV2E8	0	RCV2S10	RCV2S9	RCV2S8
TTX request H start	73H	TTXHS7	TTXHS6	TTXHS5	TTXHS4	TTXHS3	TTXHS2	TTXHS1	TTXHS0
TTX request H delay	74H	TTXHD7	TTXHD6	TTXHD5	TTXHD4	TTXHD3	TTXHD2	TTXHD1	TTXHD0
Vsync shift	75H	0	0	0	0	0	VS_S2	VS_S1	VS_S0
TTX odd request vertical start	76H	TTXOVS7	TTXOVS6	TTXOVS5	TTXOVS4	TTXOVS3	TTXOVS2	TTXOVS1	TTXOVS0
TTX odd request vertical end	77H	TTXOVE7	TTXOVE6	TTXOVE5	TTXOVE4	TTXOVE3	TTXOVE2	TTXOVE1	TTXOVE0
TTX even request vertical start	78H	TTXEVS7	TTXEVS6	TTXEVS5	TTXEVS4	TTXEVS3	TTXEVS2	TTXEVS1	TTXEVS0
TTX even request vertical end	79H	TTXEVE7	TTXEVE6	TTXEVE5	TTXEVE4	TTXEVE3	TTXEVE2	TTXEVE1	TTXEVE0
First active line	7AH	FAL7	FAL6	FAL5	FAL4	FAL3	FAL2	FAL1	FAL0
Last active line	7BH	LAL7	LAL6	LAL5	LAL4	LAL3	LAL2	LAL1	LAL0
MSB vertical	7CH	TTX60	LAL8	0	FAL8	TTXEVE8	TTXOVE8	TTXEVS8	TTXOVS8
Null	7DH	0	0	0	0	0	0	0	0
Disable TTX line	7EH	LINE12	LINE11	LINE10	LINE9	LINE8	LINE7	LINE6	LINE5
Disable TTX line	7FH	LINE20	LINE19	LINE18	LINE17	LINE16	LINE15	LINE14	LINE13

Note

1. All bits labelled ‘0’ are reserved. They must be programmed with logic 0.

7.8 I²C-bus format

Table 4 I²C-bus address; see Table 5

S	SLAVE ADDRESS	ACK	SUBADDRESS	ACK	DATA 0	ACK	--------	DATA n	ACK	P

Table 5 Explanation of Table 4

PART	DESCRIPTION
S	START condition
SLAVE ADDRESS	1000 100X or 1000 110X; note 1
ACK	acknowledge, generated by the slave
SUBADDRESS; note 2	subaddress byte
DATA	data byte
--------	continued data bytes and ACKs
P	STOP condition

Notes

1. X is the read/write control bit; X = logic 0 is order to write; X = logic 1 is order to read; no subaddressing with read.
2. If more than 1 byte DATA is transmitted, then auto-increment of the subaddress is performed.

7.9 Slave receiver

Table 6 Subaddresses 26H and 27H

DATA BYTE	LOGIC LEVEL	DESCRIPTION
WSS	–	wide screen signalling bits 3 to 0 = aspect ratio 7 to 4 = enhanced services 10 to 8 = subtitles 13 to 11 = reserved
WSSON	0	wide screen signalling output is disabled; default after reset
	1	wide screen signalling output is enabled

Table 7 Subaddresses 28H and 29H

DATA BYTE	LOGIC LEVEL	DESCRIPTION	REMARKS
BS	–	starting point of burst in clock cycles	PAL: BS = 33 (21H); default after reset
			NTSC: BS = 25 (19H)
BE	–	ending point of burst in clock cycles	PAL: BE = 29 (1DH); default after reset
			NTSC: BE = 29 (1DH)
DECCOL	0	disable colour detection bit of RTCI input	
	1	enable colour detection bit of RTCI input	bit RTCE must be set to logic 1 (see Fig.9)
DECFIS	0	field sequence as FISE in subaddress 61	
	1	field sequence as FISE bit in RTCI input	bit RTCE must be set to logic 1 (see Fig.9)

Table 8 Subaddresses 2AH to 2DH

DATA BYTE	DESCRIPTION	REMARKS
CGO0	first byte of copy guard data, odd field	LSBs of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, in accordance with the definition of line 20 encoding format
CGO1	second byte of copy guard data, odd field	
CGE0	first byte of copy guard data, even field	
CGE1	second byte of copy guard data, even field	

Table 9 Subaddress 2EH

DATA BYTE		DESCRIPTION
CCEN1	CCEN0	
0	0	copy guard encoding off
0	1	enables encoding in field 1 (odd)
1	0	enables encoding in field 2 (even)
1	1	enables encoding in both fields

Table 10 Subaddress 3AH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
UV2C	0	C_B, C_R data are twos complement
	1	C_B, C_R data are straight binary; default after reset
Y2C	0	Y data is twos complement
	1	Y data is straight binary; default after reset
SYMP	0	horizontal and vertical trigger is taken from RCV2 and RCV1 respectively; default after reset
	1	horizontal and vertical trigger is decoded out of *"CCIR 656"* compatible data at MP port
CBENB	0	data from input ports is encoded; default after reset
	1	colour bar with fixed colours is encoded

Table 11 Subaddress 5AH

DATA BYTE	DESCRIPTION	VALUE	RESULT
CHPS	phase of encoded colour subcarrier (including burst) relative to horizontal sync; can be adjusted in steps of 360/256 degrees	00H	PAL-B/G and data from input ports
		2AH	PAL-B/G and data from look-up table
		88H	NTSC-M and data from input ports
		AAH	NTSC-M and data from look-up table

Table 12 Subaddresses 5BH and 5DH

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINU	variable gain for C_B signal; input representation in accordance with *"CCIR 601"*	white-to-black = 92.5 IRE	GAINU = −2.17 × nominal to +2.16 × nominal
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 118 (76H)	output subcarrier of U contribution = nominal
		white-to-black = 100 IRE	GAINU = −2.05 × nominal to +2.04 × nominal
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 125 (7DH)	output subcarrier of U contribution = nominal

Table 13 Subaddresses 5CH and 5EH

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINV	variable gain for C_R signal; input representation in accordance with *"CCIR 601"*	white-to-black = 92.5 IRE	GAINV = −1.55 × nominal to +1.55 × nominal
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 165 (A5H)	output subcarrier of V contribution = nominal
		white-to-black = 100 IRE	GAINV = −1.46 × nominal to +1.46 × nominal
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 175 (AFH)	output subcarrier of V contribution = nominal

Table 14 Subaddress 5DH

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLCKL	variable black level; input representation in accordance with *"CCIR 601"*	white-to-sync = 140 IRE; note 1	recommended value: BLCKL = 42 (2AH)
		BLCKL = 0; note 1	output black level = 34 IRE
		BLCKL = 63 (3FH); note 1	output black level = 54 IRE
		white-to-sync = 143 IRE; note 2	recommended value: BLCKL = 35 (23H)
		BLCKL = 0; note 2	output black level = 32 IRE
		BLCKL = 63 (3FH); note 2	output black level = 52 IRE
DECOE	real-time control	logic 0	disable odd/even field control bit from RTCI
		logic 1	enable odd/even field control bit from RTCI (see Fig.9)

Notes

1. Output black level/IRE = BLCKL × 2/6.29 + 34.0.
2. Output black level/IRE = BLCKL × 2/6.18 + 31.7.

Table 15 Subaddress 5EH

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLNNL	variable blanking level	white-to-sync = 140 IRE; note 1	recommended value: BLNNL = 46 (2EH)
		BLNNL = 0; note 1	output blanking level = 25 IRE
		BLNNL = 63 (3FH); note 1	output blanking level = 45 IRE
		white-to-sync = 143 IRE; note 2	recommended value: BLNNL = 53 (35H)
		BLNNL = 0; note 2	output blanking level = 26 IRE
		BLNNL = 63 (3FH); note 2	output blanking level = 46 IRE
DECPH	real-time control	logic 0	disable subcarrier phase reset bit from RTCI
		logic 1	enable subcarrier phase reset bit from RTCI (see Fig.9)

Notes

1. Output black level/IRE = BLNNL $\times$ 2/6.29 + 25.4.
2. Output black level/IRE = BLNNL $\times$ 2/6.18 + 25.9; default after reset: 35H.

Table 16 Subaddress 5FH

DATA BYTE	DESCRIPTION
BLNVB	variable blanking level during vertical blanking interval is typically identical to value of BLNNL
CCRS	select cross-colour reduction filter in luminance; see Table 17

Table 17 Logic levels and function of CCRS

CCRS1	CCRS0	DESCRIPTION
0	0	no cross-colour reduction; for overall transfer characteristic of luminance see Fig.5
0	1	cross-colour reduction #1 active; for overall transfer characteristic see Fig.5
1	0	cross-colour reduction #2 active; for overall transfer characteristic see Fig.5
1	1	cross-colour reduction #3 active; for overall transfer characteristic see Fig.5

Table 18 Subaddress 61H

DATA BYTE	LOGIC LEVEL	DESCRIPTION
FISE	0	864 total pixel clocks per line; default after reset
	1	858 total pixel clocks per line
PAL	0	NTSC encoding (non-alternating V component)
	1	PAL encoding (alternating V component); default after reset
SCBW	0	enlarged bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 3 and 4)
	1	standard bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 3 and 4); default after reset
YGS	0	luminance gain for white – black 100 IRE; default after reset
	1	luminance gain for white – black 92.5 IRE including 7.5 IRE set-up of black
INPI	0	PAL switch phase is nominal; default after reset
	1	PAL switch phase is inverted compared to nominal if RTC is enabled; see Table 19
DOWN	0	DACs for CVBS, Y and C in normal operational mode; default after reset
	1	DACs for CVBS, Y and C forced to lowest output voltage

Table 19 Subaddress 62H

DATA BYTE	LOGIC LEVEL	DESCRIPTION
RTCE	0	no real-time control of generated subcarrier frequency; default after reset
	1	real-time control of generated subcarrier frequency through SAA7151B or SAA7111; for timing see Fig.9

Table 20 Subaddress 62H

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BSTA	amplitude of colour burst; input representation in accordance with *"CCIR 601"*	white-to-black = 92.5 IRE; burst = 40 IRE; NTSC encoding BSTA = 0 to 2.02 × nominal	recommended value: BSTA = 63 (3FH)
		white-to-black = 92.5 IRE; burst = 40 IRE; PAL encoding BSTA = 0 to 2.82 × nominal	recommended value: BSTA = 45 (2DH)
		white-to-black = 100 IRE; burst = 43 IRE; NTSC encoding BSTA = 0 to 1.90 × nominal	recommended value: BSTA = 67 (43H)
		white-to-black = 100 IRE; burst = 43 IRE; PAL encoding BSTA = 0 to 3.02 × nominal	recommended value: BSTA = 47 (2FH); default after reset

Table 21 Subaddresses 63H to 66H (four bytes to program subcarrier frequency)

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
FSC0 to FSC3	f_{sc} = subcarrier frequency (in multiples of line frequency); f_{llc} = clock frequency (in multiples of line frequency)	$FSC = round\left(\frac{f_{sc}}{f_{llc}} \times 2^{32}\right)$; note 1	FSC3 = most significant byte; FSC0 = least significant byte

Note

1. Examples:
   a) NTSC-M: f_{sc} = 227.5, f_{llc} = 1716 → FSC = 569408543 (21F07C1FH).
   b) PAL-B/G: f_{sc} = 283.7516, f_{llc} = 1728 → FSC = 705268427 (2A098ACBH).

Table 22 Subaddresses 67H to 6AH

DATA BYTE	DESCRIPTION	REMARKS
L21O0	first byte of captioning data, odd field	LSBs of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, in accordance with the definition of line 21 encoding format
L21O1	second byte of captioning data, odd field	
L21E0	first byte of extended data, even field	
L21E1	second byte of extended data, even field	

Table 23 Subaddress 6BH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
PRCV2	0	polarity of RCV2 as output is active HIGH, rising edge is taken when input, respectively; default after reset
	1	polarity of RCV2 as output is active LOW, falling edge is taken when input, respectively
ORCV2	0	pin RCV2 is switched to input; default after reset
	1	pin RCV2 is switched to output
CBLF	0	if ORCV2 = HIGH, pin RCV2 provides an HREF signal (horizontal reference pulse that is defined by RCV2S and RCV2E, also during vertical blanking interval); default after reset if ORCV2 = LOW and bit SYMP = LOW, signal input to RCV2 is used for horizontal synchronization only (if TRCV2 = 1); default after reset
	1	if ORCV2 = HIGH, pin RCV2 provides a ‘composite-blanking-not’ signal, for example a reference pulse that is defined by RCV2S and RCV2E, excluding vertical blanking interval, which is defined by FAL and LAL if ORCV2 = LOW and bit SYMP = LOW, signal input to RCV2 is used for horizontal synchronization (if TRCV2 = 1) and as an internal blanking signal
PRCV1	0	polarity of RCV1 as output is active HIGH, rising edge is taken when input; default after reset
	1	polarity of RCV1 as output is active LOW, falling edge is taken when input
ORCV1	0	pin RCV1 is switched to input; default after reset
	1	pin RCV1 is switched to output
TRCV2	0	horizontal synchronization is taken from RCV1 port (at bit SYMP = LOW) or from decoded frame sync of “*CCIR 656”* input (at bit SYMP = HIGH); default after reset
	1	horizontal synchronization is taken from RCV2 port (at bit SYMP = LOW)
SRCV1	–	defines signal type on pin RCV1; see Table 24

Table 24 Logic levels and function of SRCV1

DATA BYTE		AS OUTPUT	AS INPUT	FUNCTION
SRCV11	SRCV10			
0	0	VS	VS	vertical sync each field; default after reset
0	1	FS	FS	frame sync (odd/even)
1	0	FSEQ	FSEQ	field sequence, vertical sync every fourth field (PAL = 0) or eighth field (PAL = 1)
1	1	–	–	not applicable

Table 25 Subaddresses 6CH and 6DH

DATA BYTE	DESCRIPTION
HTRIG	sets the horizontal trigger phase related to signal on RCV1 or RCV2 input values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed; increasing HTRIG decreases delays of all internally generated timing signals; reference mark: analog output horizontal sync (leading slope) coincides with active edge of RCV used for triggering at HTRIG = 398H (398H)

Table 26 Subaddress 6DH

DATA BYTE	DESCRIPTION
VTRIG	sets the vertical trigger phase related to signal on RCV1 input increasing VTRIG decreases delays of all internally generated timing signals, measured in half lines; variation range of VTRIG = 0 to 31 (1FH)

Table 27 Subaddress 6EH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
SBLBN	0	vertical blanking is defined by programming of FAL and LAL; default after reset
	1	vertical blanking is forced in accordance with *"CCIR 624"* (50 Hz) or RS170A (60 Hz)
PHRES	–	selects the phase reset mode of the colour subcarrier generator; see Table 28
FLC	–	field length control; see Table 29

Table 28 Logic levels and function of PHRES

DATA BYTE		DESCRIPTION
PHRES1	PHRES0	
0	0	no reset or reset via RTCI from SAA7111 if bit RTCE = 1; default after reset
0	1	reset every two lines
1	0	reset every eight fields
1	1	reset every four fields

Table 29 Logic levels and function of FLC

DATA BYTE		DESCRIPTION
FLC1	FLC0	
0	0	interlaced 312.5 lines/field at 50 Hz, 262.5 lines/field at 60 Hz; default after reset
0	1	non-interlaced 312 lines/field at 50 Hz, 262 lines/field at 60 Hz
1	0	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz
1	1	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz

Table 30 Subaddress 6FH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
CCEN	–	enables individual line 21 encoding; see Table 31
TTXEN	0	disables teletext insertion; default after reset
	1	enables teletext insertion
SCCLN	–	selects the actual line, where closed caption or extended data are encoded; line = (SCCLN + 4) for M-systems; line = (SCCLN + 1) for other systems

Table 31 Logic levels and function of CCEN

DATA BYTE		DESCRIPTION
CCEN1	CCEN0	
0	0	line 21 encoding off; default after reset
0	1	enables encoding in field 1 (odd)
1	0	enables encoding in field 2 (even)
1	1	enables encoding in both fields

Table 32 Subaddresses 70H to 72H

DATA BYTE	DESCRIPTION
RCV2S	start of output signal on pin RCV2 values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed; first active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at RCV2S = 11AH (0FDH)
RCV2E	end of output signal on pin RCV2 values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed; last active pixel at analog outputs (corresponding input pixel coinciding with RCV2) at RCV2E = 694H (687H)

Table 33 Subaddresses 73H and 74H

DATA BYTE	DESCRIPTION	REMARKS
TTXHS	start of signal on pin TTXRQ; see Fig.10	PAL: TTXHS = 42H
		NTSC: TTXHS = 54H
TTXHD	indicates the delay in clock cycles between rising edge of TTXRQ output and valid data at pin TTX	minimum value: TTXHD = 2

Table 34 Subaddress 75H

DATA BYTE	DESCRIPTION	REMARKS
VS_S	vertical sync shift between RCV1 and RCV2 (switched to output); in master mode it is possible to shift Hsync (RCV2; CBLF = 0) against Vsync (RCV1; SRCV1 = 00)	standard value: VS_S = 3

Table 35 Subaddresses 76H, 77H and 7CH

DATA BYTE	DESCRIPTION	REMARKS
TTXOVS	first line of occurrence of signal on pin TTXRQ in odd field line = (TTXOVS + 4) for M-systems line = (TTXOVS + 1) for other systems	PAL: TTXOVS = 05H; NTSC: TTXOVS = 06H
TTXOVE	last line of occurrence of signal on pin TTXRQ in odd field line = (TTXOVE + 3) for M-systems line = TTXOVE for other systems	PAL: TTXOVE = 16H; NTSC: TTXOVE = 10H

Table 36 Subaddresses 78H, 79H and 7CH

DATA BYTE	DESCRIPTION	REMARKS
TTXEVS	first line of occurrence of signal on pin TTXRQ in even field line = (TTXEVS + 4) for M-systems line = (TTXEVS + 1) for other systems	PAL: TTXEVS = 04H; NTSC: TTXEVS = 05H
TTXEVE	last line of occurrence of signal on pin TTXRQ in even field line = (TTXEVE + 3) for M-systems line = TTXEVE for other systems	PAL: TTXEVE = 16H; NTSC: TTXEVE = 10H

Table 37 Subaddresses 7AH to 7CH

DATA BYTE	DESCRIPTION
FAL	first active line: measured in lines; FAL = 0 coincides with the first field synchronization pulse first active line = (FAL + 4) for M systems first active line = (FAL + 1) for other systems
LAL	last active line: measured in lines; LAL = 0 coincides with the first field synchronization pulse last active line = (LAL + 3) for M-systems last active line = LAL for other systems

Table 38 Subaddress 7CH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
TTX60	0	enables NABTS (FISE = 1) or European TTX (FISE = 0); default after reset
	1	enables world standard teletext 60 Hz (FISE = 1)

Table 39 Subaddresses 7EH and 7FH

DATA BYTE	DESCRIPTION
LINE	individual lines in both fields (PAL counting) can be disabled for insertion of teletext by the respective bits, disabled line = LINExx (50 Hz field rate); this bit mask is effective only, if the lines are enabled by TTXOVS/TTXOVE and TTXEVS/TTXEVE

In subaddresses 5BH, 5CH, 5DH, 5EH and 62H all IRE values are rounded up.

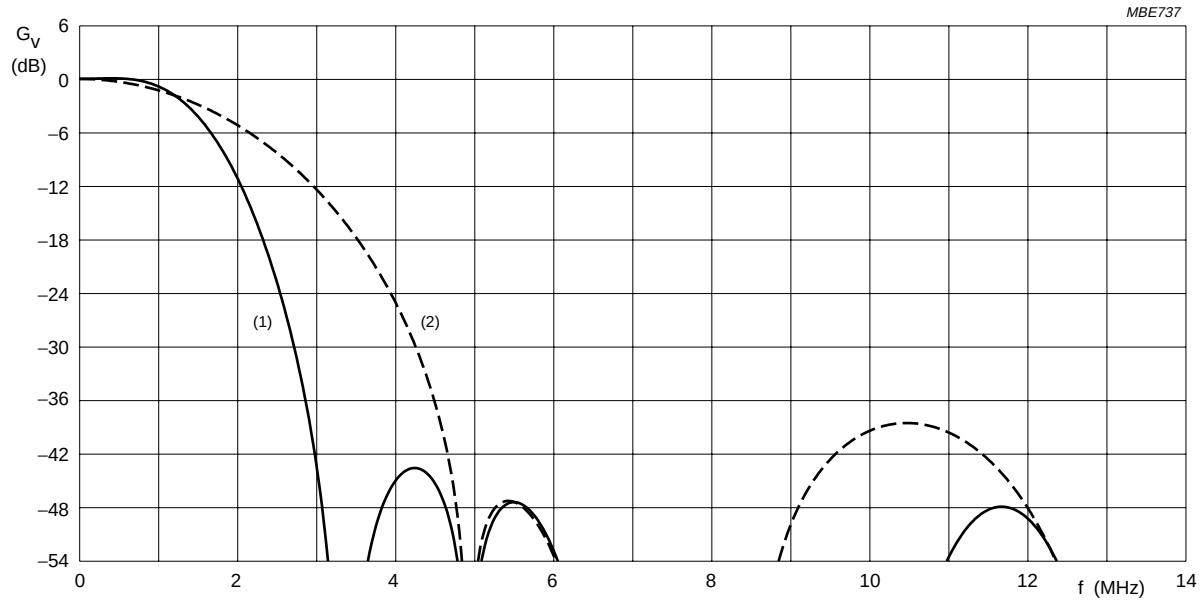
7.10 Slave transmitter

Table 40 Slave transmitter (slave address 89H or 8DH)

REGISTER FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte	–	VER2	VER1	VER0	CCRDO	CCRDE	FSEQ2	FSEQ1	O_E

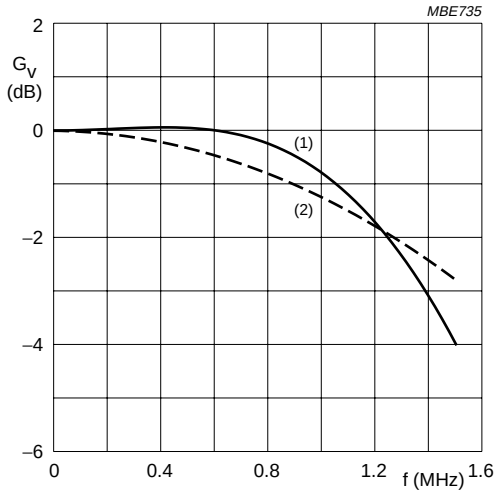
Table 41 No subaddress

DATA BYTE	LOGIC LEVEL	DESCRIPTION
VER	–	version identification of the device: it will be changed with all versions of the IC that have different programming models; current version is 001 binary
CCRDO	1	closed caption bytes of the odd field have been encoded
	0	the bit is reset after information has been written to the subaddresses 67H and 68H; it is set immediately after the data has been encoded
CCRDE	1	closed caption bytes of the even field have been encoded
	0	the bit is reset after information has been written to the subaddresses 69H and 6AH; it is set immediately after the data has been encoded
FSEQ	–	state of the internal field sequence counter, with bit O_E as LSB (repetition rate: NTSC = 4 fields, PAL = 8 fields)
O_E	1	during even field
	0	during odd field



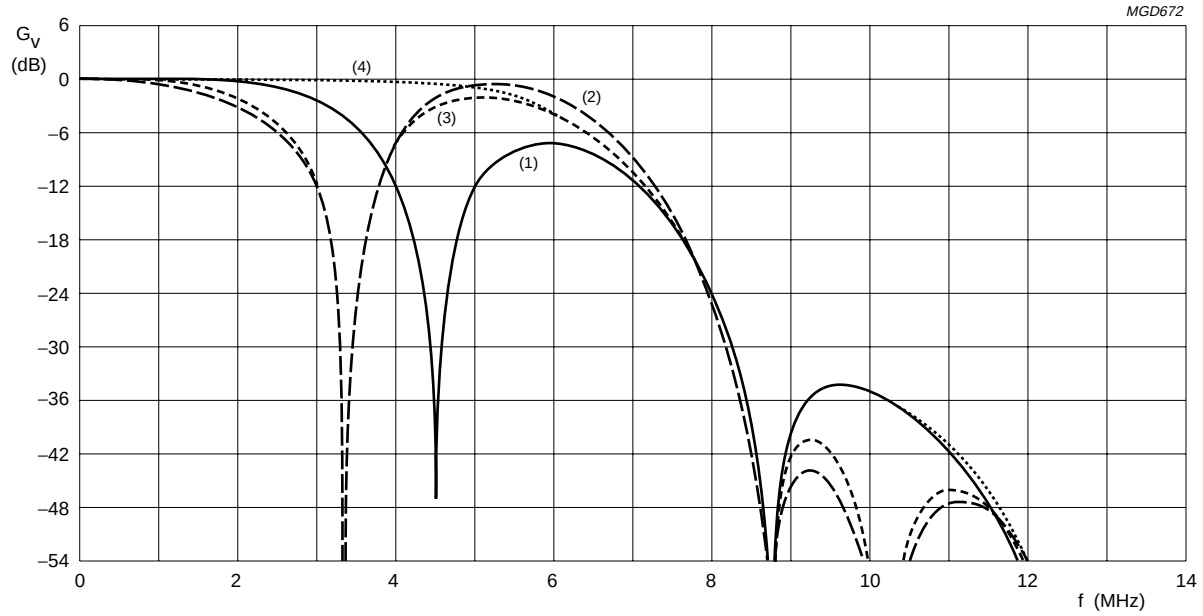
(1) SCBW = 1.
(2) SCBW = 0.

Fig.3 Chrominance transfer characteristic 1.



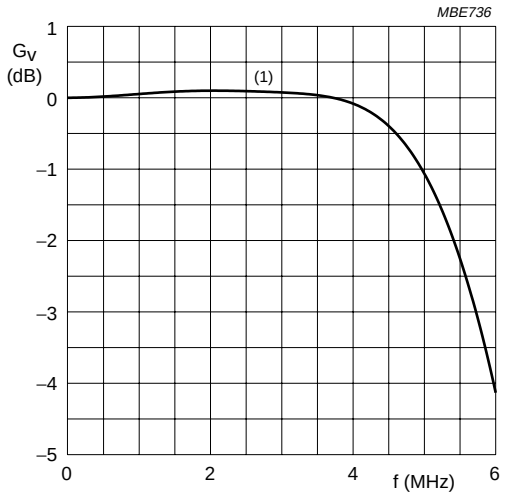
(1) SCBW = 1.
(2) SCBW = 0.

Fig.4 Chrominance transfer characteristic 2.



(1) CCRS1 = 0; CCRS0 = 1.
(2) CCRS1 = 1; CCRS0 = 0.
(3) CCRS1 = 1; CCRS0 = 1.
(4) CCRS1 = 0; CCRS0 = 0.

Fig.5 Luminance transfer characteristic 1.



(1) CCRS1 = 0; CCRS0 = 0.

Fig.6 Luminance transfer characteristic 2.

8 CHARACTERISTICS

V_{DDD} = 3.0 to 3.6 V; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Supply					
V_{DDA}	analog supply voltage		3.1	3.5	V
V_{DDD}	digital supply voltage		3.0	3.6	V
I_{DDA}	analog supply current	note 1	–	62	mA
I_{DDD}	digital supply current	V_{DDD} = 3.3 V; note 1	–	45	mA
Inputs: LLC, RCV1, RCV2, MP7 to MP0, RTCI, SA, $\overline{\text{RESET}}$ and TTX					
V_{IL}	LOW-level input voltage		−0.5	+0.8	V
V_{IH}	HIGH-level input voltage		2.0	V_{DDD} + 0.3	V
I_{LI}	input leakage current		–	1	µA
C_i	input capacitance	clocks	–	10	pF
		data	–	8	pF
		I/Os at high-impedance	–	8	pF
Outputs: RCV1, RCV2 and TTXRQ					
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	–	0.4	V
V_{OH}	HIGH-level output voltage	I_{OH} = −2 mA	2.4	–	V
I²C-bus: SDA and SCL					
V_{IL}	LOW-level input voltage		−0.5	$+0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	V_{DDD} + 0.3	V
I_i	input current	V_i = LOW or HIGH	−10	+10	µA
V_{OL}	LOW-level output voltage (pin SDA)	I_{OL} = 3 mA	–	0.4	V
I_o	output current	during acknowledge	3	–	mA
Clock timing: LLC					
T_{LLC}	cycle time	note 2	34	41	ns
δ	duty factor t_{HIGH}/T_{LLC}	note 3	40	60	%
t_r	rise time	note 2	–	5	ns
t_f	fall time	note 2	–	6	ns
Input timing: RCV1, RCV2, MP7 to MP0, RTCI, SA and TTX					
$t_{SU;DAT}$	input data set-up time		6	–	ns
$t_{HD;DAT}$	input data hold time		3	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Crystal oscillator					
f_n	nominal frequency (usually 27 MHz)	3rd harmonic	–	30	MHz
$\Delta f/f_n$	permissible deviation of nominal frequency	note 4	-50×10^{-6}	$+50 \times 10^{-6}$	
CRYSTAL SPECIFICATION					
T_{amb}	ambient temperature		0	70	°C
C_L	load capacitance		8	–	pF
R_S	series resistance		–	80	Ω
C_1	motional capacitance (typical)		1.5 – 20%	1.5 + 20%	fF
C_0	parallel capacitance (typical)		3.5 – 20%	3.5 + 20%	pF
Data and reference signal output timing					
C_L	output load capacitance		7.5	40	pF
t_h	output hold time		4	–	ns
t_d	output delay time		–	25	ns
C, Y and CVBS outputs					
$V_{o(p-p)}$	output signal voltage (peak-to-peak value)	note 5	1.25	1.50	V
R_{int}	internal serial resistance		1	3	Ω
R_L	output load resistance		75	300	Ω
B	output signal bandwidth of DACs	–3 dB	10	–	MHz
$LE_{lf(i)}$	low frequency integral linearity error of DACs		–	±3	LSB
$LE_{lf(d)}$	low frequency differential linearity error of DACs		–	±1	LSB

Notes

1. At maximum supply voltage with highly active input signals.
2. The data is for both input and output direction.
3. With LLC in input mode. In output mode, with a crystal connected to XTALO/XTALI duty factor is typically 50%.
4. If an internal oscillator is used, crystal deviation of nominal frequency is directly proportional to the deviation of subcarrier frequency and line/field frequency.
5. For full digital range, without load, V_{DDA} = 3.3 V. The typical voltage swing is 1.35 V, the typical minimum output voltage (digital zero at DAC) is 0.2 V.

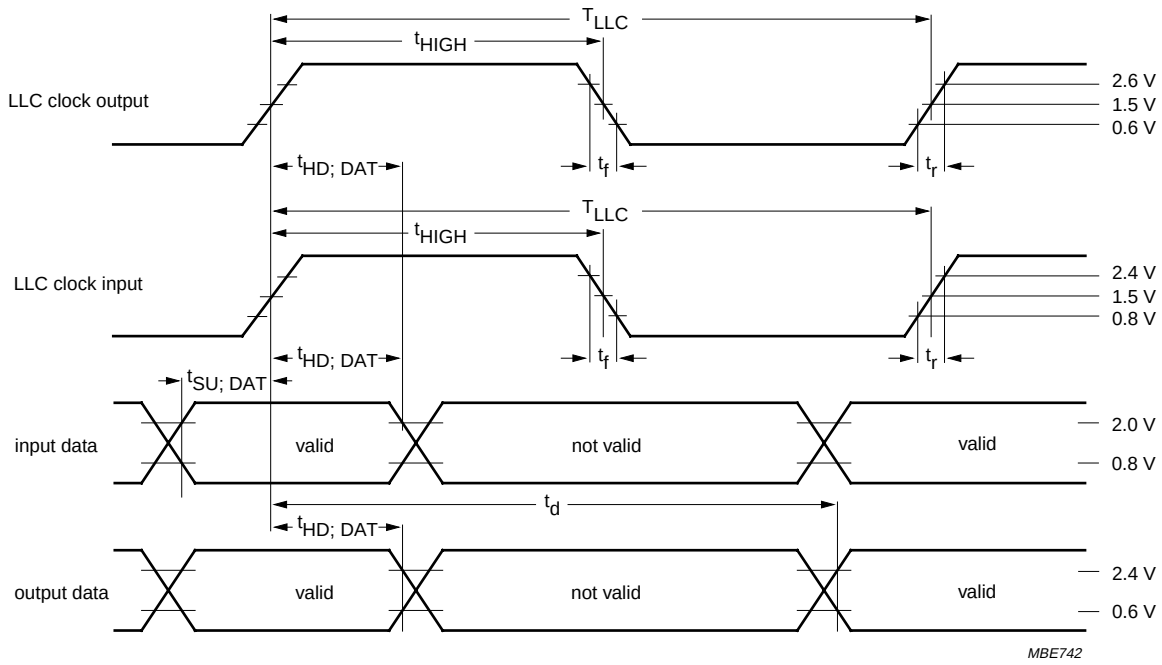
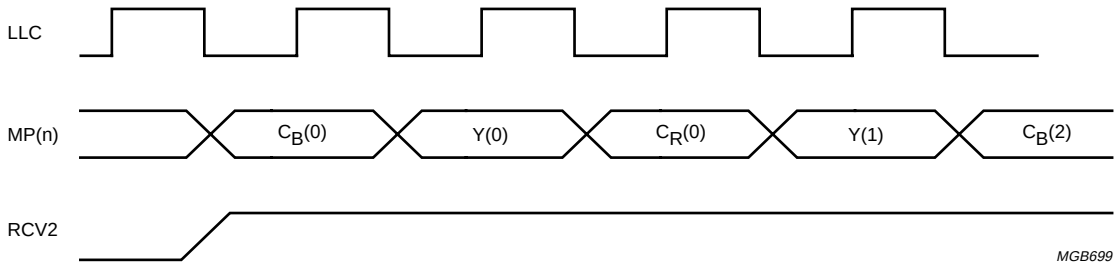


Fig.7 Clock data timing.



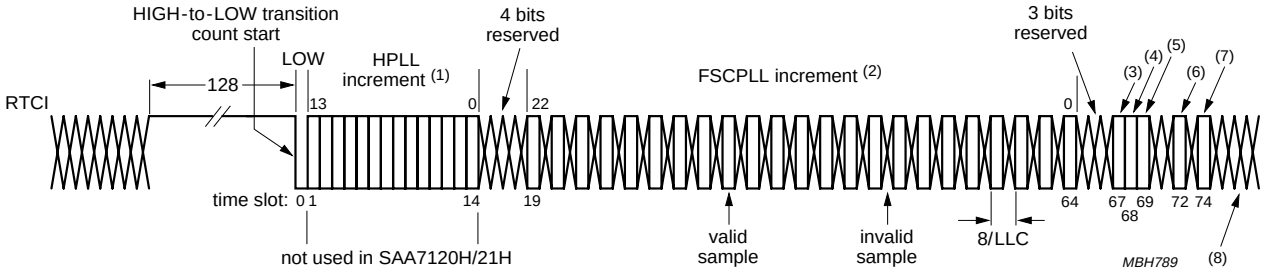
The data demultiplexing phase is coupled to the internal horizontal phase.
The phase of the RCV2 signal is programmed to 262 for 50 Hz and to 234 for 60 Hz in this example in output mode (RCV2S).

Fig.8 Functional timing.

8.1 Explanation of RTCI data bits

1. The HPLL increment is not evaluated by the SAA7120H; SAA7121H.
2. The SAA7120H; SAA7121H generates the subcarrier frequency from the FSCPLL increment if enabled (see item 7.).
3. The PAL bit indicates the line with inverted (R − Y) component of colour difference signal.
4. If the reset bit is enabled (RTCE = 1; DECPH = 1; PHRES = 00), the phase of the subcarrier is reset in each line whenever the reset bit of RTCI input is set to logic 1.
5. If the FISE bit is enabled (RTCE = 1; DECFIS = 1), the SAA7120H; SAA7121H takes this bit instead of the FISE bit in subaddress 61H.
6. If the odd/even bit is enabled (RTCE = 1; DECOE = 1), the SAA7120H; SAA7121H ignores its internally generated odd/even flag and takes the odd/even bit from RTCI input.
7. If the colour detection bit is enabled (RTCE = 1; DECCOL = 1) and no colour was detected (colour detection bit = 0), the subcarrier frequency is generated by the SAA7120H; SAA7121H. In the other case (colour detection bit = 1) the subcarrier frequency is evaluated out of FSCPLL increment.

   If the colour detection bit is disabled (RTCE = 1; DECCOL = 0), the subcarrier frequency is evaluated out of FSCPLL increment, independent of the colour detection bit of RTCI input.



(1) SAA7111/12 provides 14 to 0 bits, resulting in 2 reserved bits before FSCPLL increment.
(2) SAA7151 provides 21 to 0 bits only, resulting in 5 reserved bits before sequence bit.
(3) Sequence bit: PAL: 0 = (R − Y) line normal, 1 = (R − Y) line inverted; NTSC: 0 = no change.
(4) Reset bit: only from SAA7111 and SAA7112 decoder.
(5) FISE bit: 0 = 50 Hz, 1 = 60 Hz.
(6) Odd/even bit: odd_even from external.
(7) Colour detection: 0 = no colour detected, 1 = colour detected.
(8) Reserved bits: 229 with 50 Hz systems, 226 with 60 Hz systems.

Fig.9 RTCI timing.

8.2 Teletext timing

Time t_{FD} is the time needed to interpolate input data TTX and insert it into the CVBS and Y output signal, such that it appears at t_{TTX} = 9.78 µs (PAL) or t_{TTX} = 10.5 µs (NTSC) after the leading edge of the horizontal synchronization pulse.

Time t_{PD} is the pipeline delay time introduced by the source that is gated by TTXRQ in order to deliver TTX data. This delay is programmable by register TTXHD. For every active HIGH state at output pin TTXRQ, a new teletext bit must be provided by the source.

Since the beginning of the pulses representing the TTXRQ signal and the delay between the rising edge of TTXRQ and valid teletext input data are fully programmable (TTXHS and TTXHD), the TTX data is always inserted at the correct position after the leading edge of outgoing horizontal synchronization pulse.

Time t_{TTXWin} is the internally used insertion window for TTX data; it has a constant length that allows insertion of 360 teletext bits at a text data rate of 6.9375 Mbits/s (PAL), 296 teletext bits at a text data rate of 5.7272 Mbits/s (WST) or 288 teletext bits at a text data rate of 5.7272 Mbits/s (NABTS). The insertion window is not opened if the control bit TTXEN is logic 0.

Using appropriate programming, all suitable lines of the odd field (TTXOVS and TTXOVE) plus all suitable lines of the even field (TTXEVS and TTXEVE) can be used for teletext insertion.

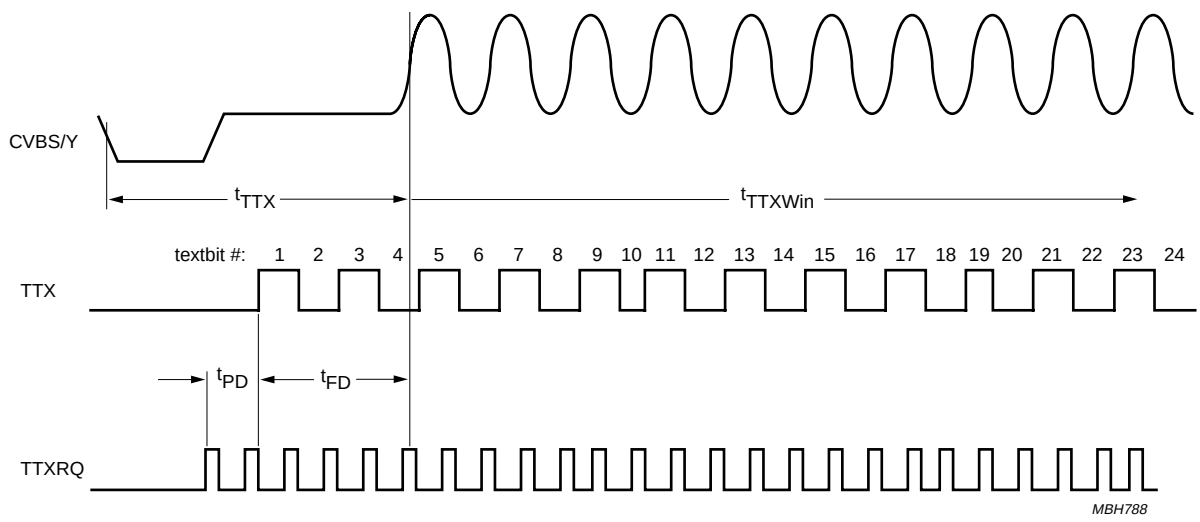


Fig.10 Teletext timing.

9 APPLICATION INFORMATION

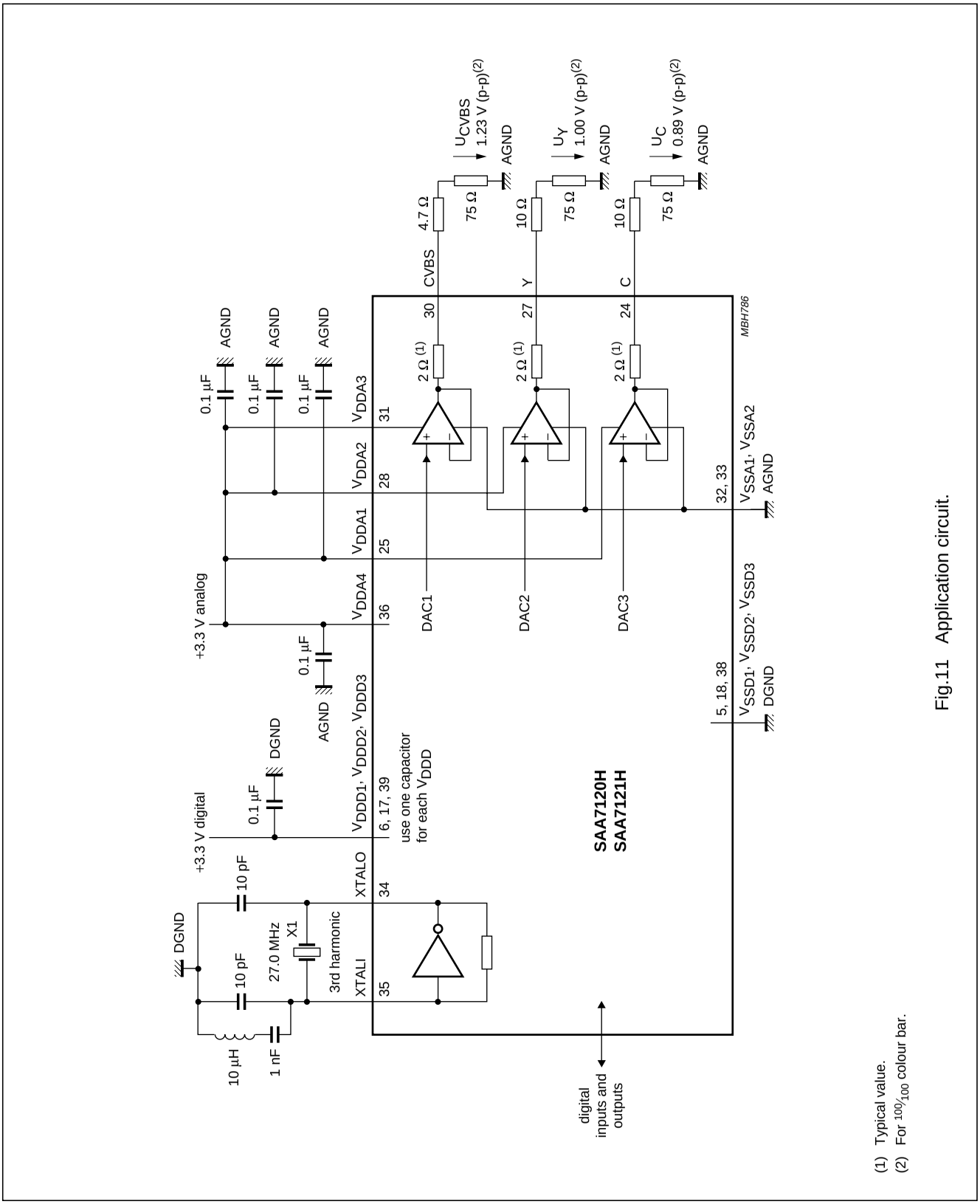


Fig.11 Application circuit.

(1) Typical value.
(2) For $^{100}/_{100}$ colour bar.

9.1 Analog output voltages

The analog output voltages are dependent on the open-loop voltage of the operational amplifiers for full-scale conversion (typical value 1.35 V), the internal series resistor (typical value 2 Ω), the external series resistor and the external load impedance.

The digital output signals in front of the DACs under nominal conditions occupy different conversion ranges, as indicated in Table 42 for a $^{100}/_{100}$ colour bar signal.

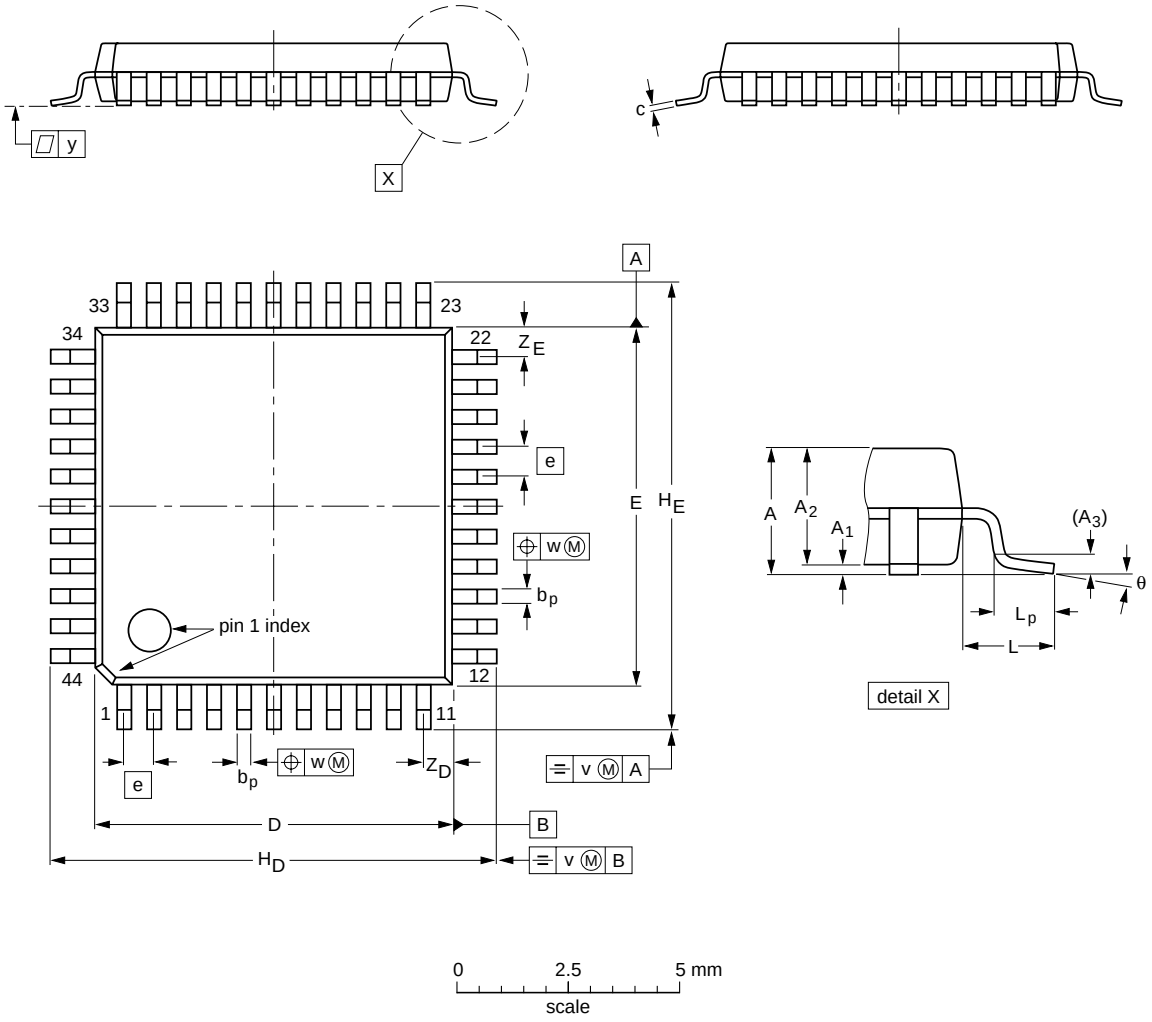
Values for the external series resistors result in a 75 Ω load.

Table 42 Digital output signals conversion range

CONVERSION RANGE (peak-to-peak)	
CVBS SYNC-TIP TO PEAK-CARRIER (digits)	**Y (VBS) SYNC-TIP TO WHITE (digits)**
1016	881

10 PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm **SOT307-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						~~95-02-04~~ 97-08-01

11 SOLDERING

11.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

11.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

11.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

11.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

11.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, TFBGA, VFBGA	not suitable	suitable
HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[3]	suitable
PLCC[4], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[4][5]	suitable
SSOP, TSSOP, VSO	not recommended[6]	suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
4. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
5. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
6. Wave soldering is suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

12 DATA SHEET STATUS

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