DATA SHEET



SAA7104H; SAA7105H
Digital video encoder

Product specification

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1 FEATURES



- Digital PAL/NTSC encoder with integrated high quality scaler and anti-flicker filter for TV output from a PC
- Supports Intel® Digital Video Out (DVO) low voltage interfacing to graphics controller
- 27 MHz crystal-stable subcarrier generation
- Maximum graphics pixel clock 85 MHz at double edged clocking, synthesized on-chip or from external source
- Programmable assignment of clock edge to bytes (in double edged mode)
- Synthesizable pixel clock (PIXCLK) with minimized output jitter, can be used as reference clock for the VGC, as well)
- PIXCLK output and bi-phase PIXCLK input (VGC clock loop-through possible)
- Hot-plug detection through dedicated interrupt pin
- Supported VGA resolutions for PAL or NTSC legacy video output up to 1280×1024 graphics data at 60 or 50 Hz frame rate
- Supported VGA resolutions for HDTV output up to 1920×1080 interlaced graphics data at 60 or 50 Hz frame rate
- Three Digital-to-Analog Converters (DACs) for CVBS (BLUE, C_B), VBS (GREEN, CVBS) and C (RED, C_R) at 27 MHz sample rate (signals in parenthesis are optionally), all at 10-bit resolution
- Non-interlaced C_B-Y-C_R or RGB input at maximum 4 : 4 : 4 sampling
- Downscaling and upscaling from 50 to 400%
- Optional interlaced C_B-Y-C_R input of Digital Versatile Disk (DVD) signals
- Optional non-interlaced RGB output to drive second VGA monitor (bypass mode, maximum 85 MHz)
- 3×256 bytes RGB Look-Up Table (LUT)
- Support for hardware cursor
- HDTV up to 1920×1080 interlaced and 1280×720 progressive, including 3-level sync pulses
- Programmable border colour of underscan area
- Programmable 5 line anti-flicker filter
- On-chip 27 MHz crystal oscillator (3rd-harmonic or fundamental 27 MHz crystal)
- Fast I^2C-bus control port (400 kHz)
- Encoder can be master or slave
- Adjustable output levels for the DACs
- Programmable horizontal and vertical input synchronization phase
- Programmable horizontal sync output phase
- Internal Colour Bar Generator (CBG)
- Optional support of various Vertical Blanking Interval (VBI) data insertion
- Macrovision™(1) Pay-per-View copy protection system rev. 7.01, rev. 6.1 and rev. 1.03 (525p) as option; this applies to the SAA7104H only. The device is protected by USA patent numbers 4631603, 4577216 and 4819098 and other intellectual property rights. Use of the Macrovision anti-copy process in the device is licensed for non-commercial home use only. Reverse engineering or disassembly is prohibited. Please contact your nearest Philips Semiconductors sales office for more information.
- Optional cross-colour reduction for PAL and NTSC CVBS outputs
- Power-save modes
- Joint Test Action Group (JTAG) boundary scan test
- Monolithic CMOS 3.3 V device, 5 V tolerant I/Os
- QFP64 package.

(1) Macrovision™ is a trademark of the Macrovision Corporation.

2 GENERAL DESCRIPTION

The SAA7104H; SAA7105H is an advanced next-generation video encoder which converts PC graphics data at maximum 1280×1024 resolution (optionally 1920×1080 interlaced) to PAL (50 Hz) or NTSC (60 Hz) video signals. A programmable scaler and anti-flicker filter (maximum 5 lines) ensures properly sized and flicker-free TV display as CVBS or S-video output.

Alternatively, the three Digital-to-Analog Converters (DACs) can output RGB signals together with a TTL composite sync to feed SCART connectors.

When the scaler/interlacer is bypassed, a second VGA monitor can be connected to the RGB outputs and separate H and V-syncs as well, thereby serving as an auxiliary monitor at maximum 1280×1024 resolution/60 Hz (PIXCLK < 85 MHz). Alternatively this port can provide Y, P_B and P_R signals for HDTV monitors.

The device includes a sync/clock generator and on-chip DACs.

All inputs intended to interface to the host graphics controller are designed for low-voltage signals between down to 1.1 V and up to 3.6 V.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DDA}	analog supply voltage	3.15	3.3	3.45	V
V_{DDD}	digital supply voltage	3.15	3.3	3.45	V
I_{DDA}	analog supply current	1	110	115	mA
I_{DDD}	digital supply current	1	175	200	mA
V_i	input signal voltage levels	TTL compatible			
$V_{o(p-p)}$	analog CVBS output signal voltage for a 100/100 colour bar at 75/2 Ω load (peak-to-peak value)	–	1.23	–	V
R_L	load resistance	–	37.5	–	Ω
$ILE_{lf(DAC)}$	low frequency integral linearity error of DACs	–	–	±3	LSB
$DLE_{lf(DAC)}$	low frequency differential linearity error of DACs	–	–	±1	LSB
T_{amb}	ambient temperature	0	–	70	°C

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7104H	QFP64	plastic quad flat package; 64 leads (lead length 1.6 mm); body $14 \times 14 \times 2.7$ mm	SOT393-1
SAA7105H			

5 BLOCK DIAGRAM

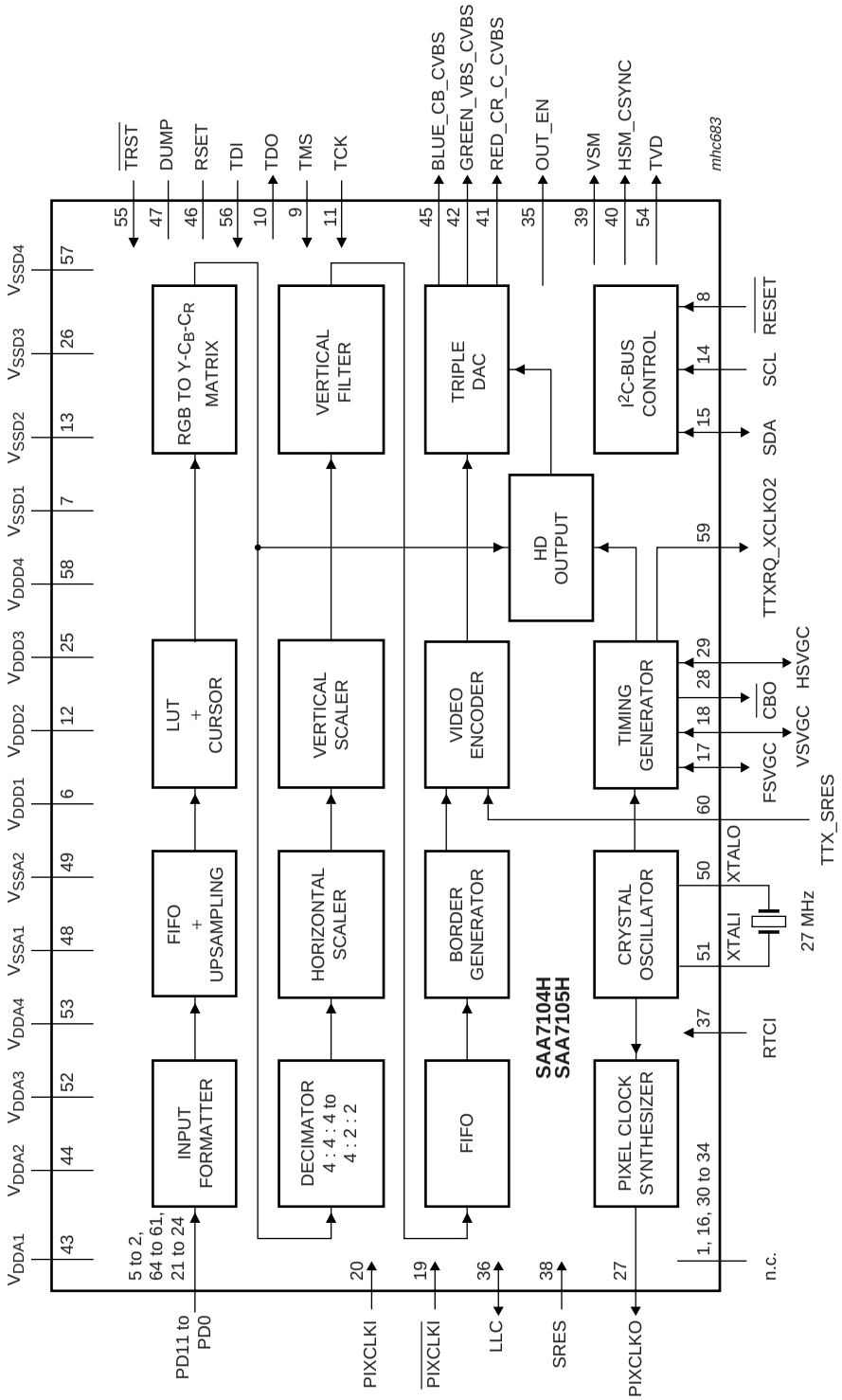


Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	TYPE[1]	DESCRIPTION
n.c.	1	–	not connected
PD8	2	I	see Tables 8 to 13 for pin assignment
PD9	3	I	see Tables 8 to 13 for pin assignment
PD10	4	I	see Tables 8 to 13 for pin assignment
PD11	5	I	see Tables 8 to 13 for pin assignment
V_{DDD1}	6	S	digital supply voltage 1 for pins PD11 to PD0, PIXCLKI, $\overline{\text{PIXCLKI}}$, PIXCLKO, FSVGC, VSVGC, HSVGC, $\overline{\text{CBO}}$ and TVD
V_{SSD1}	7	S	digital ground 1
$\overline{\text{RESET}}$	8	I	reset input; active LOW
TMS	9	I/pu	test mode select input for Boundary Scan Test (BST); note 2
TDO	10	O	test data output for BST; note 2
TCK	11	I/pu	test clock input for BST; note 2
V_{DDD2}	12	S	digital supply voltage 2 (3.3 V for I/Os)
V_{SSD2}	13	S	digital ground 2
SCL	14	I	I^2C-bus serial clock input
SDA	15	I/O	I^2C-bus serial data input/output
n.c.	16	–	not connected
FSVGC	17	I/O	frame synchronization output to Video Graphics Controller (VGC) (optional input); note 3
VSVGC	18	I/O	vertical synchronization output to VGC (optional input); note 3
$\overline{\text{PIXCLKI}}$	19	I	inverted pixel clock input
PIXCLKI	20	I	pixel clock input (looped through)
PD3	21	I	MSB – 4 with C_B-Y-C_R 4 : 2 : 2; see Tables 8 to 13 for pin assignment
PD2	22	I	MSB – 5 with C_B-Y-C_R 4 : 2 : 2; see Tables 8 to 13 for pin assignment
PD1	23	I	MSB – 6 with C_B-Y-C_R 4 : 2 : 2; see Tables 8 to 13 for pin assignment
PD0	24	I	MSB – 7 with C_B-Y-C_R 4 : 2 : 2; see Tables 8 to 13 for pin assignment
V_{DDD3}	25	S	digital supply voltage 3 (3.3 V for core)
V_{SSD3}	26	S	digital ground 3
PIXCLKO	27	O	pixel clock output to VGC
$\overline{\text{CBO}}$	28	I/O	composite blanking output to VGC; active LOW; note 3
HSVGC	29	I/O	horizontal synchronization output to VGC (optional input); note 3
n.c.	30	–	not connected
n.c.	31	–	not connected
n.c.	32	–	not connected
n.c.	33	–	not connected
n.c.	34	–	not connected
OUT_EN	35	I/pu	if HIGH (default by pull-up): LLC, RTCI and SRES are outputs; if LOW: LLC, RTCI and SRES are inputs
LLC	36	I/O	line-locked clock
RTCI	37	I/O	real-time control input

SYMBOL	PIN	TYPE[1]	DESCRIPTION
SRES	38	I/O	sync reset input
VSM	39	O	vertical synchronization output to monitor (non-interlaced auxiliary RGB)
HSM_CSYNC	40	O	horizontal synchronization output to monitor (non-interlaced auxiliary RGB) or composite sync for RGB-SCART
RED_CR_C_CVBS	41	O	analog output of RED or C_R or C or CVBS signal
GREEN_VBS_CVBS	42	O	analog output of GREEN or VBS or CVBS signal
V_{DDA1}	43	S	analog supply voltage 1 (3.3 V for DACs)
V_{DDA2}	44	S	analog supply voltage 2 (3.3 V for DACs)
BLUE_CB_CVBS	45	O	analog output of BLUE or C_B or CVBS signal
RSET	46	O	DAC reference pin; connected via 1 kΩ resistor to analog ground (do not use capacitor in parallel with 1 kΩ resistor)
DUMP	47	O	DAC reference pin; connected via 12 Ω resistor to analog ground
V_{SSA1}	48	S	analog ground 1
V_{SSA2}	49	S	analog ground 2
XTALO	50	O	crystal oscillator output
XTALI	51	I	crystal oscillator input
V_{DDA3}	52	S	analog supply voltage 3 (3.3 V for oscillator)
V_{DDA4}	53	S	analog supply voltage 4 (3.3 V)
TVD	54	O	interrupt if TV is detected at DAC output
$\overline{TRST}$	55	I/pu	test reset input for BST; active LOW; notes 2, 4 and 5
TDI	56	I	test data input for BST; note 2
V_{SSD4}	57	S	digital ground 4
V_{DDD4}	58	S	digital supply voltage 4 (3.3 V for core)
TTXRQ_XCLKO2	59	O	teletext request output or 13.5 MHz clock output of the crystal oscillator; note 3
TTX_SRES	60	I	teletext input or sync reset input
PD4	61	I	MSB – 3 with C_B-Y-C_R 4 : 2 : 2; see Tables 8 to 13 for pin assignment
PD5	62	I	MSB – 2 with C_B-Y-C_R 4 : 2 : 2; see Tables 8 to 13 for pin assignment
PD6	63	I	MSB – 1 with C_B-Y-C_R 4 : 2 : 2; see Tables 8 to 13 for pin assignment
PD7	64	I	MSB with C_B-Y-C_R 4 : 2 : 2; see Tables 8 to 13 for pin assignment

Notes

1. Pin type: I = input, O = output, S = supply, pu = pull-up.
2. In accordance with the *"IEEE1149.1"* standard the pins TDI, TMS, TCK and $\overline{TRST}$ are input pins with an internal pull-up resistor and TDO is a 3-state output pin.
3. The pins FSVGC, VSVGC, $\overline{CBO}$, HSVGC and TTXRQ_XCLKO2 are used for bootstrapping; see Section 7.1.
4. For board design without boundary scan implementation connect $\overline{TRST}$ to ground.
5. This pin provides easy initialization of the Boundary Scan Test (BST) circuit. $\overline{TRST}$ can be used to force the Test Access Port (TAP) controller to the TEST_LOGIC_RESET state (normal operation) at once.

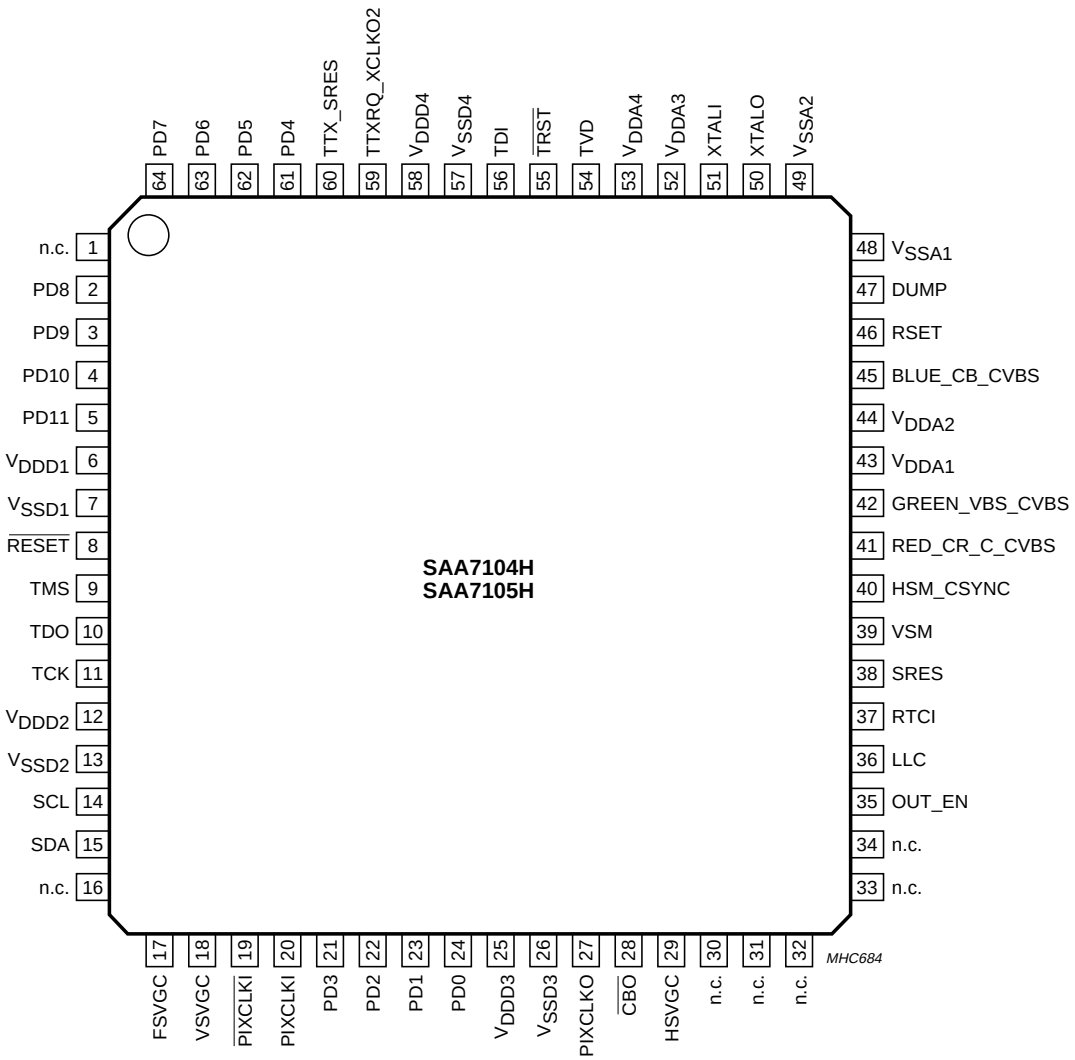


Fig.2 Pin configuration.

7 FUNCTIONAL DESCRIPTION

The digital video encoder encodes digital luminance and colour difference signals (C_B-Y-C_R) or digital RGB signals into analog CVBS, S-video and, optionally, RGB or C_R-Y-C_B signals. NTSC M, PAL B/G and sub-standards are supported.

The SAA7104H; SAA7105H can be directly connected to a PC video graphics controller with a maximum resolution of 1280×1024 (progressive) or 1920×1080 (interlaced) at a 50 or 60 Hz frame rate. A programmable scaler scales the computer graphics picture so that it will fit into a standard TV screen with an adjustable underscan area. Non-interlaced-to-interlaced conversion is optimized with an adjustable anti-flicker filter for a flicker-free display at a very high sharpness.

Besides the most common 16-bit 4 : 2 : 2 C_B-Y-C_R input format (using 8 pins with double edge clocking), other C_B-Y-C_R and RGB formats are also supported; see Tables 8 to 13.

A complete 3×256 bytes Look-Up Table (LUT), which can be used, for example, as a separate gamma corrector, is located in the RGB domain; it can be loaded either through the video input port PD (Pixel Data) or via the I^2C-bus.

The SAA7104H; SAA7105H supports a $32 \times 32 \times 2$-bit hardware cursor, the pattern of which can also be loaded through the video input port or via the I^2C-bus.

It is also possible to encode interlaced 4 : 2 : 2 video signals such as PC-DVD; for that the anti-flicker filter, and in most cases the scaler, will simply be bypassed.

Besides the applications for video output, the SAA7104H; SAA7105H can also be used for generating a kind of auxiliary VGA output, when the RGB non-interlaced input signal is fed to the DACs. This may be of interest for example, when the graphics controller provides a second graphics window at its video output port.

The basic encoder function consists of subcarrier generation, colour modulation and insertion of synchronization signals at a crystal-stable clock rate of 13.5 MHz (independent of the actual pixel clock used at the input side), corresponding to an internal 4 : 2 : 2 bandwidth in the luminance/colour difference domain. Luminance and chrominance signals are filtered in accordance with the standard requirements of *"RS-170-A"* and *"ITU-R BT.470-3"*.

For ease of analog post filtering the signals are twice oversampled to 27 MHz before digital-to-analog conversion.

The total filter transfer characteristics (scaler and anti-flicker filter are not taken into account) are illustrated in Figs 4 to 9. All three DACs are realized with full 10-bit resolution. The C_R-Y-C_B to RGB dematrix can be bypassed (optionally) in order to provide the upsampled C_R-Y-C_B input signals.

The 8-bit multiplexed C_B-Y-C_R formats are *"ITU-R BT.656"* (D1 format) compatible, but the SAV and EAV codes can be decoded optionally, when the device is operated in slave mode. For assignment of the input data to the rising or falling clock edge see Tables 8 to 13.

In order to display interlaced RGB signals through a euro-connector TV set, a separate digital composite sync signal (pin HSM_CSYNC) can be generated; it can be advanced up to 31 periods of the 27 MHz crystal clock in order to be adapted to the RGB processing of a TV set.

The SAA7104H; SAA7105H synthesizes all necessary internal signals, colour subcarrier frequency and synchronization signals from that clock.

It is also possible to connect a Philips digital video decoder (e.g. SAA7114H), using its line-locked clock for re-encoding. Information containing actual subcarrier, PAL-ID etc. is provided via pin RTCI which is connected to pin RTCO of the decoder.

Wide screen signalling data can be loaded via the I^2C-bus and is inserted into line 23 for standards using a 50 Hz field rate.

VPS data for program dependent automatic start and stop of such featured VCRs is loadable via the I^2C-bus.

The IC also contains Closed Caption and extended data services encoding (line 21), and supports teletext insertion for the appropriate bit stream format at a 27 MHz clock rate (see Fig.15). It is also possible to load data for the copy generation management system into line 20 of every field (525/60 line counting).

A number of possibilities are provided for setting different video parameters such as:

- Black and blanking level control
- Colour subcarrier frequency
- Variable burst amplitude etc.

7.1 Reset conditions

To activate the reset a pulse at least of 2 crystal clocks duration is required.

During reset ($\overline{\text{RESET}}$ = LOW) plus an extra 32 crystal clock periods, FSVGC, VSVGC, $\overline{\text{CBO}}$, HSVGC and TTX_SRES are set to input mode and HSM_CSYNC and VSM are set to 3-state. A reset also forces the I²C-bus interface to abort any running bus transfer and sets it into receive condition.

After reset, the state of the I/Os and other functions is defined by the strapping pins until an I²C-bus access redefines the corresponding registers; see Table 1.

Table 1 Strapping pins

PIN	TIED	PRESET
FSVGC	LOW	NTSC M encoding, PIXCLK fits to 640 × 480 graphics input
	HIGH	PAL B/G encoding, PIXCLK fits to 640 × 480 graphics input
VSVGC	LOW	4 : 2 : 2 Y-C_B-C_R graphics input (format 0)
	HIGH	4 : 4 : 4 RGB graphics input (format 3)
$\overline{\text{CBO}}$	LOW	input demultiplex phase: LSB = LOW
	HIGH	input demultiplex phase: LSB = HIGH
HSVGC	LOW	input demultiplex phase: MSB = LOW
	HIGH	input demultiplex phase: MSB = HIGH
TTXRQ_XCLKO2	LOW	slave (FSVGC, VSVGC and HSVGC are inputs, internal colour bar is active)
	HIGH	master (FSVGC, VSVGC and HSVGC are outputs)

7.2 Input formatter

The input formatter converts all accepted PD input data formats, either RGB or Y-C_B-C_R, to a common internal RGB or Y-C_B-C_R data stream.

When double-edge clocking is used, the data is internally split into portions PPD1 and PPD2. The clock edge assignment must be set according to the I²C-bus control bits SLOT and EDGE for correct operation.

If Y-C_B-C_R is being applied as a 27 Mbyte/s data stream, the output of the input formatter can be used directly to feed the video encoder block.

The horizontal upscaling is supported via the input formatter. According to the programming of the pixel clock dividers (see Section 7.10), it will sample up the data stream to 1 ×, 2 × or 4 × the input data rate. An optional interpolation filter is available. The clock domain transition is handled by a 4 entries wide FIFO which gets initialized every field or explicitly at request. A bypass for the FIFO is available, especially for high input data rates.

7.3 RGB LUT

The three 256 byte RAMs of this block can be addressed by three 8-bit wide signals, thus it can be used to build any transformation, e.g. a gamma correction for RGB signals. In the event that the indexed colour data is applied, the RAMs are addressed in parallel.

The LUTs can either be loaded by an I²C-bus write access or can be part of the pixel data input through the PD port. In the latter case, 256 × 3 bytes for the R, G and B LUT are expected at the beginning of the input video line, two lines before the line that has been defined as first active line, until the middle of the line immediately preceding the first active line. The first 3 bytes represent the first RGB LUT data, and so on.

7.4 Cursor insertion

A 32 × 32 dots cursor can be overlaid as an option; the bit map of the cursor can be uploaded by an I²C-bus write access to specific registers or in the pixel data input through the PD port. In the latter case, the 256 bytes defining the cursor bit map (2 bits per pixel) are expected immediately following the last RGB LUT data in the line preceding the first active line.

The cursor bit map is set up as follows: each pixel occupies 2 bits. The meaning of these bits depends on the CMODE I²C-bus register as described in Table 4. Transparent means that the input pixels are passed through, the ‘cursor colours’ can be programmed in separate registers.

The bit map is stored with 4 pixels per byte, aligned to the least significant bit. So the first pixel is in bits 0 and 1, the next pixel in bits 3 and 4 and so on. The first index is the column, followed by the row; index 0,0 is the upper left corner.

Table 2 Layout of a byte in the cursor bit map

D7	D6	D5	D4	D3	D2	D1	D0
pixel n + 3		pixel n + 2		pixel n + 1		pixel n	
D1	D0	D1	D0	D1	D0	D1	D0

For each direction, there are 2 registers controlling the position of the cursor, one controls the position of the ‘hot spot’, the other register controls the insertion position. The hot spot is the ‘tip’ of the pointer arrow. It can have any position in the bit map. The actual position registers describe the co-ordinates of the hot spot. Again 0,0 is the upper left corner. While it is not possible to move the hot spot beyond the left respectively upper screen border this is perfectly legal for the right respectively lower border. It should be noted that the cursor position is described relative to the input resolution.

Table 3 Cursor bit map

BYTE	D7	D6	D5	D4	D3	D2	D1	D0
0	row 0 column 3		row 0 column 2		row 0 column 1		row 0 column 0	
1	row 0 column 7		row 0 column 6		row 0 column 5		row 0 column 4	
2	row 0 column 11		row 0 column 10		row 0 column 9		row 0 column 8	
...	...		...		...		...	
6	row 0 column 27		row 0 column 26		row 0 column 25		row 0 column 24	
7	row 0 column 31		row 0 column 30		row 0 column 29		row 0 column 28	
...	...		...		...		...	
254	row 31 column 27		row 31 column 26		row 31 column 25		row 31 column 24	
255	row 31 column 31		row 31 column 30		row 31 column 29		row 31 column 28	

Table 4 Cursor modes

CURSOR PATTERN	CURSOR MODE	
	CMODE = 0	CMODE = 1
00	second cursor colour	second cursor colour
01	first cursor colour	first cursor colour
10	transparent	transparent
11	inverted input	auxiliary cursor colour

7.5 RGB Y-C_B-C_R matrix

RGB input signals to be encoded to PAL or NTSC are converted to the Y-C_B-C_R colour space in this block. The colour difference signals are fed through low-pass filters and formatted to a ITU-R BT.601 like 4 : 2 : 2 data stream for further processing.

A gain adjust option corrects the level swing of the graphics world (black-to-white as 0 to 255) to the required range of 16 to 235.

The matrix and formatting blocks can be bypassed for Y-C_B-C_R graphics input.

When the auxiliary VGA mode is selected, the output of the cursor insertion block is immediately directed to the triple DAC.

7.6 Horizontal scaler

The high quality horizontal scaler operates on the 4 : 2 : 2 data stream. Its control engines compensate the colour phase offset automatically.

The scaler starts processing after a programmable horizontal offset and continues with a number of input pixels. Each input pixel is a programmable fraction of the current output pixel (XINC/4096). A special case is XINC = 0, this sets the scaling factor to 1.

If the SAA7104H; SAA7105H input data is in accordance with *“ITU-R BT.656”*, the scaler enters another mode. In this event, XINC needs to be set to 2048 for a scaling factor of 1. With higher values, upscaling will occur.

The phase resolution of the circuit is 12 bits, giving a maximum offset of 0.2 after 800 input pixels. Small FIFOs rearrange a 4 : 2 : 2 data stream at the scaler output.

7.7 Vertical scaler and anti-flicker filter

The functions scaling, Anti-Flicker Filter (AFF) and re-interlacing are implemented in the vertical scaler.

Besides the entire input frame, it receives the first and last lines of the border to allow anti-flicker filtering.

The circuit generates the interlaced output fields by scaling down the input frames with different offsets for odd and even fields. Increasing the YSKIP setting reduces the anti-flicker function. A YSKIP value of 4095 switches it off; see Table 85.

An additional, programmable vertical filter supports the anti-flicker function. This filter is not available at upscaling factors of more than 2.

The programming is similar to the horizontal scaler. For the re-interlacing, the resolutions of the offset registers are not sufficient, so the weighting factors for the first lines can also be adjusted. YINC = 0 sets the scaling factor to 1; YIWGTO and YIWGTE must not be 0.

Due to the re-interlacing, the circuit can perform upscaling by a maximum factor of 2. The maximum factor depends on the setting of the anti-flicker function and can be derived from the formulae given in Section 7.20.

An additional upscaling mode allows to increase the upscaling factor to maximum 4 as it is required for the old VGA modes like 320×240.

7.8 FIFO

The FIFO acts as a buffer to translate from the PIXCLK clock domain to the XTAL clock domain. The write clock is PIXCLK and the read clock is XTAL. An underflow or overflow condition can be detected via the I^2C-bus read access.

In order to avoid underflows and overflows, it is essential that the frequency of the synthesized PIXCLK matches to the input graphics resolution and the desired scaling factor.

7.9 Border generator

When the graphics picture is to be displayed as interlaced PAL, NTSC, S-video or RGB on a TV screen, it is desired in many cases not to lose picture information due to the inherent overscanning of a TV set. The desired amount of underscan area, which is achieved through appropriate scaling in the vertical and horizontal direction, can be filled in the border generator with an arbitrary true colour tint.

7.10 Oscillator and Discrete Time Oscillator (DTO)

The master clock generation is realized as a 27 MHz crystal oscillator, which can operate with either a fundamental wave crystal or a 3rd-harmonic crystal.

The crystal clock supplies the DTO of the pixel clock synthesizer, the video encoder and the I^2C-bus control block. It also usually supplies the triple DAC, with the exception of the auxiliary VGA or HDTV mode, where the triple DAC is clocked by the pixel clock (PIXCLK).

The DTO can be programmed to synthesize all relevant pixel clock frequencies between circa 40 and 85 MHz. Two programmable dividers provide the actual clock to be used externally and internally. The dividers can be programmed to factors of 1, 2, 4 and 8. For the internal pixel clock, a divider ratio of 8 makes no sense and is thus forbidden.

The internal clock can be switched completely to the pixel clock input. In this event, the input FIFO is useless and will be bypassed.

The entire pixel clock generation can be locked to the vertical frequency. Both pixel clock dividers get re-initialized every field. Optionally, the DTO can be cleared with each V-sync. At proper programming, this will make the pixel clock frequency a precise multiple of the vertical and horizontal frequencies. This is required for some graphic controllers.

7.11 Low-pass Clock Generation Circuit (CGC)

This block reduces the phase jitter of the synthesized pixel clock. It works as a tracking filter for all relevant synthesized pixel clock frequencies.

7.12 Encoder

7.12.1 VIDEO PATH

The encoder generates luminance and colour subcarrier output signals from the Y, C_B and C_R baseband signals, which are suitable for use as CVBS or separate Y and C signals.

Input to the encoder, at 27 MHz clock (e.g. DVD), is either originated from computer graphics at pixel clock, fed through the FIFO and border generator, or a ITU-R BT.656 style signal.

Luminance is modified in gain and in offset (the offset is programmable in a certain range to enable different black level set-ups). A blanking level can be set after insertion of a fixed synchronization pulse tip level, in accordance with standard composite synchronization schemes. Other manipulations used for the Macrovision anti-taping process, such as additional insertion of AGC super-white pulses (programmable in height), are supported by the SAA7104H only.

To enable easy analog post filtering, luminance is interpolated from a 13.5 MHz data rate to a 27 MHz data rate, thereby providing luminance in a 10-bit resolution. The transfer characteristics of the luminance interpolation filter are illustrated in Figs 6 and 7. Appropriate transients at start/end of active video and for synchronization pulses are ensured.

Chrominance is modified in gain (programmable separately for C_B and C_R), and a standard dependent burst is inserted, before baseband colour signals are interpolated from a 6.75 MHz data rate to a 27 MHz data rate. One of the interpolation stages can be bypassed, thus providing a higher colour bandwidth, which can be used for the Y and C output. The transfer characteristics of the chrominance interpolation filter are illustrated in Figs 4 and 5.

The amplitude (beginning and ending) of the inserted burst, is programmable in a certain range that is suitable for standard signals and for special effects. After the succeeding quadrature modulator, colour is provided on the subcarrier in 10-bit resolution.

The numeric ratio between the Y and C outputs is in accordance with the standards.

7.12.2 Teletext insertion and encoding (not simultaneously with real-time control)

Pin TTX_SRES receives a WST or NABTS teletext bitstream sampled at the crystal clock. At each rising edge of the output signal (TTXRQ) a single teletext bit has to be provided after a programmable delay at input pin TTX_SRES.

Phase variant interpolation is achieved on this bitstream in the internal teletext encoder, providing sufficient small phase jitter on the output text lines.

TTXRQ_XCLKO2 provides a fully programmable request signal to the teletext source, indicating the insertion period of bitstream at lines which can be selected independently for both fields. The internal insertion window for text is set to 360 (PAL WST), 296 (NTSC WST) or 288 (NABTS) teletext bits including clock run-in bits. The protocol and timing are illustrated in Fig.15.

Alternatively, this pin can be provided with a buffered crystal clock (XCLK) of 13.5 MHz.

7.12.3 Video Programming System (VPS) encoding

Five bytes of VPS information can be loaded via the I^2C-bus and will be encoded in the appropriate format into line 16.

7.12.4 Closed Caption encoder

Using this circuit, data in accordance with the specification of Closed Caption or extended data service, delivered by the control interface, can be encoded (line 21). Two dedicated pairs of bytes (two bytes per field), each pair preceded by run-in clocks and framing code, are possible.

The actual line number in which data is to be encoded, can be modified in a certain range.

The data clock frequency is in accordance with the definition for NTSC M standard 32 times horizontal line frequency.

Data LOW at the output of the DACs corresponds to 0 IRE, data HIGH at the output of the DACs corresponds to approximately 50 IRE.

It is also possible to encode Closed Caption data for 50 Hz field frequencies at 32 times the horizontal line frequency.

7.12.5 Anti-taping (SAA7104H only)

For more information contact your nearest Philips Semiconductors sales office.

7.13 RGB processor

This block contains a dematrix in order to produce RED, GREEN and BLUE signals to be fed to a SCART plug.

Before Y, C_B and C_R signals are de-matrixed, individual gain adjustment for Y and colour difference signals and 2 times oversampling for luminance and 4 times oversampling for colour difference signals is performed. The transfer curves of luminance and colour difference components of RGB are illustrated in Figs 8 and 9.

7.14 Triple DAC

Both Y and C signals are converted from digital-to-analog in a 10-bit resolution at the output of the video encoder. Y and C signals are also combined into a 10-bit CVBS signal.

The CVBS output signal occurs with the same processing delay as the Y, C and optional RGB or C_R-Y-C_B outputs. Absolute amplitude at the input of the DAC for CVBS is reduced by $^{15}/_{16}$ with respect to Y and C DACs to make maximum use of the conversion ranges.

RED, GREEN and BLUE signals are also converted from digital-to-analog, each providing a 10-bit resolution.

The reference currents of all three DACs can be adjusted individually in order to adapt for different output signals. In addition, all reference currents can be adjusted commonly to compensate for small tolerances of the on-chip band gap reference voltage.

Alternatively, all currents can be switched off to reduce power dissipation.

All three outputs can be used to sense for an external load (usually 75 Ω) during a pre-defined output. A flag in the I^2C-bus status byte reflects whether a load is applied or not. In addition, an automatic sense mode can be activated which indicates a 75 Ω load at any of the three outputs at the dedicated interrupt pin TVD.

If the SAA7104H; SAA7105H is required to drive a second (auxiliary) VGA monitor or an HDTV set, the DACs receive the signal coming from the HD data path. In this event, the DACs are clocked at the incoming PIXCLKI instead of the 27 MHz crystal clock used in the video encoder.

7.15 HD data path

This data path allows the SAA7104H; SAA7105H to be used with VGA or HDTV monitors. It receives its data directly from the cursor generator and supports RGB and Y-P_B-P_R output formats (RGB not with Y-P_B-P_R input formats). No scaling is done in this mode.

A gain adjustment either leads the full level swing to the digital-to-analog converters or reduces the amplitude by a factor of 0.69. This enables sync pulses to be added to the signal as it is required for display units expecting signals with sync pulses, either regular or 3-level syncs.

7.16 Timing generator

The synchronization of the SAA7104H; SAA7105H is able to operate in two modes; slave mode and master mode.

In slave mode, the circuit accepts sync pulses on the bidirectional FSVGC (frame sync), VSVGC (vertical sync) and HSVGC (horizontal sync) pins: the polarities of the signals can be programmed. The frame sync signal is only necessary when the input signal is interlaced, in other cases it may be omitted. If the frame sync signal is present, it is possible to derive the vertical and the horizontal phase from it by setting the HFS and VFS bits. HSVGC and VSVGC are not necessary in this case, so it is possible to switch the pins to output mode.

Alternatively, the device can be triggered by auxiliary codes in a ITU-R BT.656 data stream via PD7 to PD0.

Only vertical frequencies of 50 and 60 Hz are allowed with the SAA7104H; SAA7105H. In slave mode, it is not possible to lock the encoders colour carrier to the line frequency with the PHRES bits.

In the (more common) master mode, the time base of the circuit is continuously free-running. The IC can output a frame sync at pin FSVGC, a vertical sync at pin VSVGC, a horizontal sync at pin HSVGC and a composite blanking signal at pin $\overline{CBO}$. All of these signals are defined in the PIXCLK domain. The duration of HSVGC and VSVGC are fixed, they are 64 clocks for HSVGC and 1 line for VSVGC. The leading slopes are in phase and the polarities can be programmed.

The input line length can be programmed. The field length is always derived from the field length of the encoder and the pixel clock frequency that is being used.

$\overline{CBO}$ acts as a data request signal. The circuit accepts input data at a programmable number of clocks after $\overline{CBO}$ goes active. This signal is programmable and it is possible to adjust the following (see Figs 13 and 14):

- The horizontal offset
- The length of the active part of the line
- The distance from active start to first expected data
- The vertical offset separately for odd and even fields
- The number of lines per input field.

In most cases, the vertical offsets for odd and even fields are equal. If they are not, then the even field will start later. The SAA7104H; SAA7105H will also request the first input lines in the even field, the total number of requested lines will increase by the difference of the offsets.

As stated above, the circuit can be programmed to accept the look-up and cursor data in the first 2 lines of each field. The timing generator provides normal data request pulses for these lines; the duration is the same as for regular lines.

The additional request pulses will be suppressed with LUTL set to logic 0; see Table 108. The other vertical timings do not change in this case, so the first active line can be number 2, counted from 0.

7.17 Pattern generator for HD sync pulses

The pattern generator provides appropriate synchronization patterns for the video data path in auxiliary monitor or HDTV mode. It provides maximum flexibility in terms of raster generation for all interlaced and non-interlaced computer graphics or ATSC formats. The sync engine is capable of providing a combination of event-value pairs which can be used to insert certain values in the outgoing data stream at specified times. It can also be used to generate digital signals associated with time events. These can be used as digital horizontal and vertical synchronization signals on pins HSM_CSYNC and VSM.

The picture position is adjustable through the programmable relationship between the sync pulses and the video contents.

The generation of embedded analog sync pulses is bound to a number of events which can be defined for a line. Several of these line timing definitions can exist in parallel. For the final sync raster composition a certain sequence of lines with different sync event properties has to be defined. The sequence specifies a series of line types and the number of occurrences of this specific line type. Once the sequence has been completed, it restarts from the beginning. All pulse shapes are filtered internally in order to avoid ringing after analog post filters.

The sequence of the generated pulse stream must fit precisely to the incoming data stream in terms of the total number of pixels per line and lines per frame.

The sync engines flexibility is achieved by using a sequence of linked lists carrying the properties for the image, the lines as well as fractions of lines. Figure 3 illustrates the context between the various tables.

The first table serves as an array to hold the correct sequence of lines that compose the synchronization raster; it can contain up to 16 entries. Each entry holds a 4-bit index to the next table and a 10-bit counter value which specifies how often this particular line is invoked. If the necessary line count for a particular line exceeds the 10 bits, it has to use two table entries.

The 4-bit index in the line count array points to the line type array. It holds up to 15 entries (index 0 is not used), index 1 points to the first entry, index 2 to the second entry of the line type array etc.

Each entry of the line type array can hold up to 8 index pointers to another table. These indices point to portions of a line pulse pattern: A line could be split up e.g. into a sync, a blank, and an active portion followed by another blank portion, occupying four entries in one table line.

Each index of this table points to a particular line of the next table in the linked list. This table is called the line pattern array and each of the up to seven entries stores up to four pairs of a duration in pixel clock cycles and an index to a value table. The table entries are used to define portions of a line representing a certain value for a certain number of clock cycles.

The value specified in this table is actually another 3-bit index into a value array which can hold up to eight 8-bit values. If bit 4 (MSB) of the index is logic 1, the value is inserted into the G or Y signal, only; if bit 4 = 0, the associated value is inserted into all three signals.

Two additional bits of the entries in the value array (LSBs of the second byte) determine if the associated events appear as a digital pulse on the HSM_CSYNC and/or VSM outputs.

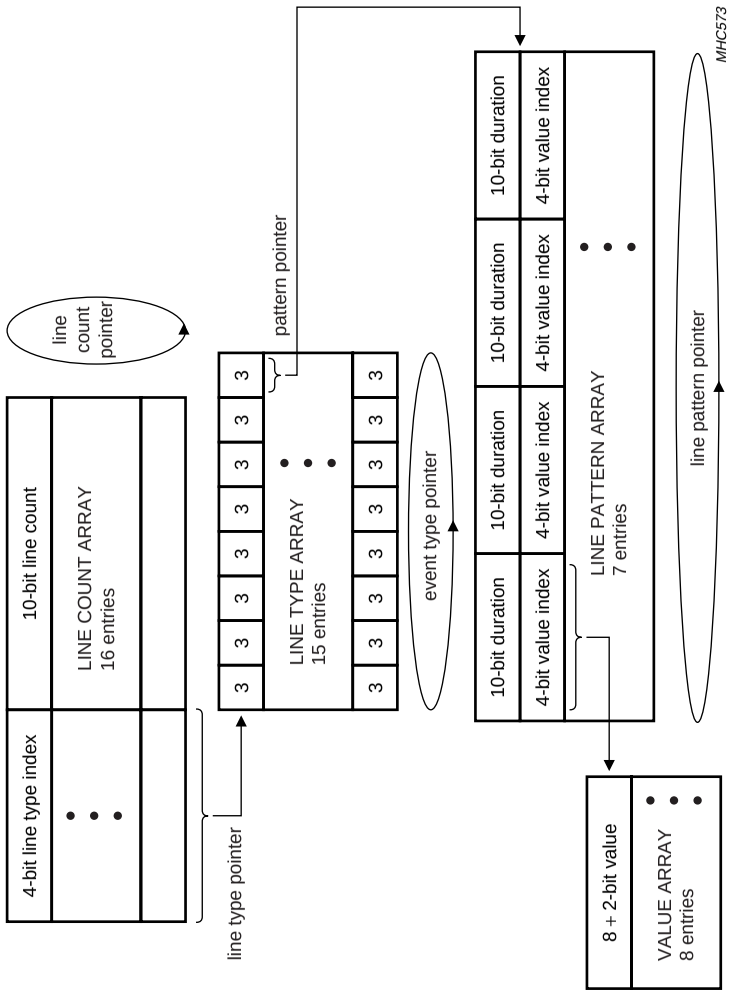


Fig.3 Context between the pattern generator tables for DH sync pulses.

To ease the trigger set-up for the sync generation module, a set of registers is provided to set up the screen raster which is defined as width and height. A trigger position can be specified as an x,y co-ordinate within the overall dimensions of the screen raster. If the x,y counter matches the specified co-ordinates, a trigger pulse is generated which pre-loads the tables with their initial values.

The listing in Table 5 outlines an example on how to set up the sync tables for a 1080i HD raster.

Important note:

Due to a problem in the programming interface, writing to the line pattern array (address D2) might destroy the data of the line type array (address D1). A work around is to write the line pattern array data before writing the line type array. Reading of the arrays is possible but all address pointers must be initialized before the next write operation.

Table 5 Example for set-up of the sync tables

SEQUENCE	COMMENT
Write to subaddress D0H	
00	points to first entry of line count array (index 0)
05 20	generate 5 lines of line type index 2 (this is the second entry of the line type array); will be the first vertical raster pulse
01 40	generate 1 line of line type index 4; will be sync-black-sync-black sequence after the first vertical pulse
0E 60	generate 14 lines of line type index 6; will be the following lines with sync-black sequence
1C 12	generate 540 lines of line type index 1; will be lines with sync and active video
02 60	generate 2 lines of line type index 6; will be the following lines with sync-black sequence
01 50	generate 1 line of line type index 5; will be the following line (line 563) with sync-black-sync-black-null sequence (null is equivalent to sync tip)
04 20	generate 4 lines of line type index 2; will be the second vertical raster pulse
01 30	generate 1 line of line type index 3; will be the following line with sync-null-sync-black sequence
0F 60	generate 15 lines of line type index 6; will be the following lines with sync-black sequence
1C 12	generate 540 lines of line type index 1; will be lines with sync and active video
02 60	generate 2 lines of line type index 6; will be the following lines with sync-black sequence; now, 1125 lines are defined
Write to subaddress D2H (insertion is done into all three analog output signals)	
00	points to first entry of line pattern array (index 1)
6F 33 2B 30 00 00 00 00	880 × value(3) + 44 × value(3); (subtract 1 from real duration)
6F 43 2B 30 00 00 00 00	880 × value(4) + 44 × value(3)
3B 30 BF 03 BF 03 2B 30	60 × value(3) + 960 × value(0) + 960 × value(0) + 44 × value(3)
2B 10 2B 20 57 30 00 00	44 × value(1) + 44 × value(2) + 88 × value(3)
3B 30 BF 33 BF 33 2B 30	60 × value(3) + 960 × value(3) + 960 × value(3) + 44 × value(3)
Write to subaddress D1H	
00	points to first entry of line type array (index 1)
34 00 00 00	use pattern entries 4 and 3 in this sequence (for sync and active video)
24 24 00 00	use pattern entries 4, 2, 4 and 2 in this sequence (for 2 × sync-black-null-black)
24 14 00 00	use pattern entries 4, 2, 4 and 1 in this sequence (for sync-black-null-black-null)
14 14 00 00	use pattern entries 4, 1, 4 and 1 in this sequence (for sync-black-sync-black)

SEQUENCE	COMMENT
14 24 00 00	use pattern entries 4, 1, 4 and 2 in this sequence (for sync-black-sync-black-null)
54 00 00 00	use pattern entries 4 and 5 in this sequence (for sync-black)
Write to subaddress D3H (no signals are directed to pins HSM_CSYNC and VSM)	
00	points to first entry of value array (index 0)
CC 00	black level, to be added during active video
80 00	sync level LOW (minimum output voltage)
0A 00	sync level HIGH (3-level sync)
CC 00	black level (needed elsewhere)
80 00	null (identical to sync level LOW)
Write to subaddress DCH	
0B	insertion is active, gain for signal is adapted accordingly

7.18 I²C-bus interface

The I²C-bus interface is a standard slave transceiver, supporting 7-bit slave addresses and 400 kbits/s guaranteed transfer rate. It uses 8-bit subaddressing with an auto-increment function. All registers are write and read, except two read only status bytes.

The register bit map consists of an RGB Look-Up Table (LUT), a cursor bit map and control registers. The LUT contains three banks of 256 bytes, where each RGB triplet is assigned to one address. Thus a write access needs the LUT address and three data bytes following subaddress FFH. For further write access auto-incrementing of the LUT address is performed. The cursor bit map access is similar to the LUT access but contains only a single byte per address.

The I²C-bus slave address is defined as 88H.

7.19 Power-down modes

In order to reduce the power consumption, the SAA7104H; SAA7105H supports 2 power-down modes, accessible via the I²C-bus. The analog power-down mode (DOWNA = 1) turns off the digital-to-analog converters and the pixel clock synthesizer. The digital power-down mode turns off all internal clocks and sets the digital outputs to LOW except the I²C-bus interface. The IC keeps its programming and can still be accessed in this mode, however not all registers can be read or written to. Reading or writing to the look-up tables, the cursor and the HD sync generator require a valid pixel clock. The typical supply current in full power-down is approximately 5 mA.

Because the analog power-down mode turns off the pixel clock synthesizer, there are limitations in some applications. If there is no pixel clock, the IC is not able to set its outputs to LOW. So, in most cases, DOWNA and DOWND should be set to logic 1 simultaneously. If the EIDIV bit is logic 1, it should be set to logic 0 before power-down.

7.20 Programming the SAA7104H; SAA7105H

The SAA7104H; SAA7105H needs to provide a continuous data stream at its analog outputs as well as receive a continuous stream of data from its data source. Because there is no frame memory isolating the data streams, restrictions apply to the input frame timings.

Input and output processing of the SAA7104H; SAA7105H are only coupled through the vertical frequencies. In master mode, the encoder provides a vertical sync and an odd/even pulse to the input processing. In slave mode, the encoder receives them.

The parameters of the input field are mainly given by the memory capacity of the SAA7104H; SAA7105H. The rule is that the scaler and thus the input processing needs to provide the video data in the same time frames as the encoder reads them. Therefore, the vertical active video times (and the vertical frequencies) need to be the same.

The second rule is that there has to be data in the buffer FIFO when the encoder enters the active video area. Therefore, the vertical offset in the input path needs to be a bit shorter than the offset of the encoder.

The following Sections give the set of equations required to program the IC for the most common application: A post processor in master mode with non-interlaced video input data.

Some variables are defined below:

- InPix: the number of active pixels per input line
- InPpl: the length of the entire input line in pixel clocks
- InLin: the number of active lines per input field/frame
- TPclk: the pixel clock period
- RiePclk: the ratio of internal to external pixel clock
- OutPix: the number of active pixels per output line
- OutLin: the number of active lines per output field
- TXclk: the encoder clock period (37.037 ns).

7.20.1 TV DISPLAY WINDOW

At 60 Hz, the first visible pixel has the index 256, 710 pixels can be encoded; at 50 Hz, the index is 284, 702 pixels can be visible.

The output lines should be centred on the screen. It should be noted that the encoder has 2 clocks per pixel; see Table 58.

ADWHS = 256 + 710 – OutPix (60 Hz);
ADWHS = 284 + 702 – OutPix (50 Hz);
ADWHE = ADWHS + OutPix × 2 (all frequencies)

For vertical, the procedure is the same. At 60 Hz, the first line with video information is number 19, 240 lines can be active. For 50 Hz, the numbers are 23 and 287; see Table 64.

$$FAL = 19 + \frac{240 - OutLin}{2} \text{ (60 Hz);}$$

$$FAL = 23 + \frac{287 - OutLin}{2} \text{ (50 Hz);}$$

LAL = FAL + OutLin (all frequencies)

Most TV sets use overscan, and not all pixels respectively lines are visible. There is no standard for the factor, it is highly recommended to make the number of output pixels and lines adjustable. A reasonable underscan factor is 10%, giving approximately 640 output pixels per line.

7.20.2 INPUT FRAME AND PIXEL CLOCK

The total number of pixel clocks per line and the input horizontal offset need to be chosen next. The only constraint is that the horizontal blanking has at least 10 clock pulses.

The required pixel clock frequency can be determined in the following way: Due to the limited internal FIFO size, the input path has to provide all pixels in the same time frame as the encoders vertical active time. The scaler also has to process the first and last border lines for the anti-flicker function. Thus:

$$TPclk = \frac{262.5 \times 1716 \times TXclk}{InPpl \times integer\left(\frac{InLin + 2}{OutLin} \times 262.5\right)} \text{ (60 Hz)}$$

$$TPclk = \frac{312.5 \times 1728 \times TXclk}{InPpl \times integer\left(\frac{InLin + 2}{OutLin} \times 312.5\right)} \text{ (50 Hz)}$$

and for the pixel clock generator

$$PCL = \frac{TXclk}{TPclk} \times 2^{20 + PCLE} \text{ (all frequencies);}$$

see Tables 67, 69 and 70. The divider PCLE should be set according to Table 69. PCLI may be set to a lower or the same value. Setting a lower value means that the internal pixel clock is higher and the data get sampled up. The difference may be 1 at 640 × 480 pixels resolution and 2 at resolutions with 320 pixels per line as a rule of thumb. This allows horizontal upscaling by a maximum factor of 2 respectively 4 (this is the parameter RiePclk).

$$PCLI = PCLE - \frac{\log RiePclk}{\log 2} \text{ (all frequencies)}$$

The equations ensure that the last line of the field has the full number of clock cycles. Many graphic controllers require this. Note that the bit PCLSY needs to be set to ensure that there is not even a fraction of a clock left at the end of the field.

7.20.3 HORIZONTAL SCALER

XOFS can be chosen arbitrarily, the condition being that XOFS + XPIX ≤ HLEN is fulfilled. Values given by the VESA display timings are preferred.

HLEN = InPpl × RiePclk – 1

$$XPIX = \frac{InPix}{2} \times RiePclk$$

$$XINC = \frac{OutPix}{InPix} \times \frac{4096}{RiePclk}$$

XINC needs to be rounded up, it needs to be set to 0 for a scaling factor of 1.

7.20.4 VERTICAL SCALER

The input vertical offset can be taken from the assumption that the scaler should just have finished writing the first line when the encoder starts reading it:

$$YOFS = \frac{FAL \times 1716 \times TXclk}{InPpl \times TPclk} - 2.5 \quad (60\ Hz)$$

$$YOFS = \frac{FAL \times 1728 \times TXclk}{InPpl \times TPclk} - 2.5 \quad (50\ Hz)$$

In most cases the vertical offsets will be the same for odd and even fields. The results should be rounded down.

YPIX = InLin

YSKIP defines the anti-flicker function. 0 means maximum flicker reduction but minimum vertical bandwidth, 4095 gives no flicker reduction and maximum bandwidth. Note that the maximum value for YINC is 4095. It might be necessary to reduce the value of YSKIP to fulfil this requirement.

$$YINC = \frac{OutLin}{InLin + 2} \times \left(1 + \frac{YSKIP}{4095}\right) \times 4096$$

$$YIWGTO = \frac{YINC}{2} + 2048$$

$$YIWGTE = \frac{YINC - YSKIP}{2}$$

When YINC = 0 it sets the scaler to scaling factor 1. The initial weighting factors must not be set to 0 in this case. YIWGTE may go negative. In this event, YINC should be added and YOFSE incremented. This can be repeated as often as necessary to make YIWGTE positive.

It should be noted that these equations assume that the input is non-interlaced but the output is interlaced. If the input is interlaced, the initial weighting factors need to be adapted to obtain the proper phase offsets in the output frame.

If vertical upscaling beyond the upper capabilities is required, the parameter YUPSC may be set to logic 1. This extends the maximum vertical scaling factor by a factor of 2. Only the parameter YINC is affected, it needs to be divided by two to get the same effect.

There are restrictions in this mode:

- The vertical filter YFILT is not available in this mode; the circuit will ignore this value
- The horizontal blanking needs to be long enough to transfer an output line between 2 memory locations. This is 710 internal pixel clocks.

  Or the upscaling factor needs to be limited to 1.5 and the horizontal upscaling factor is also limited to less than ~1.5. In this case a normal blanking length is sufficient.

7.21 Input levels and formats

The SAA7104H; SAA7105H accepts digital Y, C_B, C_R or RGB data with levels (digital codes) in accordance with *"ITU-R BT.601"*. An optional gain adjustment also allows to accept data with the full level swing of 0 to 255.

For C and CVBS outputs, deviating amplitudes of the colour difference signals can be compensated for by independent gain control setting, while gain for luminance is set to predefined values, distinguishable for 7.5 IRE set-up or without set-up.

The RGB, respectively C_R-Y-C_B path features an individual gain setting for luminance (GY) and colour difference signals (GCD). Reference levels are measured with a colour bar, 100% white, 100% amplitude and 100% saturation.

The SAA7104H; SAA7105H has special input cells for the VGC port. They operate at a wider supply voltage range and have a strict input threshold at $^1/_2V_{DDD}$. To achieve full speed of these cells, the EIDIV bit needs to be set to logic 1. Note that the impedance of these cells is approximately 6 kΩ. This may cause trouble with the bootstrapping pins of some graphic chips. So the power-on reset forces the bit to logic 0, the input impedance is regular in this mode.

Table 6 *"ITU-R BT.601"* signal component levels

COLOUR	SIGNALS(1)					
	Y	C_B	C_R	R	G	B
White	235	128	128	235	235	235
Yellow	210	16	146	235	235	16
Cyan	170	166	16	16	235	235
Green	145	54	34	16	235	16
Magenta	106	202	222	235	16	235
Red	81	90	240	235	16	16
Blue	41	240	110	16	16	235
Black	16	128	128	16	16	16

Note

1. Transformation:
   a) $R = Y + 1.3707 \times (C_R - 128)$
   b) $G = Y - 0.3365 \times (C_B - 128) - 0.6982 \times (C_R - 128)$
   c) $B = Y + 1.7324 \times (C_B - 128)$.

Table 7 Usage of bits SLOT and EDGE

DATA SLOT CONTROL (EXAMPLE FOR FORMAT 0)			
SLOT	**EDGE**	**1ST DATA**	**2ND DATA**
0	0	at rising edge G3/Y3	at falling edge R7/C_R7
0	**1**	**at falling edge G3/Y3**	**at rising edge R7/C_R7**
1	0	at rising edge R7/C_R7	at falling edge G3/Y3
1	1	at falling edge R7/C_R7	at rising edge G3/Y3

Table 8 Pin assignment for input format 0

8 + 8 + 8-BIT 4 : 4 : 4 NON-INTERLACED RGB/C_B-Y-C_R		
PIN	**FALLING CLOCK EDGE**	**RISING CLOCK EDGE**
PD11	G3/Y3	R7/C_R7
PD10	G2/Y2	R6/C_R6
PD9	G1/Y1	R5/C_R5
PD8	G0/Y0	R4/C_R4
PD7	B7/C_B7	R3/C_R3
PD6	B6/C_B6	R2/C_R2
PD5	B5/C_B5	R1/C_R1
PD4	B4/C_B4	R0/C_R0
PD3	B3/C_B3	G7/Y7
PD2	B2/C_B2	G6/Y6
PD1	B1/C_B1	G5/Y5
PD0	B0/C_B0	G4/Y4

Table 9 Pin assignment for input format 1

5 + 5 + 5-BIT 4 : 4 : 4 NON-INTERLACED RGB		
PIN	**FALLING CLOCK EDGE**	**RISING CLOCK EDGE**
PD7	G2	X
PD6	G1	R4
PD5	G0	R3
PD4	B4	R2
PD3	B3	R1
PD2	B2	R0
PD1	B1	G4
PD0	B0	G3

Table 10 Pin assignment for input format 2

5 + 6 + 5-BIT 4 : 4 : 4 NON-INTERLACED RGB		
PIN	**FALLING CLOCK EDGE**	**RISING CLOCK EDGE**
PD7	G2	R4
PD6	G1	R3
PD5	G0	R2
PD4	B4	R1
PD3	B3	R0
PD2	B2	G5
PD1	B1	G4
PD0	B0	G3

Table 11 Pin assignment for input format 3

8 + 8 + 8-BIT 4 : 2 : 2 NON-INTERLACED C_B-Y-C_R				
PIN	**FALLING CLOCK EDGE n**	**RISING CLOCK EDGE n**	**FALLING CLOCK EDGE n + 1**	**RISING CLOCK EDGE n + 1**
PD7	C_B7(0)	Y7(0)	C_R7(0)	Y7(1)
PD6	C_B6(0)	Y6(0)	C_R6(0)	Y6(1)
PD5	C_B5(0)	Y5(0)	C_R5(0)	Y5(1)
PD4	C_B4(0)	Y4(0)	C_R4(0)	Y4(1)
PD3	C_B3(0)	Y3(0)	C_R3(0)	Y3(1)
PD2	C_B2(0)	Y2(0)	C_R2(0)	Y2(1)
PD1	C_B1(0)	Y1(0)	C_R1(0)	Y1(1)
PD0	C_B0(0)	Y0(0)	C_R0(0)	Y0(1)

Table 12 Pin assignment for input format 4

8 + 8 + 8-BIT 4 : 2 : 2 INTERLACED C_B-Y-C_R (ITU-R BT.656, 27 MHz CLOCK)				
PIN	**RISING CLOCK EDGE n**	**RISING CLOCK EDGE n + 1**	**RISING CLOCK EDGE n + 2**	**RISING CLOCK EDGE n + 3**
PD7	C_B7(0)	Y7(0)	C_R7(0)	Y7(1)
PD6	C_B6(0)	Y6(0)	C_R6(0)	Y6(1)
PD5	C_B5(0)	Y5(0)	C_R5(0)	Y5(1)
PD4	C_B4(0)	Y4(0)	C_R4(0)	Y4(1)
PD3	C_B3(0)	Y3(0)	C_R3(0)	Y3(1)
PD2	C_B2(0)	Y2(0)	C_R2(0)	Y2(1)
PD1	C_B1(0)	Y1(0)	C_R1(0)	Y1(1)
PD0	C_B0(0)	Y0(0)	C_R0(0)	Y0(1)

Table 13 Pin assignment for input format 5; note 1

8-BIT NON-INTERLACED INDEX COLOUR		
PIN	**FALLING CLOCK EDGE**	**RISING CLOCK EDGE**
PD11	X	X
PD10	X	X
PD9	X	X
PD8	X	X
PD7	INDEX7	X
PD6	INDEX6	X
PD5	INDEX5	X
PD4	INDEX4	X
PD3	INDEX3	X
PD2	INDEX2	X
PD1	INDEX1	X
PD0	INDEX0	X

Note

1. X = don’t care.

Table 14 Pin assignment for input format 6

8 + 8 + 8-BIT 4 : 4 : 4 NON-INTERLACED RGB/C_B-Y-C_R		
PIN	**FALLING CLOCK EDGE**	**RISING CLOCK EDGE**
PD11	G4/Y4	R7/C_R7
PD10	G3/Y3	R6/C_R6
PD9	G2/Y2	R5/C_R5
PD8	B7/C_B7	R4/C_R4
PD7	B6/C_B6	R3/C_R3
PD6	B5/C_B5	G7/Y7
PD5	B4/C_B4	G6/Y6
PD4	B3/C_B3	G5/Y5
PD3	G0/Y0	R2/C_R2
PD2	B2/C_B2	R1/C_R1
PD1	B1/C_B1	R0/C_R0
PD0	B0/C_B0	G1/Y1

7.22 Bit allocation map

Table 15 Slave receiver (slave address 88H)

REGISTER FUNCTION	SUB ADDR. (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
Status byte (read only)	00	VER2	VER1	VER0	CCRDO	CCRDE	(1)	FSEQ	O_E
Null	01 to 15	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Common DAC adjust fine	16	(1)	(1)	(1)	(1)	DACF3	DACF2	DACF1	DACF0
R DAC adjust coarse	17	(1)	(1)	(1)	RDACC4	RDACC3	RDACC2	RDACC1	RDACC0
G DAC adjust coarse	18	(1)	(1)	(1)	GDACC4	GDACC3	GDACC2	GDACC1	GDACC0
B DAC adjust coarse	19	(1)	(1)	(1)	BDACC4	BDACC3	BDACC2	BDACC1	BDACC0
MSM threshold	1A	MSMT7	MSMT6	MSMT5	MSMT4	MSMT3	MSMT2	MSMT1	MSMT0
Monitor sense mode	1B	MSM	MSA	MSOE	(1)	(1)	RCOMP	GCOMP	BCOMP
Chip ID (02B or 03B, read only)	1C	CID7	CID6	CID5	CID4	CID3	CID2	CID1	CID0
Wide screen signal	26	WSS7	WSS6	WSS5	WSS4	WSS3	WSS2	WSS1	WSS0
Wide screen signal	27	WSSON	(1)	WSS13	WSS12	WSS11	WSS10	WSS9	WSS8
Real-time control, burst start	28	(1)	(1)	BS5	BS4	BS3	BS2	BS1	BS0
Sync reset enable, burst end	29	SRES	(1)	BE5	BE4	BE3	BE2	BE1	BE0
Copy generation 0	2A	CG07	CG06	CG05	CG04	CG03	CG02	CG01	CG00
Copy generation 1	2B	CG15	CG14	CG13	CG12	CG11	CG10	CG09	CG08
CG enable, copy generation 2	2C	CGEN	(1)	(1)	(1)	CG19	CG18	CG17	CG16
Output port control	2D	VBSEN	CVBSEN1	CVBSEN0	CEN	ENCOFF	CLK2EN	CVBSEN2	(1)
Null	2E to 36	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Input path control	37	(1)	YUPSC	YFIL1	YFIL0	(1)	CZOOM	IGAIN	XINT
Gain luminance for RGB	38	(1)	(1)	(1)	GY4	GY3	GY2	GY1	GY0
Gain colour difference for RGB	39	(1)	(1)	(1)	GCD4	GCD3	GCD2	GCD1	GCD0
Input port control 1	3A	CBENB	(1)	SYNTV	SYMP	DEMOFF	CSYNC	Y2C	UV2C
VPS enable, input control 2	54	VPSEN	(1)	GPVAL	GPEN	(1)	(1)	EDGE	SLOT
VPS byte 5	55	VPS57	VPS56	VPS55	VPS54	VPS53	VPS52	VPS51	VPS50
VPS byte 11	56	VPS117	VPS116	VPS115	VPS114	VPS113	VPS112	VPS111	VPS110
VPS byte 12	57	VPS127	VPS126	VPS125	VPS124	VPS123	VPS122	VPS121	VPS120
VPS byte 13	58	VPS137	VPS136	VPS135	VPS134	VPS133	VPS132	VPS131	VPS130
VPS byte 14	59	VPS147	VPS146	VPS145	VPS144	VPS143	VPS142	VPS141	VPS140
Chrominance phase	5A	CHPS7	CHPS6	CHPS5	CHPS4	CHPS3	CHPS2	CHPS1	CHPS0

REGISTER FUNCTION	SUB ADDR. (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
Gain U	5B	GAINU7	GAINU6	GAINU5	GAINU4	GAINU3	GAINU2	GAINU1	GAINU0
Gain V	5C	GAINV7	GAINV6	GAINV5	GAINV4	GAINV3	GAINV2	GAINV1	GAINV0
Gain U MSB, black level	5D	GAINU8	(1)	BLCKL5	BLCKL4	BLCKL3	BLCKL2	BLCKL1	BLCKL0
Gain V MSB, blanking level	5E	GAINV8	(1)	BLNNL5	BLNNL4	BLNNL3	BLNNL2	BLNNL1	BLNNL0
CCR, blanking level VBI	5F	CCRS1	CCRS0	BLNVB5	BLNVB4	BLNVB3	BLNVB2	BLNVB1	BLNVB0
Null	60	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Standard control	61	DOWND	DOWNA	INPI	YGS	(1)	SCBW	PAL	FISE
Burst amplitude	62	RTCE	BSTA6	BSTA5	BSTA4	BSTA3	BSTA2	BSTA1	BSTA0
Subcarrier 0	63	FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00
Subcarrier 1	64	FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08
Subcarrier 2	65	FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16
Subcarrier 3	66	FSC31	FSC30	FSC29	FSC28	FSC27	FSC26	FSC25	FSC24
Line 21 odd 0	67	L21O07	L21O06	L21O05	L21O04	L21O03	L21O02	L21O01	L21O00
Line 21 odd 1	68	L21O17	L21O16	L21O15	L21O14	L21O13	L21O12	L21O11	L21O10
Line 21 even 0	69	L21E07	L21E06	L21E05	L21E04	L21E03	L21E02	L21E01	L21E00
Line 21 even 1	6A	L21E17	L21E16	L21E15	L21E14	L21E13	L21E12	L21E11	L21E10
Null	6B	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Trigger control	6C	HTRIG7	HTRIG6	HTRIG5	HTRIG4	HTRIG3	HTRIG2	HTRIG1	HTRIG0
Trigger control	6D	HTRIG10	HTRIG9	HTRIG8	VTRIG4	VTRIG3	VTRIG2	VTRIG1	VTRIG0
Multi control	6E	NVTRIG	BLCKON	PHRES1	PHRES0	LDEL1	LDEL0	FLC1	FLC0
Closed Caption, teletext enable	6F	CCEN1	CCEN0	TTXEN	SCCLN4	SCCLN3	SCCLN2	SCCLN1	SCCLN0
Active display window horizontal start	70	ADWHS7	ADWHS6	ADWHS5	ADWHS4	ADWHS3	ADWHS2	ADWHS1	ADWHS0
Active display window horizontal end	71	ADWHE7	ADWHE6	ADWHE5	ADWHE4	ADWHE3	ADWHE2	ADWHE1	ADWHE0
MSBs ADWH	72	(1)	ADWHE10	ADWHE9	ADWHE8	(1)	ADWHS10	ADWHS9	ADWHS8
TTX request horizontal start	73	TTXHS7	TTXHS6	TTXHS5	TTXHS4	TTXHS3	TTXHS2	TTXHS1	TTXHS0
TTX request horizontal delay	74	(1)	(1)	(1)	(1)	TTXHD3	TTXHD2	TTXHD1	TTXHD0
CSYNC advance	75	CSYNCA4	CSYNCA3	CSYNCA2	CSYNCA1	CSYNCA0	(1)	(1)	(1)
TTX odd request vertical start	76	TTXOVS7	TTXOVS6	TTXOVS5	TTXOVS4	TTXOVS3	TTXOVS2	TTXOVS1	TTXOVS0
TTX odd request vertical end	77	TTXOVE7	TTXOVE6	TTXOVE5	TTXOVE4	TTXOVE3	TTXOVE2	TTXOVE1	TTXOVE0
TTX even request vertical start	78	TTXEVS7	TTXEVS6	TTXEVS5	TTXEVS4	TTXEVS3	TTXEVS2	TTXEVS1	TTXEVS0

REGISTER FUNCTION	SUB ADDR. (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
TTX even request vertical end	79	TTXEVE7	TTXEVE6	TTXEVE5	TTXEVE4	TTXEVE3	TTXEVE2	TTXEVE1	TTXEVE0
First active line	7A	FAL7	FAL6	FAL5	FAL4	FAL3	FAL2	FAL1	FAL0
Last active line	7B	LAL7	LAL6	LAL5	LAL4	LAL3	LAL2	LAL1	LAL0
TTX mode, MSB vertical	7C	TTX60	LAL8	TTXO	FAL8	TTXEVE8	TTXOVE8	TTXEVS8	TTXOVS8
Null	7D	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Disable TTX line	7E	LINE12	LINE11	LINE10	LINE9	LINE8	LINE7	LINE6	LINE5
Disable TTX line	7F	LINE20	LINE19	LINE18	LINE17	LINE16	LINE15	LINE14	LINE13
FIFO status (read only)	80	(1)	(1)	(1)	(1)	IFERR	BFERR	OVFL	UDFL
Pixel clock 0	81	PCL07	PCL06	PCL05	PCL04	PCL03	PCL02	PCL01	PCL00
Pixel clock 1	82	PCL15	PCL14	PCL13	PCL12	PCL11	PCL10	PCL09	PCL08
Pixel clock 2	83	PCL23	PCL22	PCL21	PCL20	PCL19	PCL18	PCL17	PCL16
Pixel clock control	84	DCLK	PCLSY	IFRA	IFBP	PCLE1	PCLE0	PCLI1	PCLI0
FIFO control	85	EIDIV	(1)	(1)	(1)	FILI3	FILI2	FILI1	FILI0
Null	86 to 8F	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)
Horizontal offset	90	XOFS7	XOFS6	XOFS5	XOFS4	XOFS3	XOFS2	XOFS1	XOFS0
Pixel number	91	XPIX7	XPIX6	XPIX5	XPIX4	XPIX3	XPIX2	XPIX1	XPIX0
Vertical offset odd	92	YOFSO7	YOFSO6	YOFSO5	YOFSO4	YOFSO3	YOFSO2	YOFSO1	YOFSO0
Vertical offset even	93	YOFSE7	YOFSE6	YOFSE5	YOFSE4	YOFSE3	YOFSE2	YOFSE1	YOFSE0
MSBs	94	YOFSE9	YOFSE8	YOFSO9	YOFSO8	XPIX9	XPIX8	XOFS9	XOFS8
Line number	95	YPIX7	YPIX6	YPIX5	YPIX4	YPIX3	YPIX2	YPIX1	YPIX0
Scaler CTRL, MCB YPIX	96	EFS	PCBN	SLAVE	ILC	YFIL	(1)	YPIX9	YPIX8
Sync control	97	HFS	VFS	OFS	PFS	OVS	PVS	OHS	PHS
Line length	98	HLEN7	HLEN6	HLEN5	HLEN4	HLEN3	HLEN2	HLEN1	HLEN0
Input delay, MSB line length	99	IDEL3	IDEL2	IDEL1	IDEL0	HLEN11	HLEN10	HLEN9	HLEN8
Horizontal increment	9A	XINC7	XINC6	XINC5	XINC4	XINC3	XINC2	XINC1	XINC0
Vertical increment	9B	YINC7	YINC6	YINC5	YINC4	YINC3	YINC2	YINC1	YINC0
MSBs vertical and horizontal increment	9C	YINC11	YINC10	YINC9	YINC8	XINC11	XINC10	XINC9	XINC8
Weighting factor odd	9D	YIWGTO7	YIWGTO6	YIWGTO5	YIWGTO4	YIWGTO3	YIWGTO2	YIWGTO1	YIWGTO0
Weighting factor even	9E	YIWGTE7	YIWGTE6	YIWGTE5	YIWGTE4	YIWGTE3	YIWGTE2	YIWGTE1	YIWGTE0
Weighting factor MSB	9F	YIWGTE11	YIWGTE10	YIWGTE9	YIWGTE8	YIWGTO11	YIWGTO10	YIWGTO9	YIWGTO8
Vertical line skip	A0	YSKIP7	YSKIP6	YSKIP5	YSKIP4	YSKIP3	YSKIP2	YSKIP1	YSKIP0

REGISTER FUNCTION	SUB ADDR. (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
Blank enable for NI-bypass, vertical line skip MSB	A1	BLEN	(1)	(1)	(1)	YSKIP11	YSKIP10	YSKIP9	YSKIP8
Border colour Y	A2	BCY7	BCY6	BCY5	BCY4	BCY3	BCY2	BCY1	BCY0
Border colour U	A3	BCU7	BCU6	BCU5	BCU4	BCU3	BCU2	BCU1	BCU0
Border colour V	A4	BCV7	BCV6	BCV5	BCV4	BCV3	BCV2	BCV1	BCV0
HD sync line count array	D0	RAM address (see Table 88)							
HD sync line type array	D1	RAM address (see Table 90)							
HD sync line pattern array	D2	RAM address (see Table 92)							
HD sync value array	D3	RAM address (see Table 94)							
HD sync trigger state 1	D4	HLCT7	HLCT6	HLCT5	HLCT4	HLCT3	HLCT2	HLCT1	HLCT0
HD sync trigger state 2	D5	HLCPT3	HLCPT2	HLCPT1	HLCPT0	HLPPT1	HLPPT0	HLCT9	HLCT8
HD sync trigger state 3	D6	HDCT7	HDCT6	HDCT5	HDCT4	HDCT3	HDCT2	HDCT1	HDCT0
HD sync trigger state 4	D7	(1)	HEPT2	HEPT1	HEPT0	(1)	(1)	HDCT9	HDCT8
HD sync trigger phase x	D8	HTX7	HTX6	HTX5	HTX4	HTX3	HTX2	HTX1	HTX0
	D9	(1)	(1)	(1)	(1)	HTX11	HTX10	HTX9	HTX8
HD sync trigger phase y	DA	HTY7	HTY6	HTY5	HTY4	HTY3	HTY2	HTY1	HTY0
	DB	(1)	(1)	(1)	(1)	(1)	(1)	HTY9	HTY8
HD output control	DC	(1)	(1)	(1)	(1)	HDSYE	HDTC	HDGY	HDIP
Cursor colour 1 R	F0	CC1R7	CC1R6	CC1R5	CC1R4	CC1R3	CC1R2	CC1R1	CC1R0
Cursor colour 1 G	F1	CC1G7	CC1G6	CC1G5	CC1G4	CC1G3	CC1G2	CC1G1	CC1G0
Cursor colour 1 B	F2	CC1B7	CC1B6	CC1B5	CC1B4	CC1B3	CC1B2	CC1B1	CC1B0
Cursor colour 2 R	F3	CC2R7	CC2R6	CC2R5	CC2R4	CC2R3	CC2R2	CC2R1	CC2R0
Cursor colour 2 G	F4	CC2G7	CC2G6	CC2G5	CC2G4	CC2G3	CC2G2	CC2G1	CC2G0
Cursor colour 2 B	F5	CC2B7	CC2B6	CC2B5	CC2B4	CC2B3	CC2B2	CC2B1	CC2B0
Auxiliary cursor colour R	F6	AUXR7	AUXR6	AUXR5	AUXR4	AUXR3	AUXR2	AUXR1	AUXR0
Auxiliary cursor colour G	F7	AUXG7	AUXG6	AUXG5	AUXG4	AUXG3	AUXG2	AUXG1	AUXG0
Auxiliary cursor colour B	F8	AUXB7	AUXB6	AUXB5	AUXB4	AUXB3	AUXB2	AUXB1	AUXB0
Horizontal cursor position	F9	XCP7	XCP6	XCP5	XCP4	XCP3	XCP2	XCP1	XCP0
Horizontal hot spot, MSB XCP	FA	XHS4	XHS3	XHS2	XHS1	XHS0	XCP10	XCP9	XCP8
Vertical cursor position	FB	YCP7	YCP6	YCP5	YCP4	YCP3	YCP2	YCP1	YCP0
Vertical hot spot, MSB YCP	FC	YHS4	YHS3	YHS2	YHS1	YHS0	(1)	YCP9	YCP8

REGISTER FUNCTION	SUB ADDR. (HEX)	D7	D6	D5	D4	D3	D2	D1	D0
Input path control	FD	LUTOFF	CMODE	LUTL	IF2	IF1	IF0	MATOFF	DFOFF
Cursor bit map	FE	RAM address (see Table 109)							
Colour look-up table	FF	RAM address (see Table 110)							

Note

1. All unused control bits must be programmed with logic 0 to ensure compatibility to future enhancements.

7.23 I²C-bus format

Table 16 I²C-bus write access to control registers; see Table 22

S	1 0 0 0 1 0 0 0	A	SUBADDRESS	A	DATA 0	A	--------	DATA n	A	P

Table 17 I²C-bus write access to the HD line count array (subaddress D0H); see Table 22

S	1 0 0 0 1 0 0 0	A	D0H	A	RAM ADDRESS	A	DATA 00	A	DATA 01	A	--------	DATA n	A	P

Table 18 I²C-bus write access to cursor bit map (subaddress FEH); see Table 22

S	1 0 0 0 1 0 0 0	A	FEH	A	RAM ADDRESS	A	DATA 0	A	--------	DATA n	A	P

Table 19 I²C-bus write access to colour look-up table (subaddress FFH); see Table 22

S	1 0 0 0 1 0 0 0	A	FFH	A	RAM ADDRESS	A	DATA 0R	A	DATA 0G	A	DATA 0B	A	--------	P

Table 20 I²C-bus read access to control registers; see Table 22

S	1 0 0 0 1 0 0 0	A	SUBADDRESS	A	Sr	1 0 0 0 1 0 0 1	A	DATA 0	Am	--------	DATA n	Am	P

Table 21 I²C-bus read access to cursor bit map or colour LUT; see Table 22

S	1 0 0 0 1 0 0 0	A	FEH or FFH	A	RAM ADDRESS	A	Sr	1 0 0 0 1 0 0 1	A	DATA 0	Am	--------	DATA n	Am	P

Table 22 Explanations of Tables 16 to 21

CODE	DESCRIPTION
S	START condition
Sr	repeated START condition
1 0 0 0 1 0 0 X; note 1	slave address
A	acknowledge generated by the slave
Am	acknowledge generated by the master
SUBADDRESS; note 2	subaddress byte
DATA	data byte
--------	continued data bytes and acknowledges
P	STOP condition
RAM ADDRESS	start address for RAM access

Notes

1. X is the read/write control bit; X = logic 0 is order to write; X = logic 1 is order to read.
2. If more than 1 byte of DATA is transmitted, then auto-increment of the subaddress is performed.

7.24 Slave receiver

Table 23 Subaddress 16H

DATA BYTE	DESCRIPTION
DACF	output level adjustment fine in 1% steps for all DACs; default after reset is 00H; see Table 24

Table 24 Fine adjustment of DAC output voltage

BINARY	GAIN (%)
0111	7
0110	6
0101	5
0100	4
0011	3
0010	2
0001	1
0000	0
1000	0
1001	−1
1010	−2
1011	−3
1100	−4
1101	−5
1110	−6
1111	−7

Table 25 Subaddresses 17H to 19H

DATA BYTE	DESCRIPTION
RDACC	output level coarse adjustment for RED DAC; default after reset is 1BH for output of C signal 00000b ≡ 0.585 V to 11111b ≡ 1.240 V at 37.5 Ω nominal for full-scale conversion
GDACC	output level coarse adjustment for GREEN DAC; default after reset is 1BH for output of VBS signal 00000b ≡ 0.585 V to 11111b ≡ 1.240 V at 37.5 Ω nominal for full-scale conversion
BDACC	output level coarse adjustment for BLUE DAC; default after reset is 1FH for output of CVBS signal 00000b ≡ 0.585 V to 11111b ≡ 1.240 V at 37.5 Ω nominal for full-scale conversion

Table 26 Subaddress 1AH

DATA BYTE	DESCRIPTION
MSMT	monitor sense mode threshold for DAC output voltage, should be set to 70

Table 27 Subaddress 1BH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
MSM	0	monitor sense mode off; RCOMP, GCOMP and BCOMP bits are not valid; default after reset
	1	monitor sense mode on
MSA	0	automatic monitor sense mode off; RCOMP, GCOMP and BCOMP bits are not valid; default after reset
	1	automatic monitor sense mode on if MSM = 0
MSOE	0	pin TVD is active
	1	pin TVD is 3-state; default after reset
RCOMP (read only)	0	check comparator at DAC on pin RED_CR_C_CVBS is active, output is loaded
	1	check comparator at DAC on pin RED_CR_C_CVBS is inactive, output is not loaded
GCOMP (read only)	0	check comparator at DAC on pin GREEN_VBS_CVBS is active, output is loaded
	1	check comparator at DAC on pin GREEN_VBS_CVBS is inactive, output is not loaded
BCOMP (read only)	0	check comparator at DAC on pin BLUE_CB_CVBS is active, output is loaded
	1	check comparator at DAC on pin BLUE_CB_CVBS is inactive, output is not loaded

Table 28 Subaddresses 26H and 27H

DATA BYTE	LOGIC LEVEL	DESCRIPTION
WSS	–	wide screen signalling bits 3 to 0 = aspect ratio 7 to 4 = enhanced services 10 to 8 = subtitles 13 to 11 = reserved
WSSON	0	wide screen signalling output is disabled; default after reset
	1	wide screen signalling output is enabled

Table 29 Subaddress 28H

DATA BYTE	LOGIC LEVEL	DESCRIPTION	REMARKS
BS	–	starting point of burst in clock cycles	PAL: BS = 33 (21H); default after reset if strapping pin FSVGC tied to HIGH
			NTSC: BS = 25 (19H); default after reset if strapping pin FSVGC tied to LOW

Table 30 Subaddress 29H

DATA BYTE	LOGIC LEVEL	DESCRIPTION	REMARKS
SRES	0	pin TTX_SRES accepts a teletext bit stream (TTX)	default after reset
	1	pin TTX_SRES accepts a sync reset input (SRES)	a HIGH impulse resets synchronization of the encoder (first field, first line)
BE	–	ending point of burst in clock cycles	PAL: BE = 29 (1DH); default after reset if strapping pin FSVGC tied to HIGH
			NTSC: BE = 29 (1DH); default after reset if strapping pin FSVGC tied to LOW

Table 31 Subaddresses 2AH to 2CH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
CG	–	LSBs of the respective bytes are encoded immediately after run-in, the MSBs of the respective bytes have to carry the CRCC bits, in accordance with the definition of copy generation management system encoding format.
CGEN	0	copy generation data output is disabled; default after reset
	1	copy generation data output is enabled

Table 32 Subaddress 2DH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
VBSEN	0	pin GREEN_VBS_CVBS provides a component GREEN signal (CVBSEN1 = 0) or CVBS signal (CVBSEN1 = 1)
	1	pin GREEN_VBS_CVBS provides a luminance (VBS) signal; default after reset
CVBSEN1	0	pin GREEN_VBS_CVBS provides a component GREEN (G) or luminance (VBS) signal; default after reset
	1	pin GREEN_VBS_CVBS provides a CVBS signal
CVBSEN0	0	pin BLUE_CB_CVBS provides a component BLUE (B) or colour difference BLUE (C_B) signal
	1	pin BLUE_CB_CVBS provides a CVBS signal; default after reset
CEN	0	pin RED_CR_C_CVBS provides a component RED (R) or colour difference RED (C_R) signal
	1	pin RED_CR_C_CVBS provides a chrominance signal (C) as modulated subcarrier for S-video; default after reset
ENCOFF	0	encoder is active; default after reset
	1	encoder bypass, DACs are provided with RGB signal after cursor insertion block
CLK2EN	0	pin TTXRQ_XCLKO2 provides a teletext request signal (TTXRQ)
	1	pin TTXRQ_XCLKO2 provides the buffered crystal clock divided by two (13.5 MHz); default after reset
CVBSEN2	0	pin RED_CR_C_CVBS provides a signal according to CEN; default after reset
	1	pin RED_CR_C_CVBS provides a CVBS signal

Table 33 Subaddress 37H

DATA BYTE	LOGIC LEVEL	DESCRIPTION
YUPSC	0	normal operation of the vertical scaler; default after reset
	1	vertical upscaling is enabled
YFIL	–	controls the vertical interpolation filter, see Table 34; the filter is not available if YUPSC = 1
CZOOM	0	normal operation of the cursor generator; default after reset
	1	the cursor will be zoomed by a factor of 2 in both directions
IGAIN	0	expected input level swing is 16 to 235 (8-bit RGB); default after reset
	1	expected input level swing is 0 to 255 (8-bit RGB)
XINT	0	no horizontal interpolation filter; default after reset
	1	interpolation filter for horizontal upscaling is active

Table 34 Logic levels and function of YFIL

DATA BYTE		DESCRIPTION
YFIL1	YFIL0	
0	0	no filter active; default after reset
0	1	filter is inserted before vertical scaling
1	0	filter is inserted after vertical scaling; YSKIP should be logic 0
1	1	reserved

Table 35 Subaddresses 38H and 39H

DATA BYTE	DESCRIPTION
GY4 to GY0	Gain luminance of RGB (C_R, Y and C_B) output, ranging from ($1 - {}^{16}\!/_{32}$) to ($1 + {}^{15}\!/_{32}$). Suggested nominal value = 0, depending on external application.
GCD4 to GCD0	Gain colour difference of RGB (C_R, Y and C_B) output, ranging from ($1 - {}^{16}\!/_{32}$) to ($1 + {}^{15}\!/_{32}$). Suggested nominal value = 0, depending on external application.

Table 36 Subaddress 3AH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
CBENB	0	data from input ports is encoded
	1	colour bar with fixed colours is encoded
SYNTV	0	in slave mode, the encoder is only synchronized at the beginning of an odd field; default after reset
	1	in slave mode, the encoder receives a vertical sync signal
SYMP	0	horizontal and vertical trigger is taken from FSVGC or both VSVGC and HSVGC; default after reset
	1	horizontal and vertical trigger is decoded out of *"ITU-R BT.656"* compatible data at PD port
DEMOFF	0	Y-C_B-C_R to RGB dematrix is active; default after reset
	1	Y-C_B-C_R to RGB dematrix is bypassed
CSYNC	0	pin HSM_CSYNC provides a horizontal sync for non-interlaced VGA components output (at PIXCLK)
	1	pin HSM_CSYNC provides a composite sync for interlaced components output (at XTAL clock)
Y2C	0	input luminance data is twos complement from PD input port
	1	input luminance data is straight binary from PD input port; default after reset
UV2C	0	input colour difference data is twos complement from PD input port
	1	input colour difference data is straight binary from PD input port; default after reset

Table 37 Subaddress 54H

DATA BYTE	LOGIC LEVEL	DESCRIPTION
VPSEN	0	video programming system data insertion is disabled; default after reset
	1	video programming system data insertion in line 16 is enabled
GPVAL	0	pin VSM provides a LOW level if GPEN = 1
	1	pin VSM provides a HIGH level if GPEN = 1
GPEN	0	pin VSM provides a vertical sync for a monitor; default after reset
	1	pin VSM provides a constant signal according to GPVAL
EDGE	0	input data is sampled with inverse clock edges
	1	input data is sampled with the clock edges specified in Tables 8 to 13; default after reset
SLOT	0	normal assignment of the input data to the clock edge; default after reset
	1	correct time misalignment due to inverted assignment of input data to the clock edge

Table 38 Subaddresses 55H to 59H

DATA BYTE	DESCRIPTION	REMARKS
VPS5	fifth byte of video programming system data	in line 16; LSB first; all other bytes are not relevant for VPS
VPS11	eleventh byte of video programming system data	
VPS12	twelfth byte of video programming system data	
VPS13	thirteenth byte of video programming system data	
VPS14	fourteenth byte of video programming system data	

Table 39 Subaddress 5AH; note 1

DATA BYTE	DESCRIPTION	VALUE	RESULT
CHPS	phase of encoded colour subcarrier (including burst) relative to horizontal sync; can be adjusted in steps of 360/256 degrees	6BH	PAL B/G and data from input ports in master mode
		16H	PAL B/G and data from look-up table
		25H	NTSC M and data from input ports in master mode
		46H	NTSC M and data from look-up table

Note

1. The default after reset is 00H.

Table 40 Subaddresses 5BH and 5DH

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINU	variable gain for C_B signal; input representation in accordance with *"ITU-R BT.601"*	white-to-black = 92.5 IRE	GAINU = −2.17 × nominal to +2.16 × nominal
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 118 (76H)	output subcarrier of U contribution = nominal
		white-to-black = 100 IRE	GAINU = −2.05 × nominal to +2.04 × nominal
		GAINU = 0	output subcarrier of U contribution = 0
		GAINU = 125 (7DH)	output subcarrier of U contribution = nominal

Table 41 Subaddresses 5CH and 5EH

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
GAINV	variable gain for C_R signal; input representation in accordance with *"ITU-R BT.601"*	white-to-black = 92.5 IRE	GAINV = −1.55 × nominal to +1.55 × nominal
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 165 (A5H)	output subcarrier of V contribution = nominal
		white-to-black = 100 IRE	GAINV = −1.46 × nominal to +1.46 × nominal
		GAINV = 0	output subcarrier of V contribution = 0
		GAINV = 175 (AFH)	output subcarrier of V contribution = nominal

Table 42 Subaddress 5DH

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLCKL	variable black level; input representation in accordance with *"ITU-R BT.601"*	white-to-sync = 140 IRE; note 1	recommended value: BLCKL = 58 (3AH)
		BLCKL = 0; note 1	output black level = 29 IRE
		BLCKL = 63 (3FH); note 1	output black level = 49 IRE
		white-to-sync = 143 IRE; note 2	recommended value: BLCKL = 51 (33H)
		BLCKL = 0; note 2	output black level = 27 IRE
		BLCKL = 63 (3FH); note 2	output black level = 47 IRE

Notes

1. Output black level/IRE = BLCKL × 2/6.29 + 28.9.
2. Output black level/IRE = BLCKL × 2/6.18 + 26.5.

Table 43 Subaddress 5EH

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
BLNNL	variable blanking level	white-to-sync = 140 IRE; note 1	recommended value: BLNNL = 46 (2EH)
		BLNNL = 0; note 1	output blanking level = 25 IRE
		BLNNL = 63 (3FH); note 1	output blanking level = 45 IRE
		white-to-sync = 143 IRE; note 2	recommended value: BLNNL = 53 (35H)
		BLNNL = 0; note 2	output blanking level = 26 IRE
		BLNNL = 63 (3FH); note 2	output blanking level = 46 IRE

Notes

1. Output black level/IRE = BLNNL $\times$ 2/6.29 + 25.4.
2. Output black level/IRE = BLNNL $\times$ 2/6.18 + 25.9; default after reset: 35H.

Table 44 Subaddress 5FH

DATA BYTE	DESCRIPTION
CCRS	select cross-colour reduction filter in luminance; see Table 45
BLNVB	variable blanking level during vertical blanking interval is typically identical to value of BLNNL

Table 45 Logic levels and function of CCRS

CCRS1	CCRS0	DESCRIPTION
0	0	no cross-colour reduction; for overall transfer characteristic of luminance see Fig.6
0	1	cross-colour reduction #1 active; for overall transfer characteristic see Fig.6
1	0	cross-colour reduction #2 active; for overall transfer characteristic see Fig.6
1	1	cross-colour reduction #3 active; for overall transfer characteristic see Fig.6

Table 46 Subaddress 61H

DATA BYTE	LOGIC LEVEL	DESCRIPTION
DOWND	0	digital core in normal operational mode; default after reset
	1	digital core in sleep mode and is reactivated with an I^2C-bus address
DOWNA	0	DACs in normal operational mode; default after reset
	1	DACs in power-down mode
INPI	0	PAL switch phase is nominal; default after reset
	1	PAL switch is inverted compared to nominal if RTCE = 1
YGS	0	luminance gain for white − black 100 IRE
	1	luminance gain for white − black 92.5 IRE including 7.5 IRE set-up of black
SCBW	0	enlarged bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 4 and 5)
	1	standard bandwidth for chrominance encoding (for overall transfer characteristic of chrominance in baseband representation see Figs 4 and 5); default after reset
PAL	0	NTSC encoding (non-alternating V component)
	1	PAL encoding (alternating V component)
FISE	0	864 total pixel clocks per line
	1	858 total pixel clocks per line

Table 47 Subaddress 62H

DATA BYTE	LOGIC LEVEL	DESCRIPTION	CONDITIONS	REMARKS
RTCE	0	no real-time control of generated subcarrier frequency; default after reset		
	1	real-time control of generated subcarrier frequency through a Philips video decoder; for a specification of the RTC protocol see document *"RTC Functional Description"*, available on request		
BSTA	–	amplitude of colour burst; input representation in accordance with *"ITU-R BT.601"*	white-to-black = 92.5 IRE; burst = 40 IRE; NTSC encoding BSTA = 0 to 2.02 × nominal	recommended value: BSTA = 63 (3FH)
			white-to-black = 92.5 IRE; burst = 40 IRE; PAL encoding BSTA = 0 to 2.82 × nominal	recommended value: BSTA = 45 (2DH)
			white-to-black = 100 IRE; burst = 43 IRE; NTSC encoding BSTA = 0 to 1.90 × nominal	recommended value: BSTA = 67 (43H)
			white-to-black = 100 IRE; burst = 43 IRE; PAL encoding BSTA = 0 to 3.02 × nominal	recommended value: BSTA = 47 (2FH); default after reset

Table 48 Subaddresses 63H to 66H (four bytes to program subcarrier frequency)

DATA BYTE	DESCRIPTION	CONDITIONS	REMARKS
FSC0 to FSC3	f_{fsc} = subcarrier frequency (in multiples of line frequency); f_{llc} = clock frequency (in multiples of line frequency)	$FSC = round\left(\frac{f_{fsc}}{f_{llc}} \times 2^{32}\right)$; note 1	FSC3 = most significant byte; FSC0 = least significant byte

Note

1. Examples:
   a) NTSC M: f_{fsc} = 227.5, f_{llc} = 1716 → FSC = 569408543 (21F07C1FH).
   b) PAL B/G: f_{fsc} = 283.7516, f_{llc} = 1728 → FSC = 705268427 (2A098ACBH).

Table 49 Subaddresses 67H to 6AH

DATA BYTE	DESCRIPTION	REMARKS
L21O0	first byte of captioning data, odd field	LSBs of the respective bytes are encoded immediately after run-in and framing code, the MSBs of the respective bytes have to carry the parity bit, in accordance with the definition of line 21 encoding format.
L21O1	second byte of captioning data, odd field	
L21E0	first byte of extended data, even field	
L21E1	second byte of extended data, even field	

Table 50 Subaddresses 6CH and 6DH

DATA BYTE	DESCRIPTION
HTRIG	sets the horizontal trigger phase related to chip-internal horizontal input values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed; increasing HTRIG decreases delays of all internally generated timing signals; the default value is 0

Table 51 Subaddress 6DH

DATA BYTE	DESCRIPTION
VTRIG	sets the vertical trigger phase related to chip-internal vertical input increasing VTRIG decreases delays of all internally generated timing signals, measured in half lines; variation range of VTRIG = 0 to 31 (1FH); the default value is 0

Table 52 Subaddress 6EH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
NVTRIG	0	values of the VTRIG register are positive
	1	values of the VTRIG register are negative
BLCKON	0	encoder in normal operation mode; default after reset
	1	output signal is forced to blanking level
PHRES	–	selects the phase reset mode of the colour subcarrier generator; see Table 53
LDEL	–	selects the delay on luminance path with reference to chrominance path; see Table 54
FLC	–	field length control; see Table 55

Table 53 Logic levels and function of PHRES

DATA BYTE		DESCRIPTION
PHRES1	PHRES0	
0	0	no subcarrier reset
0	1	subcarrier reset every two lines
1	0	subcarrier reset every eight fields
1	1	subcarrier reset every four fields

Table 54 Logic levels and function of LDEL

DATA BYTE		DESCRIPTION
LDEL1	LDEL0	
0	0	no luminance delay; default after reset
0	1	1 LLC luminance delay
1	0	2 LLC luminance delay
1	1	3 LLC luminance delay

Table 55 Logic levels and function of FLC

DATA BYTE		DESCRIPTION
FLC1	FLC0	
0	0	interlaced 312.5 lines/field at 50 Hz, 262.5 lines/field at 60 Hz; default after reset
0	1	non-interlaced 312 lines/field at 50 Hz, 262 lines/field at 60 Hz
1	0	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz
1	1	non-interlaced 313 lines/field at 50 Hz, 263 lines/field at 60 Hz

Table 56 Subaddress 6FH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
CCEN	–	enables individual line 21 encoding; see Table 57
TTXEN	0	disables teletext insertion; default after reset
	1	enables teletext insertion
SCCLN	–	selects the actual line, where Closed Caption or extended data are encoded; line = (SCCLN + 4) for M-systems; line = (SCCLN + 1) for other systems

Table 57 Logic levels and function of CCEN

DATA BYTE		DESCRIPTION
CCEN1	CCEN0	
0	0	line 21 encoding off; default after reset
0	1	enables encoding in field 1 (odd)
1	0	enables encoding in field 2 (even)
1	1	enables encoding in both fields

Table 58 Subaddresses 70H to 72H

DATA BYTE	DESCRIPTION
ADWHS	active display window horizontal start; defines the start of the active TV display portion after the border colour values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed
ADWHE	active display window horizontal end; defines the end of the active TV display portion before the border colour values above 1715 (FISE = 1) or 1727 (FISE = 0) are not allowed

Table 59 Subaddress 73H

DATA BYTE	DESCRIPTION	REMARKS
TTXHS	start of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0); see Fig.15	TTXHS = 42H; is default after reset if strapped to PAL
		TTXHS = 54H; is default after reset if strapped to NTSC

Table 60 Subaddress 74H

DATA BYTE	DESCRIPTION	REMARKS
TTXHD	indicates the delay in clock cycles between rising edge of TTXRQ output signal on pin TTXRQ_XCLKO2 (CLK2EN = 0) and valid data at pin TTX_SRES	minimum value: TTXHD = 2; is default after reset

Table 61 Subaddress 75H

DATA BYTE	DESCRIPTION
CSYNCA	advanced composite sync against RGB output from 0 XTAL clocks to 31 XTAL clocks

Table 62 Subaddresses 76H, 77H and 7CH

DATA BYTE	DESCRIPTION	REMARKS
TTXOVS	first line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0) in odd field line = (TTXOVS + 4) for M-systems line = (TTXOVS + 1) for other systems	TTXOVS = 05H; is default after reset if strapped to PAL TTXOVS = 06H; is default after reset if strapped to NTSC
TTXOVE	last line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0) in odd field line = (TTXOVE + 3) for M-systems line = TTXOVE for other systems	TTXOVE = 16H; is default after reset if strapped to PAL TTXOVE = 10H; is default after reset if strapped to NTSC

Table 63 Subaddresses 78H, 79H and 7CH

DATA BYTE	DESCRIPTION	REMARKS
TTXEVS	first line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0) in even field line = (TTXEVS + 4) for M-systems line = (TTXEVS + 1) for other systems	TTXEVS = 04H; is default after reset if strapped to PAL TTXEVS = 05H; is default after reset if strapped to NTSC
TTXEVE	last line of occurrence of signal TTXRQ on pin TTXRQ_XCLKO2 (CLK2EN = 0) in even field line = (TTXEVE + 3) for M-systems line = TTXEVE for other systems	TTXEVE = 16H; is default after reset if strapped to PAL TTXEVE = 10H; is default after reset if strapped to NTSC

Table 64 Subaddresses 7AH to 7CH

DATA BYTE	DESCRIPTION
FAL	first active line = FAL + 4 for M-systems and FAL + 1 for other systems, measured in lines FAL = 0 coincides with the first field synchronization pulse
LAL	last active line = LAL + 3 for M-systems and LAL for other system, measured in lines LAL = 0 coincides with the first field synchronization pulse

Table 65 Subaddress 7CH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
TTX60	0	enables NABTS (FISE = 1) or European TTX (FISE = 0); default after reset
	1	enables world standard teletext 60 Hz (FISE = 1)
TTXO	0	new teletext protocol selected; at each rising edge of TTXRQ a single teletext bit is requested (see Fig.15); default after reset
	1	old teletext protocol selected; the encoder provides a window of TTXRQ going HIGH; the length of the window depends on the chosen teletext standard (see Fig.15)

Table 66 Subaddresses 7EH and 7FH

DATA BYTE	DESCRIPTION
LINE	individual lines in both fields (PAL counting) can be disabled for insertion of teletext by the respective bits, disabled line = LINExx (50 Hz field rate) this bit mask is effective only if the lines are enabled by TTXOVS/TTXOVE and TTXEVS/TTXEVE

Table 67 Subaddresses 81H to 83H

DATA BYTE	DESCRIPTION
PCL	defines the frequency of the synthesized pixel clock PIXCLKO; $f_{PIXCLK} = \left(\frac{PCL}{2^{24}} \times f_{XTAL}\right) \times 8$; f_{XTAL} = 27 MHz nominal, e.g. 640 × 480 to NTSC M: PCL = 20F63BH; 640 × 480 to PAL B/G: PCL = 1B5A73H (as by strapping pins)

Table 68 Subaddress 84H

DATA BYTE	LOGIC LEVEL	DESCRIPTION
DCLK	0	pixel clock input is differential, pin $\overline{\text{PIXCLKI}}$ receives the inverted clock; default after reset
	1	pixel clock input is single ended, pin $\overline{\text{PIXCLKI}}$ has no function
PCLSY	0	pixel clock generator runs free; default after reset
	1	pixel clock generator gets synchronized with the vertical sync
IFRA	0	input FIFO gets reset explicitly at falling edge
	1	input FIFO gets reset every field; default after reset
IFBP	0	input FIFO is active
	1	input FIFO is bypassed; default after reset
PCLE	–	controls the divider for the external pixel clock; see Table 69
PCLI	–	controls the divider for the internal pixel clock; see Table 70

Table 69 Logic levels and function of PCLE

DATA BYTE		DESCRIPTION
PCLE1	PCLE0	
0	0	divider ratio for PIXCLK output is 1
0	1	divider ratio for PIXCLK output is 2; default after reset
1	0	divider ratio for PIXCLK output is 4
1	1	divider ratio for PIXCLK output is 8

Table 70 Logic levels and function of PCLI

DATA BYTE		DESCRIPTION
PCLI1	PCLI0	
0	0	divider ratio for internal PIXCLK is 1
0	1	divider ratio for internal PIXCLK is 2; default after reset
1	0	divider ratio for internal PIXCLK is 4
1	1	not allowed

Table 71 Subaddress 85H

DATA BYTE	LOGIC LEVEL	DESCRIPTION
EIDIV	0	set to logic 0 if DVO compliant signals are applied; default after reset
	1	set to logic 1 if non-DVO compliant signals are applied
FILI	–	threshold for FIFO internal transfers; nominal value is 8; default after reset

Table 72 Subaddresses 90H and 94H

DATA BYTE	DESCRIPTION
XOFS	horizontal offset; defines the number of PIXCLKs from horizontal sync (HSVGC) output to composite blanking ($\overline{\text{CBO}}$) output

Table 73 Subaddresses 91H and 94H

DATA BYTE	DESCRIPTION
XPIX	pixel in X direction; defines half the number of active pixels per input line (identical to the length of $\overline{CBO}$ pulses)

Table 74 Subaddresses 92H and 94H

DATA BYTE	DESCRIPTION
YOFSO	vertical offset in odd field; defines (in the odd field) the number of lines from VSVGC to first line with active $\overline{CBO}$; if no LUT data is requested, the first active $\overline{CBO}$ will be output at YOFSO + 2; usually, YOFSO = YOFSE with the exception of extreme vertical downscaling and interlacing

Table 75 Subaddresses 93H and 94H

DATA BYTE	DESCRIPTION
YOFSE	vertical offset in even field; defines (in the even field) the number of lines from VSVGC to first line with active $\overline{CBO}$; if no LUT data is requested, the first active $\overline{CBO}$ will be output at YOFSE + 2; usually, YOFSE = YOFSO with the exception of extreme vertical downscaling and interlacing

Table 76 Subaddresses 95H and 96H

DATA BYTE	DESCRIPTION
YPIX	defines the number of requested input lines from the feeding device; number of requested lines = YPIX + YOFSE – YOFSO

Table 77 Subaddress 96H

DATA BYTE	LOGIC LEVEL	DESCRIPTION
EFS	0	frame sync signal at pin FSVGC ignored in slave mode
	1	frame sync signal at pin FSVGC accepted in slave mode
PCBN	0	normal polarity of $\overline{CBO}$ signal (HIGH during active video)
	1	inverted polarity of $\overline{CBO}$ signal (LOW during active video)
SLAVE	0	the SAA7104H; SAA7105H is timing master to the graphics controller
	1	the SAA7104H; SAA7105H is timing slave to the graphics controller
ILC	0	if hardware cursor insertion is active, set LOW for non-interlaced input signals
	1	if hardware cursor insertion is active, set HIGH for interlaced input signals
YFIL	0	luminance sharpness booster disabled
	1	luminance sharpness booster enabled

Table 78 Subaddress 97H

DATA BYTE	LOGIC LEVEL	DESCRIPTION
HFS	0	horizontal sync is directly derived from input signal (slave mode) at pin HSVGC
	1	horizontal sync is derived from a frame sync signal (slave mode) at pin FSVGC (only if EFS is set HIGH)
VFS	0	vertical sync (field sync) is directly derived from input signal (slave mode) at pin VSVGC
	1	vertical sync (field sync) is derived from a frame sync signal (slave mode) at pin FSVGC (only if EFS is set HIGH)
OFS	0	pin FSVGC is switched to input
	1	pin FSVGC is switched to active output
PFS	0	polarity of signal at pin FSVGC in output mode (master mode) is active HIGH; rising edge of the input signal is used in slave mode
	1	polarity of signal at pin FSVGC in output mode (master mode) is active LOW; falling edge of the input signal is used in slave mode
OVS	0	pin VSVGC is switched to input
	1	pin VSVGC is switched to active output
PVS	0	polarity of signal at pin VSVGC in output mode (master mode) is active HIGH; rising edge of the input signal is used in slave mode
	1	polarity of signal at pin VSVGC in output mode (master mode) is active LOW; falling edge of the input signal is used in slave mode
OHS	0	pin HSVGC is switched to input
	1	pin HSVGC is switched to active output
PHS	0	polarity of signal at pin HSVGC in output mode (master mode) is active HIGH; rising edge of the input signal is used in slave mode
	1	polarity of signal at pin HSVGC in output mode (master mode) is active LOW; falling edge of the input signal is used in slave mode

Table 79 Subaddresses 98H and 99H

DATA BYTE	DESCRIPTION
HLEN	horizontal length; $HLEN = \frac{\text{number of PIXCLKs}}{\text{line}} - 1$

Table 80 Subaddress 99H

DATA BYTE	DESCRIPTION
IDEL	input delay; defines the distance in PIXCLKs between the active edge of $\overline{CBO}$ and the first received valid pixel

Table 81 Subaddresses 9AH and 9CH

DATA BYTE	DESCRIPTION
XINC	incremental fraction of the horizontal scaling engine; $XINC = \frac{\frac{\text{number of output pixels}}{\text{line}}}{\frac{\text{number of input pixels}}{\text{line}}} \times 4096$

Table 82 Subaddresses 9BH and 9CH

DATA BYTE	DESCRIPTION
YINC	incremental fraction of the vertical scaling engine; $YINC = \frac{\text{number of active output lines}}{\text{number of active input lines}} \times 4096$

Table 83 Subaddresses 9DH and 9FH

DATA BYTE	DESCRIPTION
YIWGTO	weighting factor for the first line of the odd field; $YIWGTO = \frac{YINC}{2} + 2048$

Table 84 Subaddresses 9EH and 9FH

DATA BYTE	DESCRIPTION
YIWGTE	weighting factor for the first line of the even field; $YIWGTE = \frac{YINC - YSKIP}{2}$

Table 85 Subaddresses A0H and A1H

DATA BYTE	DESCRIPTION
YSKIP	vertical line skip; defines the effectiveness of the anti-flicker filter; YSKIP = 0: most effective; YSKIP = 4095: anti-flicker filter switched off

Table 86 Subaddress A1H

DATA BYTE	LOGIC LEVEL	DESCRIPTION
BLEN	0	no internal blanking for non-interlaced graphics in bypass mode; default after reset
	1	forced internal blanking for non-interlaced graphics in bypass mode

Table 87 Subaddresses A2H to A4H

DATA BYTE	DESCRIPTION
BCY, BCU and BCV	luminance and colour difference portion of border colour in underscan area

Table 88 Subaddress D0H

DATA BYTE	DESCRIPTION
HLCA	RAM start address for the HD sync line count array; the byte following subaddress D0 points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition. Each line count array entry consists of 2 bytes; see Table 89. The array has 15 entries.
HLC	HD line counter. The system will repeat the pattern described in 'HLT' HLC times and then start with the next entry in line count array.
HLT	HD line type pointer. If not 0, the value points into the line type array, index HLT − 1 with the description of the current line. 0 means the entry is not used.

Table 89 Layout of the data bytes in the line count array

BYTE	DESCRIPTION							
0	HLC7	HLC6	HLC5	HLC4	HLC3	HLC2	HLC1	HLC0
1	HLT3	HLT2	HLT1	HLT0	0	0	HLC9	HLC8

Table 90 Subaddress D1H

DATA BYTE	DESCRIPTION
HLTA	RAM start address for the HD sync line type array; the byte following subaddress D1 points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition. Each line type array entry consists of 4 bytes; see Table 91. The array has 15 entries.
HLP	HD line type; if not 0, the value points into the line pattern array. The index used is HLP − 1. It consists of value-duration pairs. Each entry consists of 8 pointers, used from index 0 to 7. The value 0 means that the entry is not used.

Table 91 Layout of the data bytes in the line type array

BYTE	DESCRIPTION							
0	0	HLP12	HLP11	HLP10	0	HLP02	HLP01	HLP00
1	0	HLP32	HLP31	HLP30	0	HLP22	HLP21	HLP20
2	0	HLP52	HLP51	HLP50	0	HLP42	HLP41	HLP40
3	0	HLP72	HLP71	HLP70	0	HLP62	HLP61	HLP60

Table 92 Subaddress D2H

DATA BYTE	DESCRIPTION
HLPA	RAM start address for the HD sync line pattern array; the byte following subaddress D2 points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition. Each line pattern array entry consists of 4 value-duration pairs occupying 2 bytes; see Table 93. The array has 7 entries.
HPD	HD pattern duration. The value defines the time in pixel clocks (HPD + 1) the corresponding value HPV is added to the HD output signal. If 0, this entry will be skipped.
HPV	HD pattern value pointer. This gives the index in the HD value array containing the level to be inserted into the HD output path. If the MSB of HPV is logic 1, the value will only be inserted into the Y/GREEN channel of the HD data path, the other channels remain unchanged.

Table 93 Layout of the data bytes in the line pattern array

BYTE	DESCRIPTION							
0	HPD07	HPD06	HPD05	HPD04	HPD03	HPD02	HPD01	HPD00
1	HPV03	HPV02	HPV01	HPV00	0	0	HPD09	HPD08
2	HPD17	HPD16	HPD14	HPD14	HPD13	HPD12	HPD11	HPD10
3	HPV13	HPV12	HPV11	HPV10	0	0	HPD19	HPD18
4	HPD27	HPD26	HPD25	HPD24	HPD23	HPD22	HPD21	HPD20
5	HPV23	HPV22	HPV21	HPV20	0	0	HPD29	HPD28
6	HPD37	HPD36	HPD35	HPD34	HPD33	HPD32	HPD31	HPD30
7	HPV33	HPV32	HPV31	HPV30	0	0	HPD39	HPD38

Table 94 Subaddress D3H

DATA BYTE	DESCRIPTION
HPVA	RAM start address for the HD sync value array; the byte following subaddress D3 points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition. Each line pattern array entry consists of 2 bytes. The array has 8 entries.
HPVE	HD pattern value entry. The HD path will insert a level of (HPV + 52) $\times$ 0.66 IRE into the data path. The value is signed 8-bits wide; see Table 95.
HHS	HD horizontal sync. If the HD engine is active, this value will be provided at pin HSM_CSYNC; see Table 95.
HVS	HD vertical sync. If the HD engine is active, this value will be provided at pin VSM; see Table 95.

Table 95 Layout of the data bytes in the value array

BYTE	DESCRIPTION							
0	HPVE7	HPVE6	HPVE5	HPVE4	HPVE3	HPVE2	HPVE1	HPVE0
1	0	0	0	0	0	0	HVS	HHS

Table 96 Subaddresses D4H and D5H

DATA BYTE	DESCRIPTION
HLCT	state of the HD line counter after trigger, note that it counts backwards
HLCPT	state of the HD line type pointer after trigger
HLPPT	state of the HD pattern pointer after trigger

Table 97 Subaddresses D6H and D7H

DATA BYTE	DESCRIPTION
HDCT	state of the HD duration counter after trigger, note that it counts backwards
HEPT	state of the HD event type pointer in the line type array after trigger

Table 98 Subaddresses D8H and D9H

DATA BYTE	DESCRIPTION
HTX	horizontal trigger phase for the HD sync engine in pixel clocks

Table 99 Subaddresses DAH and DBH

DATA BYTE	DESCRIPTION
HTY	vertical trigger phase for the HD sync engine in input lines

Table 100 Subaddress DCH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
HDSYE	0	the HD sync engine is off; default after reset
	1	the HD sync engine is active
HDTC	0	HD output path processes RGB; default after reset
	1	HD output path processes YUV
HDGY	0	gain in the HD output path is reduced, insertion of sync pulses is possible; default after reset
	1	full level swing at the input causes full level swing at the DACs in HD mode
HDIP	0	interpolator for the colour difference signal in the HD output path is active; default after reset
	1	interpolator for the colour difference signals in the HD output path is off

Table 101 Subaddresses F0H to F2H

DATA BYTE	DESCRIPTION
CC1R, CC1G and CC1B	RED, GREEN and BLUE portion of first cursor colour

Table 102 Subaddresses F3H to F5H

DATA BYTE	DESCRIPTION
CC2R, CC2G and CC2B	RED, GREEN and BLUE portion of second cursor colour

Table 103 Subaddresses F6H to F8H

DATA BYTE	DESCRIPTION
AUXR, AUXG and AUXB	RED, GREEN and BLUE portion of auxiliary cursor colour

Table 104 Subaddresses F9H and FAH

DATA BYTE	DESCRIPTION
XCP	horizontal cursor position

Table 105 Subaddress FAH

DATA BYTE	DESCRIPTION
XHS	horizontal hot spot of cursor

Table 106 Subaddresses FBH and FCH

DATA BYTE	DESCRIPTION
YCP	vertical cursor position

Table 107 Subaddress FCH

DATA BYTE	DESCRIPTION
YHS	vertical hot spot of cursor

Table 108 Subaddress FDH

DATA BYTE	LOGIC LEVEL	DESCRIPTION
LUTOFF	0	colour look-up table is active
	1	colour look-up table is bypassed
CMODE	0	cursor mode; input colour will be inverted
	1	auxiliary cursor colour will be inserted
LUTL	0	LUT loading via input data stream is inactive
	1	colour and cursor LUTs are loaded via input data stream
IF	0	input format is 8 + 8 + 8-bit 4 : 4 : 4 non-interlaced RGB or C_B-Y-C_R
	1	input format is 5 + 5 + 5-bit 4 : 4 : 4 non-interlaced RGB
	2	input format is 5 + 6 + 5-bit 4 : 4 : 4 non-interlaced RGB
	3	input format is 8 + 8 + 8-bit 4 : 2 : 2 non-interlaced C_B-Y-C_R
	4	input format is 8 + 8 + 8-bit 4 : 2 : 2 interlaced C_B-Y-C_R (ITU-R BT.656, 27 MHz clock) (in subaddresses 91H and 94H set XPIX = number of active pixels/line)
	5	input format is 8-bit non-interlaced index colour
	6	input format is 8 + 8 + 8-bit 4 : 4 : 4 non-interlaced RGB or C_B-Y-C_R (special bit ordering)
MATOFF	0	RGB to C_R-Y-C_B matrix is active
	1	RGB to C_R-Y-C_B matrix is bypassed
DFOFF	0	down formatter (4 : 4 : 4 to 4 : 2 : 2) in input path is active
	1	down formatter is bypassed

Table 109 Subaddress FEH

DATA BYTE	DESCRIPTION
CURSA	RAM start address for cursor bit map; the byte following subaddress FEH points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition

Table 110 Subaddress FFH

DATA BYTE	DESCRIPTION
COLSA	RAM start address for colour LUT; the byte following subaddress FFH points to the first cell to be loaded with the next transmitted byte; succeeding cells are loaded by auto-incrementing until stop condition

In subaddresses 5BH, 5CH, 5DH, 5EH, 62H and D3H all IRE values are rounded up.

7.25 Slave transmitter

Table 111 Slave transmitter (slave address 89H)

REGISTER FUNCTION	SUBADDRESS	DATA BYTE							
		D7	D6	D5	D4	D3	D2	D1	D0
Status byte	00H	VER2	VER1	VER0	CCRDO	CCRDE	0	FSEQ	O_E
Chip ID	1CH	CID7	CID6	CID5	CID4	CID3	CID2	CID1	CID0
FIFO status	80H	0	0	0	0	0	0	OVFL	UDFL

Table 112 Subaddress 00H

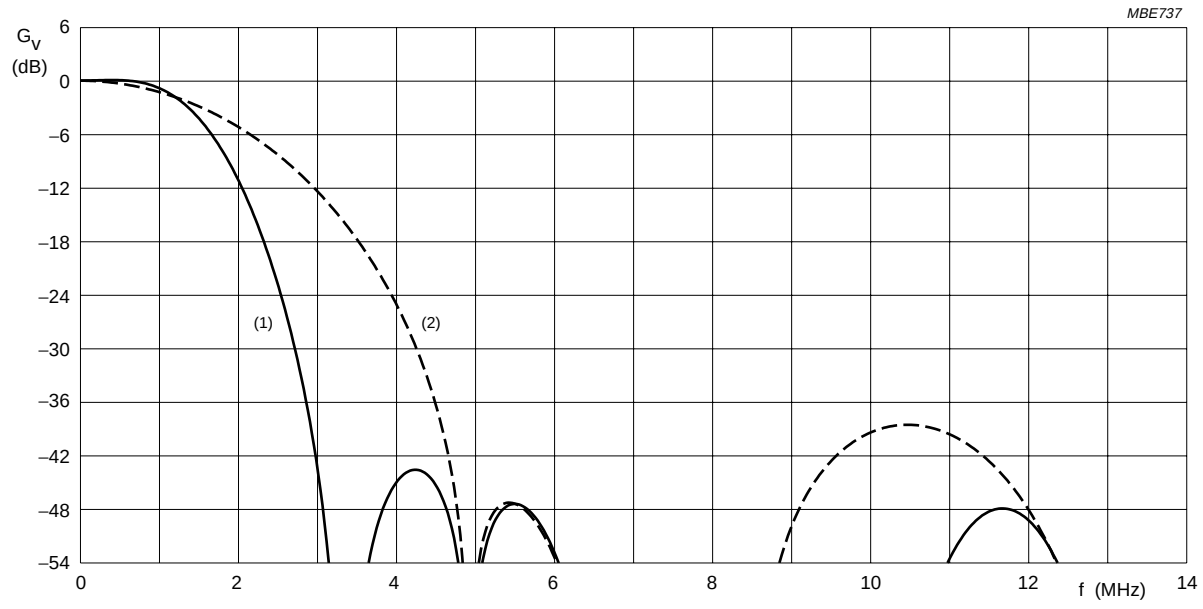
DATA BYTE	LOGIC LEVEL	DESCRIPTION
VER	–	version identification of the device: it will be changed with all versions of the IC that have different programming models; current version is 101 binary
CCRDO	1	Closed Caption bytes of the odd field have been encoded
	0	the bit is reset after information has been written to the subaddresses 67H and 68H; it is set immediately after the data has been encoded
CCRDE	1	Closed Caption bytes of the even field have been encoded
	0	the bit is reset after information has been written to the subaddresses 69H and 6AH; it is set immediately after the data has been encoded
FSEQ	1	during first field of a sequence (repetition rate: NTSC = 4 fields, PAL = 8 fields)
	0	not first field of a sequence
O_E	1	during even field
	0	during odd field

Table 113 Subaddress 1CH

DATA BYTE	DESCRIPTION
CID	chip ID of SAA7104H = 04H; chip ID of SAA7105H = 05H

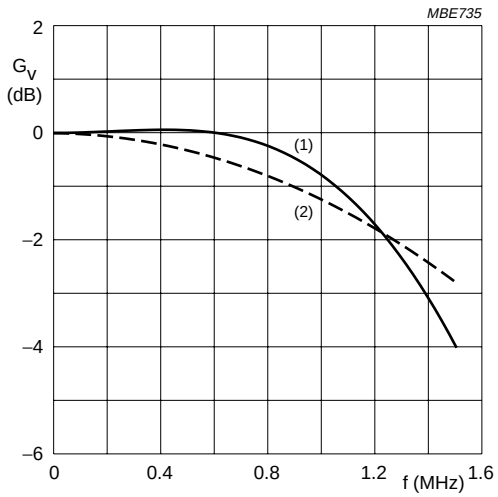
Table 114 Subaddress 80H

DATA BYTE	LOGIC LEVEL	DESCRIPTION
IFERR	0	normal FIFO state
	1	input FIFO overflow/underflow has occurred
BFERR	0	normal FIFO state
	1	buffer FIFO overflow, only if YUPSC = 1
OVFL	0	no FIFO overflow
	1	FIFO overflow has occurred; this bit is reset after this subaddress has been read
UDFL	0	no FIFO underflow
	1	FIFO underflow has occurred; this bit is reset after this subaddress has been read



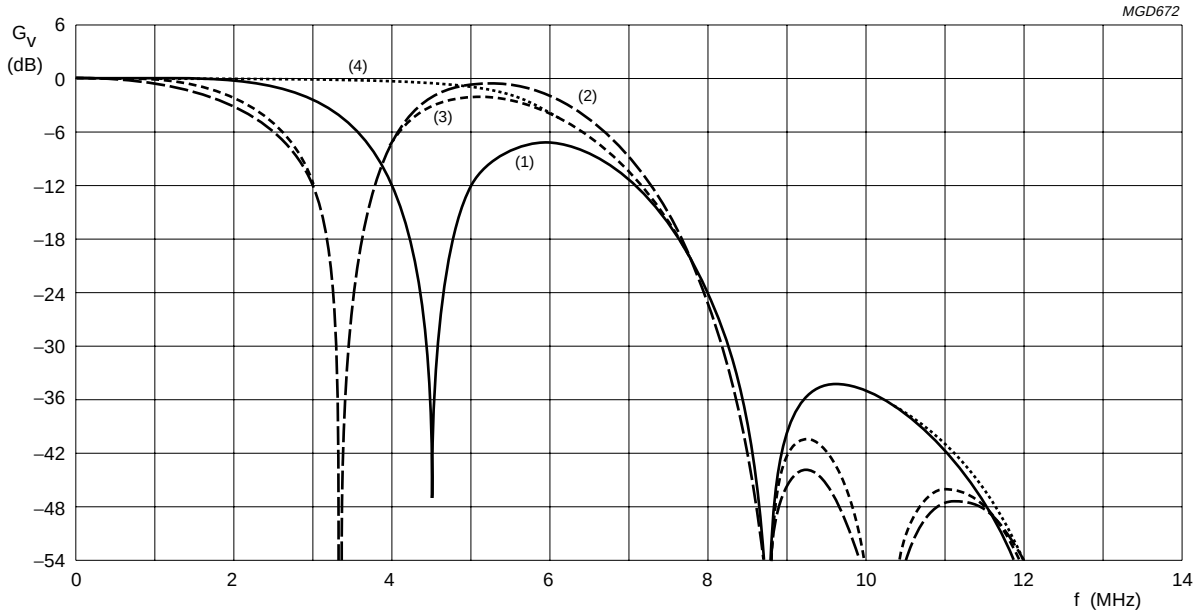
(1) SCBW = 1.
(2) SCBW = 0.

Fig.4 Chrominance transfer characteristic 1.



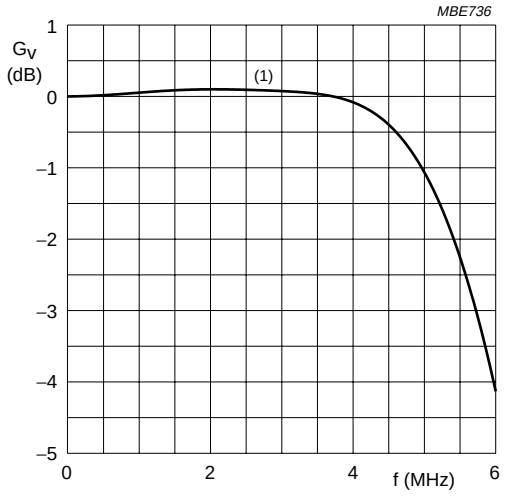
(1) SCBW = 1.
(2) SCBW = 0.

Fig.5 Chrominance transfer characteristic 2.



(1) CCRS1 = 0; CCRS) = 1.
(2) CCRS1 = 1; CCRS) = 0.
(3) CCRS1 = 1; CCRS) = 1.
(4) CCRS1 = 0; CCRS) = 0.

Fig.6 Luminance transfer characteristic 1 (excluding scaler).



(1) CCRS1 = 0; CCRS0 = 0.

Fig.7 Luminance transfer characteristic 2(excluding scaler).

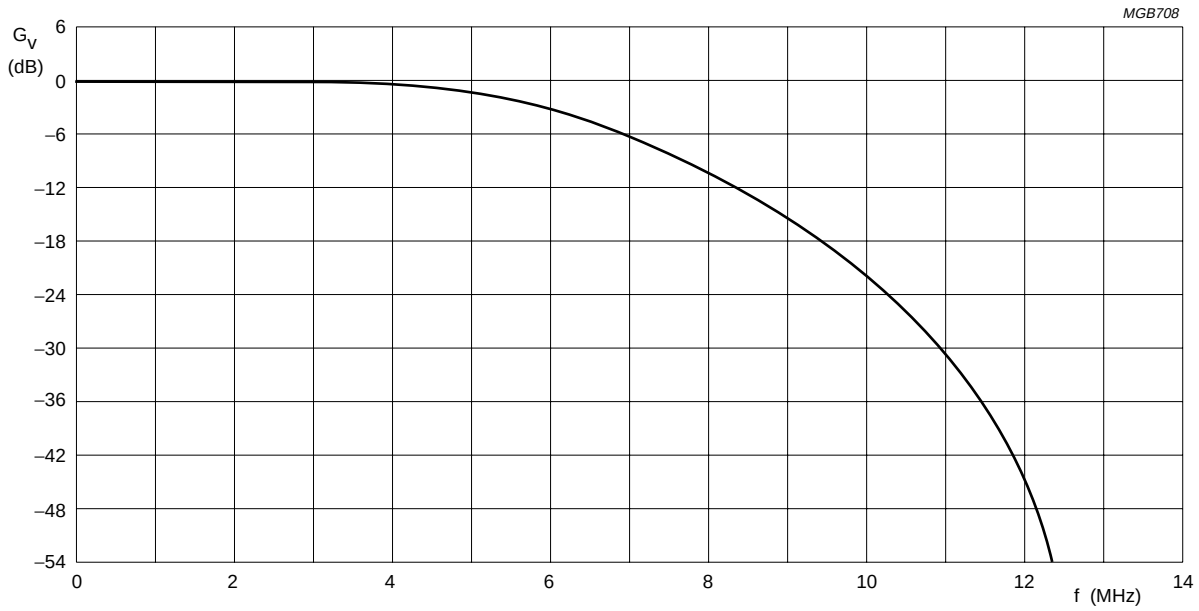


Fig.8 Luminance transfer characteristic in RGB (excluding scaler).

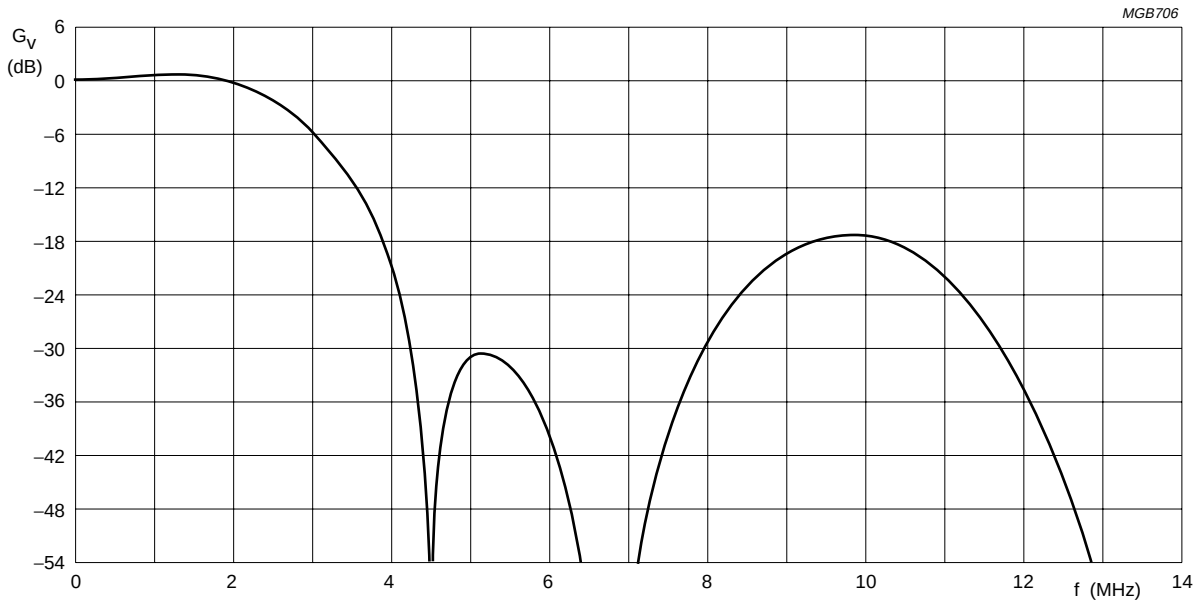


Fig.9 Colour difference transfer characteristic in RGB (excluding scaler).

8 BOUNDARY SCAN TEST

The SAA7104H; SAA7105H has built-in logic and 5 dedicated pins to support boundary scan testing which allows board testing without special hardware (nails). The SAA7104H; SAA7105H follows the *"IEEE Std. 1149.1 - Standard Test Access Port and Boundary-Scan Architecture"* set by the Joint Test Action Group (JTAG) chaired by Philips.

The 5 special pins are Test Mode Select (TMS), Test Clock (TCK), Test Reset ($\overline{\text{TRST}}$), Test Data Input (TDI) and Test Data Output (TDO).

The Boundary Scan Test (BST) functions BYPASS, EXTEST, INTEST, SAMPLE, CLAMP and IDCODE are all supported; see Table 115. Details about the JTAG BST-TEST can be found in the specification "*IEEE Std. 1149.1"*. A file containing the detailed Boundary Scan Description Language (BSDL) of the SAA7104H; SAA7105H is available on request.

Table 115 BST instructions supported by the SAA7104H; SAA7105H

INSTRUCTION	DESCRIPTION
BYPASS	This mandatory instruction provides a minimum length serial path (1 bit) between TDI and TDO when no test operation of the component is required.
EXTEST	This mandatory instruction allows testing of off-chip circuitry and board level interconnections.
SAMPLE	This mandatory instruction can be used to take a sample of the inputs during normal operation of the component. It can also be used to preload data values into the latched outputs of the boundary scan register.
CLAMP	This optional instruction is useful for testing when not all ICs have BST. This instruction addresses the bypass register while the boundary scan register is in external test mode.
IDCODE	This optional instruction will provide information on the components manufacturer, part number and version number.
INTEST	This optional instruction allows testing of the internal logic (no support for customer available).
USER1	This private instruction allows testing by the manufacturer (no support for customer available).

8.1 Initialization of boundary scan circuit

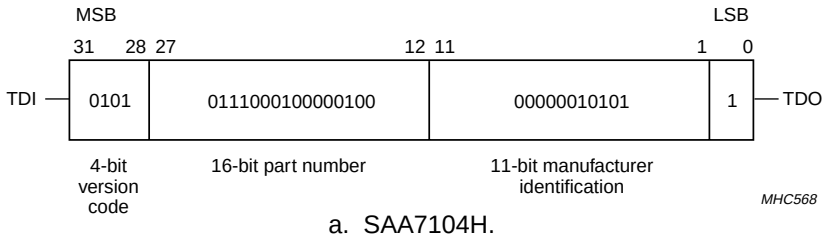
The Test Access Port (TAP) controller of an IC should be in the reset state (TEST_LOGIC_RESET) when the IC is in functional mode. This reset state also forces the instruction register into a functional instruction such as IDCODE or BYPASS.

To solve the power-up reset, the standard specifies that the TAP controller will be forced asynchronously to the TEST_LOGIC_RESET state by setting the $\overline{\text{TRST}}$ pin LOW.

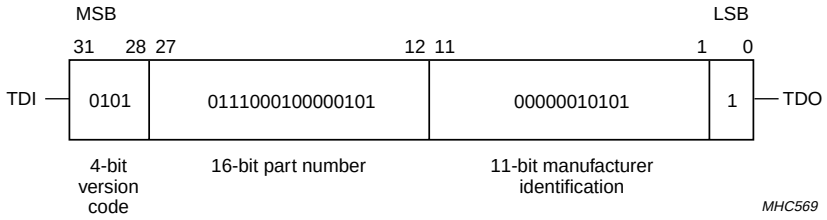
8.2 Device identification codes

A device identification register is specified in *"IEEE Std. 1149.1b-1994"*. It is a 32-bit register which contains fields for the specification of the IC manufacturer, the IC part number and the IC version number. Its biggest advantage is the possibility to check for the correct ICs mounted after production and to determine the version number of the ICs during field service.

When the IDCODE instruction is loaded into the BST instruction register, the identification register will be connected between TDI and TDO of the IC.
The identification register will load a component specific code during the CAPTURE_DATA_REGISTER state of the TAP controller, this code can subsequently be shifted out. At board level this code can be used to verify component manufacturer, type and version number. The device identification register contains 32 bits, numbered 31 to 0, where bit 31 is the most significant bit (nearest to TDI) and bit 0 is the least significant bit (nearest to TDO); see Fig.10.



a. SAA7104H.



b. SAA7105H.

Fig.10 32 bits of identification code.

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); all ground pins connected together and grounded (0 V); all supply pins connected together.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDD}	digital supply voltage		–0.5	+4.6	V
V_{DDA}	analog supply voltage		–0.5	+4.6	V
$V_{i(A)}$	input voltage at analog inputs		–0.5	+4.6	V
$V_{i(n)}$	input voltage at pins XTALI, SDA and SCL		–0.5	V_{DDD} + 0.5	V
$V_{i(D)}$	input voltage at digital inputs or I/O pins	outputs in 3-state	–0.5	+4.6	V
		outputs in 3-state; note 1	–0.5	+5.5	V
ΔV_{SS}	voltage difference between $V_{SSA(n)}$ and $V_{SSD(n)}$		–	100	mV
T_{stg}	storage temperature		–65	+150	°C
T_{amb}	ambient temperature		0	70	°C
V_{esd}	electrostatic discharge voltage	human body model; note 2	–	±2000	V
		machine model; note 3	–	±200	V

Notes

1. Condition for maximum voltage at digital inputs or I/O pins: 3.0 V < V_{DDD} < 3.6 V.
2. Class 2 according to EIA/JESD22-114-B.
3. Class B according to EIA/JESD22-115-A.

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	44[1]	K/W

Note

1. The overall $R_{th(j-a)}$ value can vary depending on the board layout. To minimize the effective $R_{th(j-a)}$ all power and ground pins must be connected to the power and ground layers directly. An ample copper area direct under the SAA7104H; SAA7105H with a number of through-hole plating, which connect to the ground layer (four-layer board: second layer), can also reduce the effective $R_{th(j-a)}$. Please do not use any solder-stop varnish under the chip. In addition the usage of soldering glue with a high thermal conductance after curing is recommended.

11 CHARACTERISTICS

T_{amb} = 0 to 70 °C (typical values excluded); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	analog supply voltage		3.15	3.3	3.45	V
V_{DDD2}, V_{DDD3}, V_{DDD4}	digital supply voltage		3.15	3.3	3.45	V
V_{DDD1}	digital supply voltage (DVO)		1.045	1.1	1.155	V
			1.425	1.5	1.575	V
			1.71	1.8	1.89	V
			2.375	2.5	2.625	V
			3.135	3.3	3.465	V
I_{DDA}	analog supply current	note 1	1	110	115	mA
I_{DDD}	digital supply current	note 2	1	175	200	mA
Inputs						
V_{IL}	LOW-level input voltage	V_{DDD1} = 1.1 V, 1.5 V, 1.8 V or 2.5 V; note 3	−0.1	–	+0.2	V
		V_{DDD1} = 3.3 V; note 3	−0.5	–	+0.8	V
		pins $\overline{\text{RESET}}$, TMS, TCK, $\overline{\text{TRST}}$ and TDI	−0.5	–	+0.8	V
V_{IH}	HIGH-level input voltage	V_{DDD1} = 1.1 V, 1.5 V, 1.8 V or 2.5 V; note 3	V_{DDD1} − 0.2	–	V_{DDD1} + 0.1	V
		V_{DDD1} = 3.3 V; note 3	2	–	V_{DDD1} + 0.3	V
		pins $\overline{\text{RESET}}$, TMS, TCK, $\overline{\text{TRST}}$ and TDI	2	–	V_{DDD2} + 0.3	V
I_{LI}	input leakage current		–	–	10	µA
C_i	input capacitance	clocks	–	–	10	pF
		data	–	–	10	pF
		I/Os at high-impedance	–	–	10	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Outputs						
V_{OL}	LOW-level output voltage	V_{DDD1} = 1.1 V, 1.5 V, 1.8 V or 2.5 V; note 3	0	–	0.1	V
		V_{DDD1} = 3.3 V; note 3	0	–	0.4	V
		pins TDO, TTXRQ_XCLKO2, VSM and HSM_CSYNC	0	–	0.4	V
V_{OH}	HIGH-level output voltage	V_{DDD1} = 1.1 V, 1.5 V, 1.8 V or 2.5 V; note 3	V_{DDD1} – 0.1	–	V_{DDD1}	V
		V_{DDD1} = 3.3 V; note 3	2.4	–	V_{DDD1}	V
		pins TDO, TTXRQ_XCLKO2, VSM and HSM_CSYNC	2.4	–	V_{DDD2}	V
I²C-bus; pins SDA and SCL						
V_{IL}	LOW-level input voltage		–0.5	–	$0.3V_{DDD2}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD2}$	–	V_{DDD2} + 0.3	V
I_i	input current	V_i = LOW or HIGH	–10	–	+10	µA
V_{OL}	LOW-level output voltage (pin SDA)	I_{OL} = 3 mA	–	–	0.4	V
I_o	output current	during acknowledge	3	–	–	mA
Clock timing; pins PIXCLKI and PIXCLKO						
T_{PIXCLK}	cycle time	note 4	12	–	–	ns
$t_{d(CLKD)}$	delay from PIXCLKO to PIXCLKI	note 5	–	–	–	ns
δ	duty factor t_{HIGH}/T_{PIXCLK}	note 4	40	50	60	%
	duty factor t_{HIGH}/T_{CLKO2}	output	40	50	60	%
t_r	rise time	note 4	–	–	1.5	ns
t_f	fall time	note 4	–	–	1.5	ns
Input timing						
$t_{SU;DAT}$	input data set-up time	pins PD11 to PD0, RTCI and TTX_SRES	2	–	–	ns
$t_{HD;DAT}$	input data hold time	pins PD11 to PD0, RTCI and TTX_SRES	1.5	–	–	ns
$t_{SU;DAT}$	input data set-up time	pins HSVGC, VSVGC and FSVGC; note 6	2	–	–	ns
$t_{HD;DAT}$	input data hold time	pins HSVGC, VSVGC and FSVGC; note 6	1.5	–	–	ns
Crystal oscillator						
f_{nom}	nominal frequency		–	27	–	MHz
$\Delta f/f_{nom}$	permissible deviation of nominal frequency	note 7	–50	–	+50	10^{-6}

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CRYSTAL SPECIFICATION						
T_{amb}	ambient temperature		0	–	70	°C
C_L	load capacitance		8	–	–	pF
R_S	series resistance		–	–	80	Ω
C_1	motional capacitance (typical)		1.2	1.5	1.8	fF
C_0	parallel capacitance (typical)		2.8	3.5	4.2	pF
Data and reference signal output timing						
$C_{o(L)}$	output load capacitance		8	–	40	pF
$t_{o(h)(gfx)}$	output hold time to graphics controller	pins HSVGC, VSVGC, FSVGC and $\overline{CBO}$	1.5	–	–	ns
$t_{o(d)(gfx)}$	output delay time to graphics controller	pins HSVGC, VSVGC, FSVGC and $\overline{CBO}$	–	–	10	ns
$t_{o(h)}$	output hold time	pins TDO, TTXRQ_XCLKO2, VSM and HSM_CSYNC	3	–	–	ns
$t_{o(d)}$	output delay time	pins TDO, TTXRQ_XCLKO2, VSM and HSM_CSYNC	–	–	25	ns
CVBS and RGB outputs						
$V_{o(CVBS)(p-p)}$	output voltage CVBS (peak-to-peak value)	see Table 116	–	1.23	–	V
$V_{o(VBS)(p-p)}$	output voltage VBS (S-video) (peak-to-peak value)	see Table 116	–	1	–	V
$V_{o(C)(p-p)}$	output voltage C (S-video) (peak-to-peak value)	see Table 116	–	0.89	–	V
$V_{o(RGB)(p-p)}$	output voltage R, G, B (peak-to-peak value)	see Table 116	–	0.7	–	V
ΔV_o	inequality of output signal voltages		–	2	–	%
$R_{o(L)}$	output load resistance		–	37.5	–	Ω
B_{DAC}	output signal bandwidth of DACs	−3 dB; note 8	–	170	–	MHz
$ILE_{lf(DAC)}$	low frequency integral linearity error of DACs		–	–	±3	LSB
$DLE_{lf(DAC)}$	low frequency differential linearity error of DACs		–	–	±1	LSB

Notes

1. Minimum value for I^2C-bus bit DOWNA = 1.
2. Minimum value for I^2C-bus bit DOWND = 1.
3. Levels refer to pins PD11 to PD0, $\overline{\text{PIXCLKI}}$, FSVGC, PIXCLKI, VSVGC, PIXCLKO, $\overline{\text{CBO}}$, TVD, and HSVGC, being inputs or outputs directly connected to a graphics controller.
   Input sensitivity is $^1/_2V_{DDD2}$ + 100 mV for HIGH and $^1/_2V_{DDD2}$ − 100 mV for LOW.
   The reference voltage $^1/_2V_{DDD2}$ is generated on chip.
4. The data is for both input and output direction.
5. This parameter is arbitrary, if PIXCLKI is looped through the VGC.
6. Tested with programming IFBP = 1.
7. If an internal oscillator is used, crystal deviation of nominal frequency is directly proportional to the deviation of subcarrier frequency and line/field frequency.
8. $B_{-3\,dB} = \frac{1}{2\pi R_L(C_{ext} + 5\,pF)}$ with R_L = 37.5 Ω and C_{ext} = 20 pF (typical).

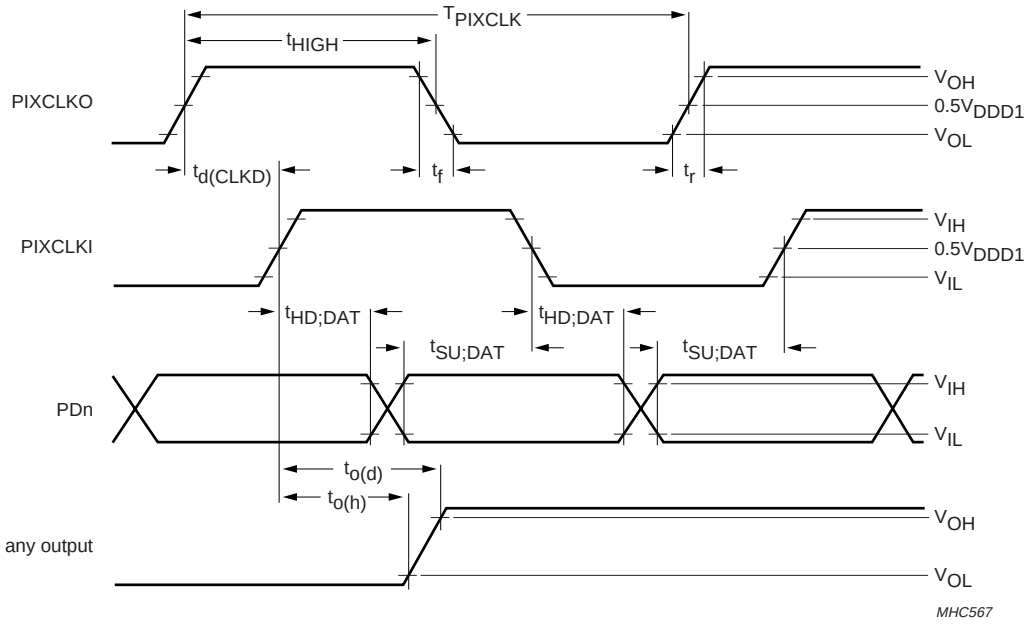


Fig.11 Input/output timing specification 1.

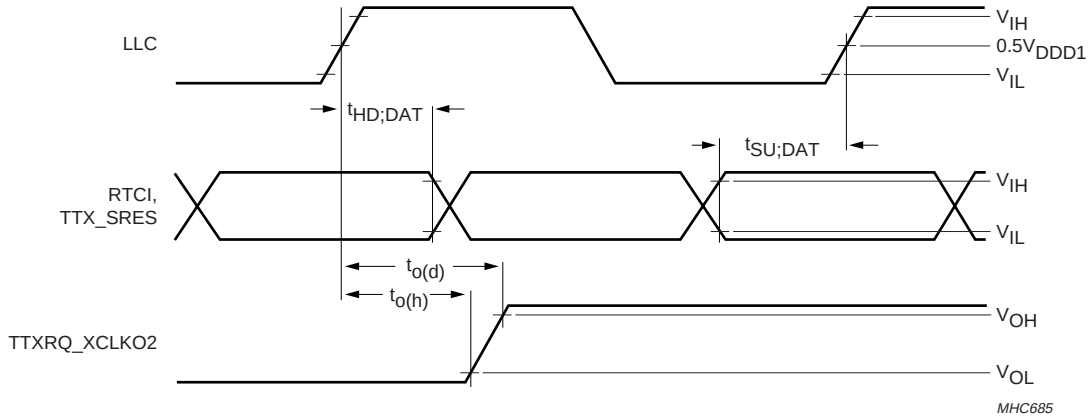


Fig.12 Input/output timing specification 2.

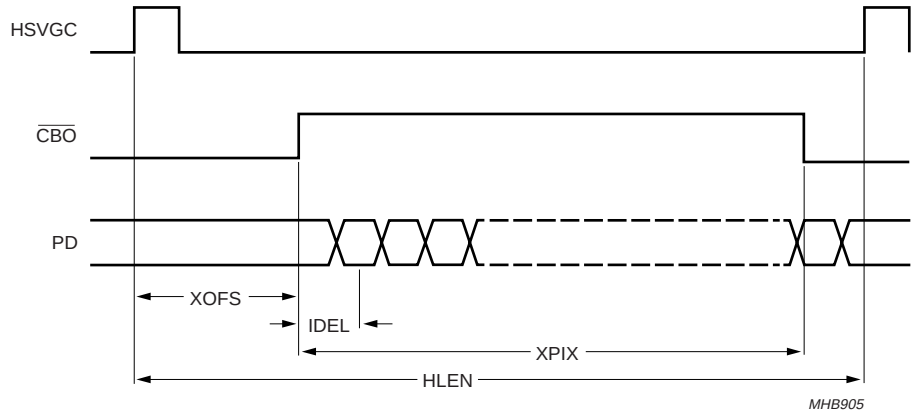


Fig.13 Horizontal input timing.

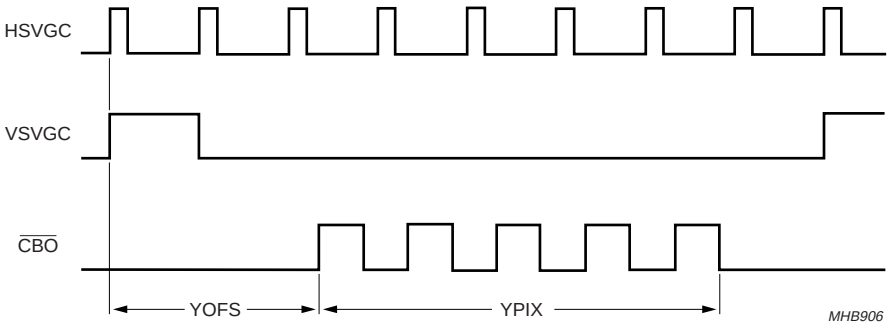


Fig.14 Vertical input timing.

11.1 Teletext timing

Time t_{FD} is the time needed to interpolate input data TTX and insert it into the CVBS and VBS output signal, such that it appears at t_{TTX} = 9.78 µs (PAL) or t_{TTX} = 10.5 µs (NTSC) after the leading edge of the horizontal synchronization pulse.

Time t_{PD} is the pipeline delay time introduced by the source that is gated by TTXRQ_XCLKO2 in order to deliver TTX data. This delay is programmable by register TTXHD. For every active HIGH state at output pin TTXRQ_XCLKO2, a new teletext bit must be provided by the source.

Since the beginning of the pulses representing the TTXRQ signal and the delay between the rising edge of TTXRQ and valid teletext input data are fully programmable (TTXHS and TTXHD), the TTX data is always inserted at the correct position after the leading edge of the outgoing horizontal synchronization pulse.

Time $t_{i(TTXW)}$ is the internally used insertion window for TTX data; it has a constant length that allows insertion of 360 teletext bits at a text data rate of 6.9375 Mbits/s (PAL), 296 teletext bits at a text data rate of 5.7272 Mbits/s (world standard TTX) or 288 teletext bits at a text data rate of 5.7272 Mbits/s (NABTS). The insertion window is not opened if the control bit TTXEN is zero.

Using appropriate programming, all suitable lines of the odd field (TTXOVS and TTXOVE) plus all suitable lines of the even field (TTXEVS and TTXEVE) can be used for teletext insertion.

It is essential to note that the two pins used for teletext insertion must be configured for this purpose by the correct I²C-bus register settings.

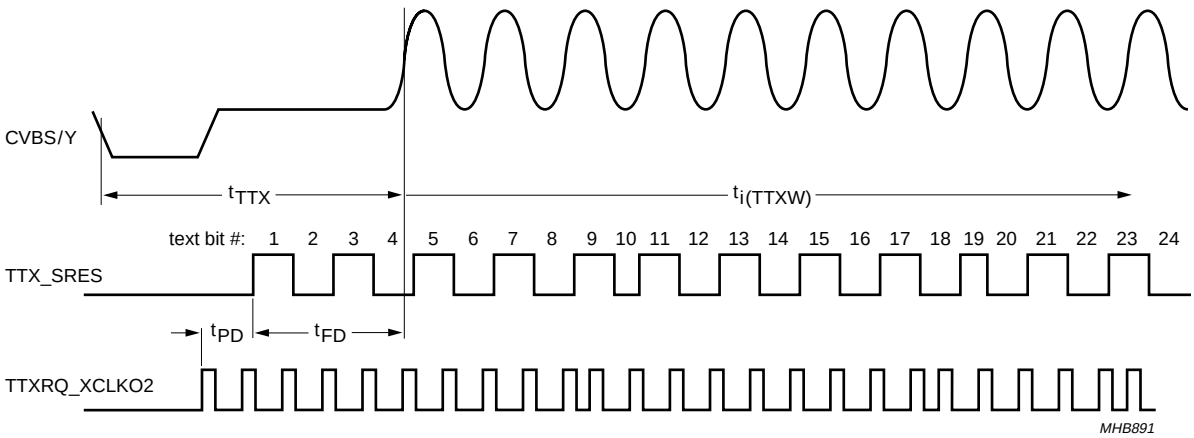


Fig.15 Teletext timing.

12 APPLICATION INFORMATION

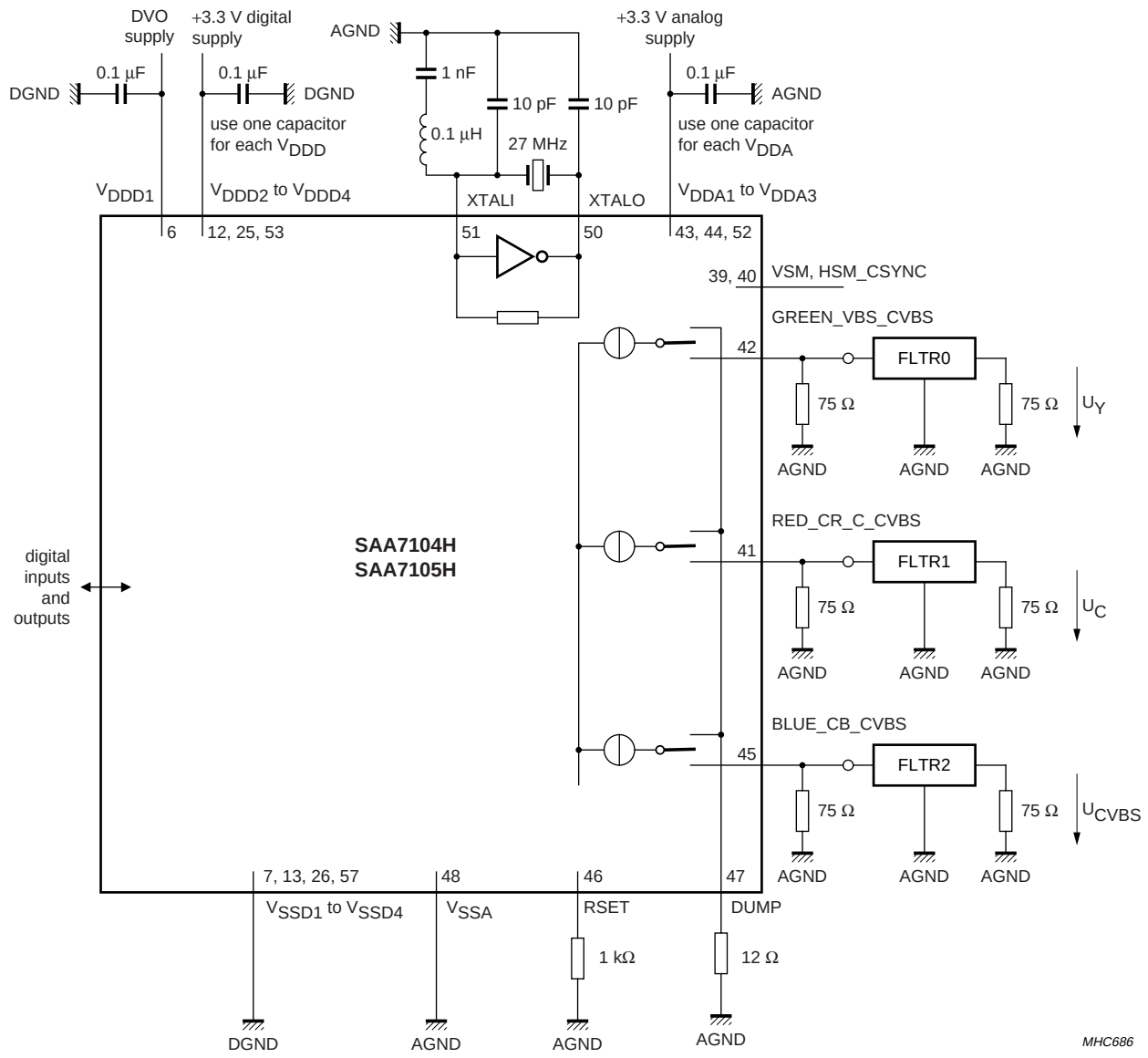


Fig.16 Application circuit.

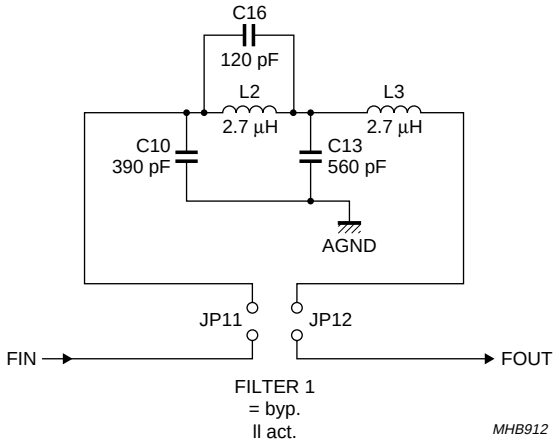
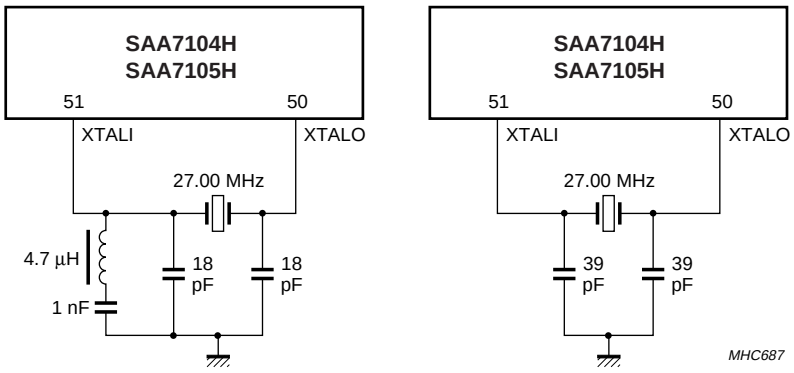
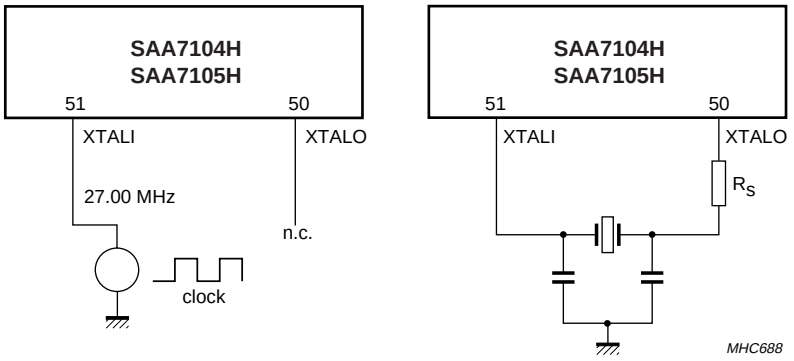


Fig.17 FLTR0, FLTR1 and FLTR2 of Fig.16.



(1a) With 3rd-harmonic quartz. Crystal load = 8 pF.

(1b) With fundamental quartz. Crystal load = 20 pF.



(2a) With direct clock.

(2b) With fundamental quartz and restricted drive level. When P_{drive} of the internal oscillator is too high, a resistance R_S can be placed in series with the oscillator output XTALO.

Note: The decreased crystal amplitude results in a lower drive level but on the other hand the jitter performance will decrease.

Fig.18 Oscillator application.

12.1 Reconstruction filter

Figure 17 shows a possible reconstruction filter for the digital-to-analog converters. Due to its cut-off frequency of ~6 MHz, it is not suitable for HDTV applications.

12.2 Analog output voltages

The analog output voltages are dependent on the total load (typical value 37.5 Ω), the digital gain parameters and the I^2C-bus settings of the DAC reference currents (analog settings).

The digital output signals in front of the DACs under nominal (nominal here stands for the settings given in Tables 40 to 47 for example a standard PAL or NTSC signal) conditions occupy different conversion ranges, as indicated in Table 116 for a $^{100}/_{100}$ colour bar signal.

By setting the reference currents of the DACs as shown in Table 116, standard compliant amplitudes can be achieved for all signal combinations; it is assumed that in subaddress 16H, parameter DACF = 0000b, that means the fine adjustment for all DACs in common is set to 0%.

If S-video output is desired, the adjustment for the C (chrominance subcarrier) output should be identical to the one for VBS (luminance plus sync) output.

Table 116 Digital output signals conversion range

SET/OUT	CVBS, SYNC TIP-TO-WHITE	VBS, SYNC TIP-TO-WHITE	RGB, BLACK-TO-WHITE
Digital settings	see Tables 40 to 47	see Tables 40 to 47	see Table 35
Digital output	1014	881	876
Analog settings	e.g. B DAC = 1FH	e.g. G DAC = 1BH	e.g. R DAC = G DAC = B DAC = 0BH
Analog output	1.23 V (p-p)	1.00 V (p-p)	0.70 V (p-p)

12.3 Suggestions for a board layout

Use separate ground planes for analog and digital ground. Connect these planes only at one point directly under the device, by using a 0 Ω resistor directly at the supply stage. Use separate supply lines for analog and digital supply. Place the supply decoupling capacitors close to the supply pins.

Use L_{bead} (ferrite coil) in each digital supply line close to the decoupling capacitors to minimize radiation energy (EMC).

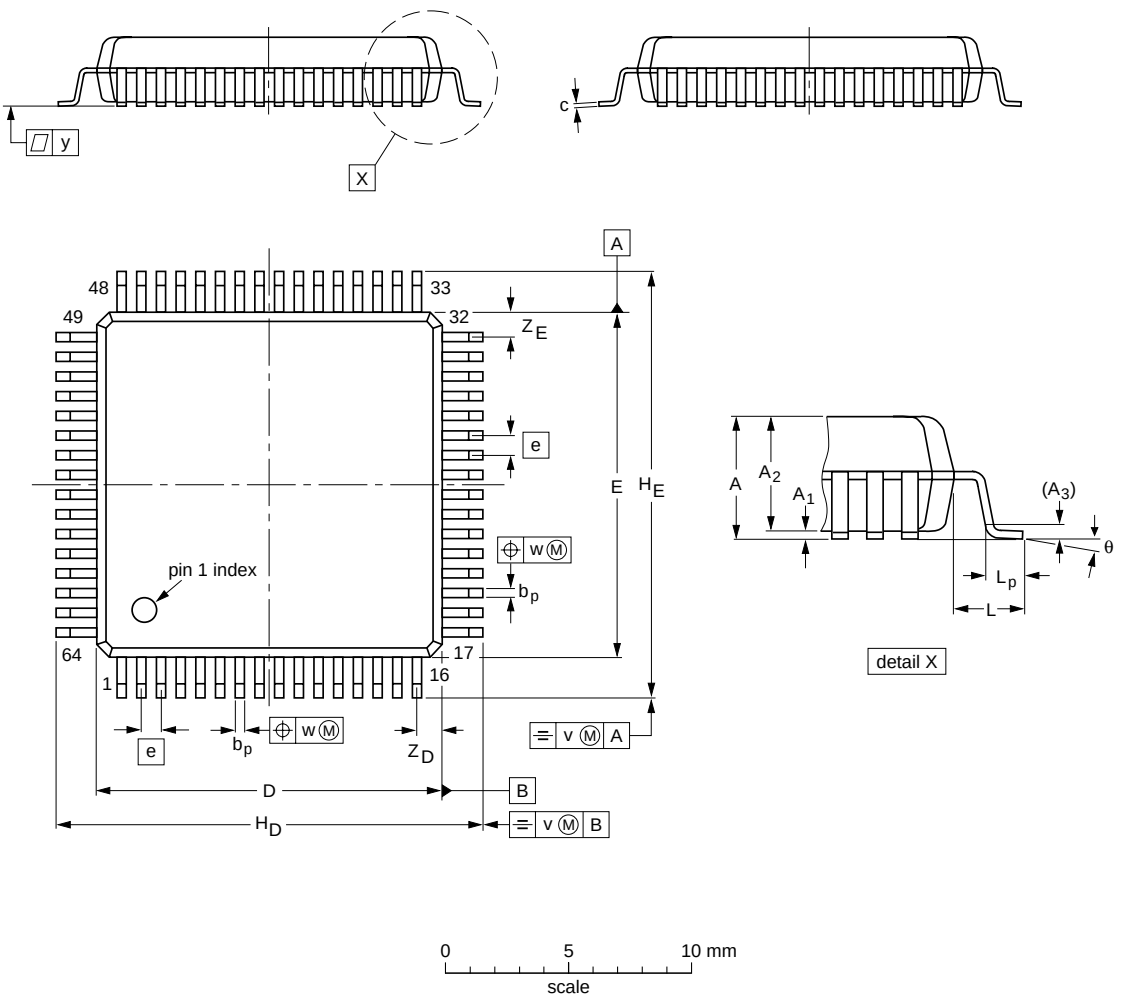
Place the analog coupling (clamp) capacitors close to the analog input pins. Place the analog termination resistors close to the coupling capacitors.

Be careful of hidden layout capacitors around the crystal application.

Use serial resistors in clock, sync and data lines, to avoid clock or data reflection effects and to soften data energy.

13 PACKAGE OUTLINE

QFP64: plastic quad flat package; 64 leads (lead length 1.6 mm); body 14 x 14 x 2.7 mm **SOT393-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3	0.25 0.10	2.75 2.55	0.25	0.45 0.30	0.23 0.13	14.1 13.9	14.1 13.9	0.8	17.45 16.95	17.45 16.95	1.6	1.03 0.73	0.16	0.16	0.1	1.2 0.8	1.2 0.8	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT393-1	134E07	MS-022				~~00-01-19~~ 03-02-20

14 SOLDERING

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON-T and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
8. Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
9. Hot bar or manual soldering is suitable for PMFP packages.

15 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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