LIGHT EMITTING DIODE DRIVER

FEATURES

- Drives 24 LED's under control of Serial Interface
- Light Emitting Diode intensity programmable using a single resistor
- Automatic lamp test facility on reset ($\overline{MRST}$)
- Minimal external components
- LED intensity constant, regardless of number of LED's illuminated
- 11 Bit Information word controls up to 192 LED's (using eight SA8803s)
- Readback of LED status
- Requires a local clock of 8 times the data rate
- Constant current from power supply option

DESCRIPTION

The block Diagram of the SA8803 is shown in Fig. 1. A control word is clocked into the device via the DATA pin with a local clock provided to pin CLK. The control word comprises a 3-bit chip address, a 5-bit LED address and a Status (on/off) bit. Provided that the Chip Adress matches the setting on pins AD0..AD2 then the LED State Register is addressed and the state of the selected LED is set according to the Status bit in the Control word.

The LEDs are driven by banks of Constant Current Sources in which the value of the current in all six banks is set by a single external resistor connected between pin INTENS and VEE. The total current drained by the device and the LEDs may be fixed at six times the LED current by connecting pin CC to GND.

The status of all LEDs can be verified at any time by pulling the TEST pin low. When tis happens the contents of the LED Status Register are clocked out of the SA8803 on the pin DOUT. An additional test feature is that al LEDs are illuminated for a short period after power up to simplify system testing.

PIN CONNECTIONS

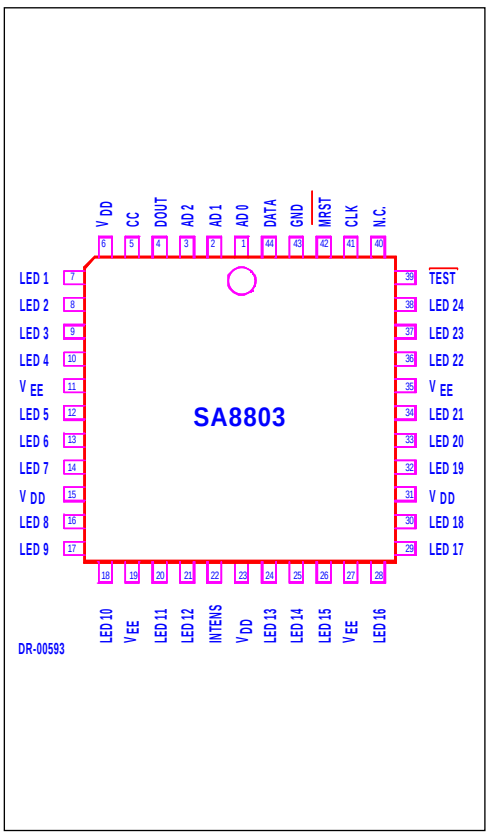
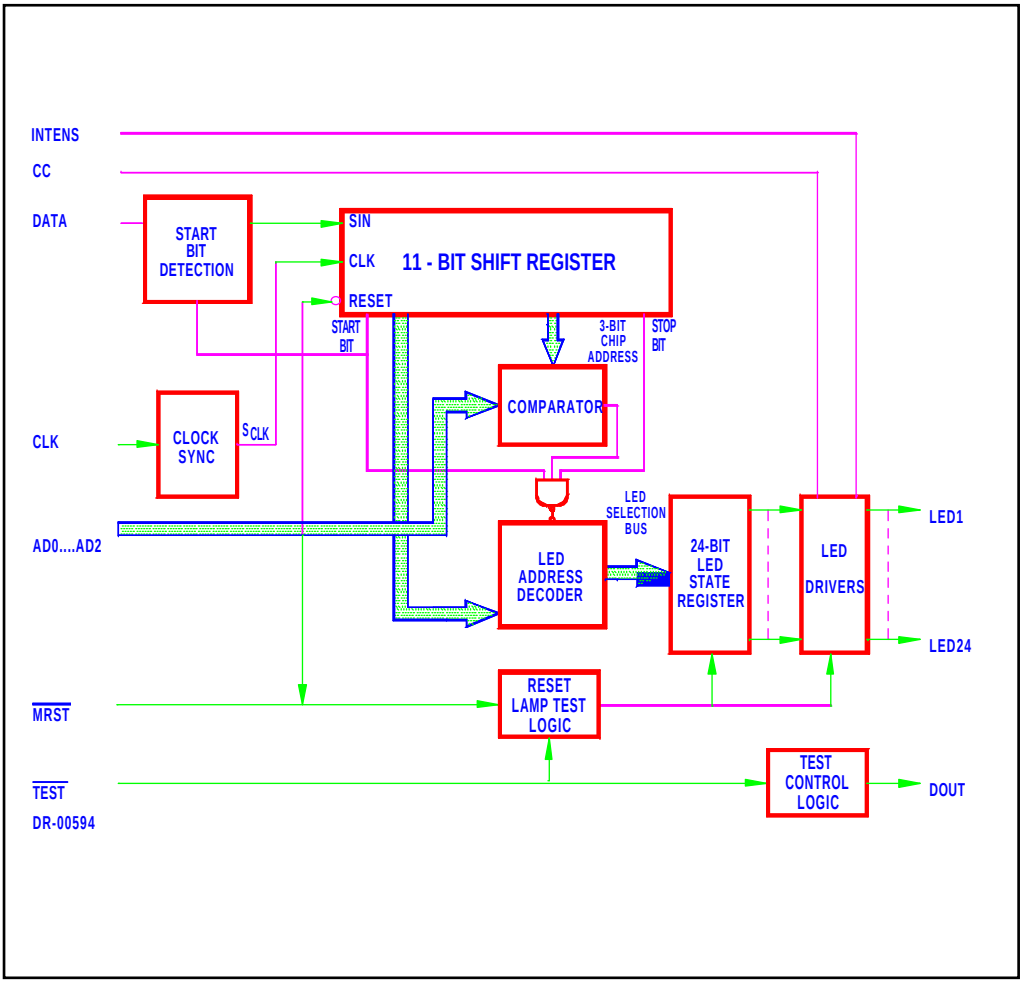


FIGURE 1: BLOCK DIAGRAM



PIN DESCRIPTION

Pin	Designation	Description
1..3	AD0..AD2	Device address input pins. The binary code set up on these pins, must match the address field of the control word, before device access may be achieved. These Schmitt-triggered inputs have on-chip pull-up resistors.
4	DOUT	This output is used for the manufacturers test requirements and MUST be left open.
5	CC	Constant Current Drain Select.This Schmitt-triggered input has on-chip pullup provided.
7..10, 12..14, 16..18, 20..21, 24..26 28..30 32..34, 36..38	LED1..LED4, LED5..LED7 LED8..LED10, LED11..LED12, LED13..LED15, LED16..LED18, LED19..LED21, LED22..LED24	High current LED drive terminal outputs.
22	INTENS	This analog input is used to set the drive current supplied to the LED's. A resistor is connected from this pin to V_{EE}.
39	$\overline{\text{TEST}}$	Active low input that enables the internal LED status word to be output from the DOUT pin. This Schmitt-triggered input has on-chip pullup provided.
40	NC	Internally Unconnected.
41	CLK	External clock Schmitt-triggered input runs at 8X the data rate (Baud rate).
42	$\overline{\text{MRST}}$	This active low Schmitt-Trigger input may be used to reset all internal registers. When active (low) this input will cause all LED's to be driven for the duration of $\overline{\text{MRST}}$ (lamp test). When $\overline{\text{MRST}}$ goes inactive all LED's will be turned off. On-chip pullup provided.
43	GND	0V Supply Input for logic (0V)
44	DATA	Serial data input. Accept data in the form of an 11-bit information word. This Schmitt-triggered input has on-chip pullup provided.
11, 19, 27, 35	VEE	Negative Supply Inputs (-5V)
6, 15, 23, 31	VDD	Positive Supply Inputs (+5V)

Note: All inputs and outputs are CMOS compatible, unless otherwise specified.

FUNCTIONAL DESCRIPTION

1. Control Word

The control word written serially into the DATA pin, will contain 9 information bits.

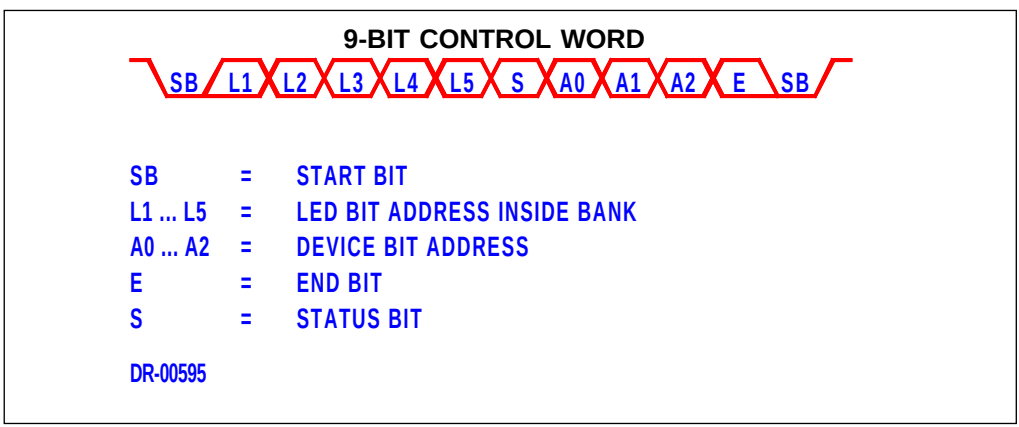
The data structure is illustrated in Figure 2 below.

Because the chip address is 3 bits wide, a single chip controller will be able to address 8 SA8803 devices. Each SA8803 can drive 24 LED's, which means that the controller is capable of addressing 192 LED's. The address bits in the control word are internally compared with the address on the AD0..AD2 address lines to determine if the SA8803 is being addressed.

Table 1. LED Addresses

L5	L4	L3	L2	L1	LED
0	0	0	0	0	IGNORED
0	0	0	0	1	1
0	0	0	1	0	2
		etc			
1	1	0	0	0	24
1 ⋮ 1	1 ⋮ 1	0 ⋮ 1	0 ⋮ 1	1 ⋮ 1	IGNORED

FIGURE 2: CONTROL WORD STRUCTURE



As can be seen from the structure of the control word, the controller should send 1 start bit, 9 data bits, and 1 stop bit.

When a LED is addressed its state will be set according to the status bit. A logic one will enable the LED, and a logic zero will disable the LED.

3. LED Intensity Control

The LED "on" current (I_D), is determined by the current flowing from the INTENS pin through the external resistor. The values of I_D can be calculated as follows:

$$I_D = K_T . \frac{V_X}{R}$$

K_T - Current Transfer Ratio of the Internal Current Mirror (typically 10.0)

R - The programming resistor value

V_X - The voltage drop across the external resistor (internally controlled to 5.0V)

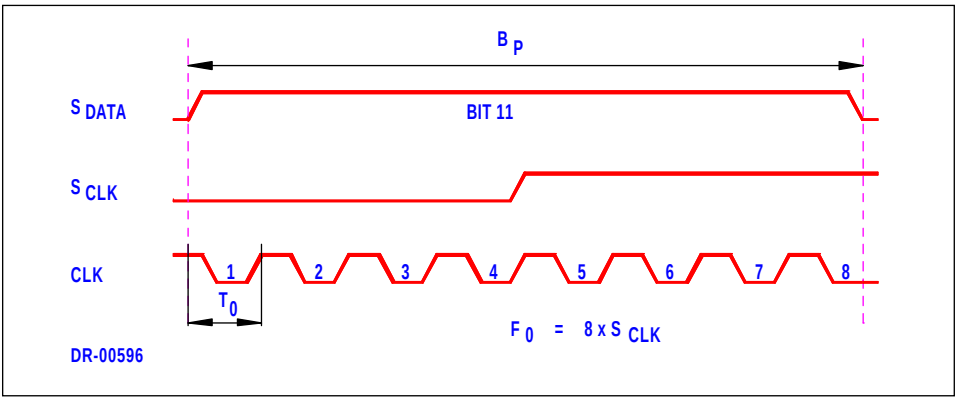
4. Constant Current Mode

When the CC pin is pulled high, the device will draw a constant current from the V_{DD} supply which is equal to all LED's in the "on"condition regardless of the status of the LED's.

5. Clock Characteristics

S_{CLK} is the internal synchronous clock derived from the asynchronous external clock applied at the CLK input pin. It divides the external clock by 8. Theoretically the rising edge of S_{CLK} (synchronous Clock) should be in the middle of every bit, as shown in Figure 4. Because of phase shift due to the clock frequency being more or less than 8 times the baud rate, this edge may shift its position with regard to the bit period (B_P). The extreme case that may still be tolerated is an edge arriving at either the beginning, or end of bit 11. This represents the maximum shift that can be tolerated for valid data to be received for an inaccurate input clock frequency (F_O).

FIGURE 3: TIMING DIAGRAM



The acceptable Clock pulse Period (T_O) may be calculated as follows:

The rising edge may not shift more than half a bit period (B_P), therefore:

$$11 \times B_P - (½ \times B_P) < 11 \times 8 \times T_O < 11 \times B_P (½ \times B_P)$$

Therefore:

$$11 \times 8 \times T_O = 11 \times B_P \pm (½ \times B_P)$$

$$\therefore \quad T_O = (B_P \div 8) \pm \frac{(B_P \div 8)}{22}$$

$$\therefore \quad T_O = (B_P \div 8) \pm 4{,}55\%$$

The acceptable frequency for the clock F_O is calculated as follows:

$$F_O = \frac{1}{T_O}$$

$$\therefore F_O = \frac{1}{(B_P \div 8)\left(1 \pm \frac{1}{22}\right)}$$

But because:

$$B_R \times 8 = \frac{1}{(B_P \div 8)}$$

where B_R = Baud Rate

$$F_O = (B_R \times 8) \times \frac{22}{(1 \pm 22)}$$

$$\therefore \quad F_O = B_R \times 8 \pm 4.55\%$$

The SA8803 has been specified for an external clock frequency of 8 times the Baud Rate ± 3%.

6. Test feature

If the $\overline{\text{TEST}}$ pin is pulled low, the status of all 24 LED's are output at pin DOUT in 3 groups of 8 status bits each, with a start bit and a stop bit added. The data rate of this status word is equal to the input data rate (i.e. CLK) devided by 8.

The three data word that are serially output at DOUT each contain 11-bit. This means that bit 10 is not used in each case. The words therefore contain a start bit, 8 LED status bits (1 for off, 0 for on). 1 unused bit, and a stop bit. The three groups are output consecutively in the following order: first LED's 1 to 8, then 9 to 16, and then 17 to 24.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	-0.30 V to +5.50 V
Supply Voltage, V_{EE}	0.30 V to -5.50 V
Input or Output Voltage	-0.30 V to (V_{DD} +0.30) V
DC Forward Bias Current, Input or Output	± 10 mA
Storage Temperature (Plastic)	-40 to 125°C
Operating Temperature	0° - 70°

Note 1: Referenced to GND. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect the device reliability.

ELECTRICAL CHARACTERISTICS

DC Electrical Characteristics Across Temperature Range (Note 1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
TTL INTERFACE						
V_{IL}	Low Level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{OL}	Low Level Ouput Voltage	$I_{OL} \leq 4mA$		0.1	0.4	V
V_{OH}	High Level Output Voltage	$I_{OH} \leq 4$ mA	2.4	4.5		V

Symbol	Parameter	Condition	Min	Typ	Max	Unit
CMOS INTERFACE						
V_{IL}	Low Level Input Voltage				1.5	V
V_{IH}	High Level Input Voltage		3.5			V
V_{OL}	Low Level Output Voltage	$I_O \leq \pm 4$ mA			1.0	V
V_{OH}	High Level Output Voltage	$I_O \leq \pm 4$ mA	V_{DD} -1.0			V
V_{T+}	Schmitt. Trig. +ve Threshold			3.4	4.0	V
V_{T-}	Schmitt. Trig. -ve Threshold		1.4	2.0		V
GENERAL						
I_{IL}	Low Level Input Current	$V_I = V_{SS}$	-10	<1	10	µA
I_{IH}	High Level Input Current	$V_I = V_{DD}$	-10	<1	10	µA
I_{ILU}	Input Current with Pull Up	$V_I = V_{SS}$	-200	-50	-10	µA
I_{IHD}	Input Current with Pull Down	$V_I = V_{DD}$	10	50	200	µA
I_{OZ}	Tri-state Output Leakage	$V_O = O_V$ or V_{DD}	-10	<1	10	µA
V_{ESD}	Electrostatic Protection	C = 100pF R = 1.5Kohm	2000			V
V_{DD}	Logic Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Analog Supply Voltage		-5.5	-5.0	-4.5	V
K_T	Current Transfer Ratio			10.5		
ΔK_T	Delta Current Transfer Ratio	$I_D = 10$ mA			± 15	%
I_D	LED Current	Programmed Value			10	mA
F_O	Operating Frequency [1]	Must be ± 3% of 8 x Baud Rate	0.4	128	448	kHz

NOTE 1) The operating frequency range for F_O is wide enough to cover baud rates from 50 to 56000 bps.

NOTES:

South African Micro-Electronic Systems (Pty) Ltd

P O Box 15888,
Lynn East,
0039
Republic of South Africa,

33 Eland Street,
Koedoespoort Industrial Area,
Pretoria,
Republic of South Africa

Tel: 012 333-6021
Fax: 012 333-8071

Tel: Int +27 12 333-6021
Fax: Int +27 12 333-8071