MITEL
SEMICONDUCTOR

SA828 Family
Three-Phase PWM Waveform Generator

DS4226 - 2.0 November 1996

The SA828 PWM generator has been designed to provide waveforms for the control of variable speed AC machines, uninterruptible power supplies and other forms of power electronic devices which require pulse width modulation as a means of efficient power control.

The six TTL level PWM outputs (Fig. 2) control the six switches in a three-phase inverter bridge. This is usually via an external isolation and amplification stage.

The SA828 is fabricated in CMOS for low power consumption.

Information contained within the pulse width modulated sequences controls the shape, power frequency, amplitude, and rotational direction (as defined by the red-yellow-blue phase sequence) of the output waveform. Parameters such as the carrier frequency, minimum pulse width, and pulse delay time may be defined during the initialisation of the device. The pulse delay time (underlap) controls the delay between turning on and off the two power switches in each output phase of the inverter bridge, in order to accommodate variations in the turn-on and turn-off times of families of power devices.

The SA828 is easily controlled by a microprocessor and its fully-digital generation of PWM waveforms gives unprecedented accuracy and temperature stability. Precision pulse shaping capability allows optimum efficiency with any power circuitry. The device operates as a stand-alone microprocessor peripheral, reading the power waveform directly from an internal ROM and requiring microprocessor intervention only when operating parameters need to be changed.

An 8-bit multiplexed data bus is used to receive addresses and data from the microprocessor/controller. This is a standard MOTEL™ bus, compatible with most microprocessors/controllers.

Rotational frequency is defined to 12 bits for high accuracy and a zero setting is included in order to implement DC injection braking with no software overhead.

This family is pin and functionally compatible with the MA828 PWM generator . Two standard wave shapes are available to cover most applications. In addition, any symmetrical wave shape can be integrated on-chip to order.

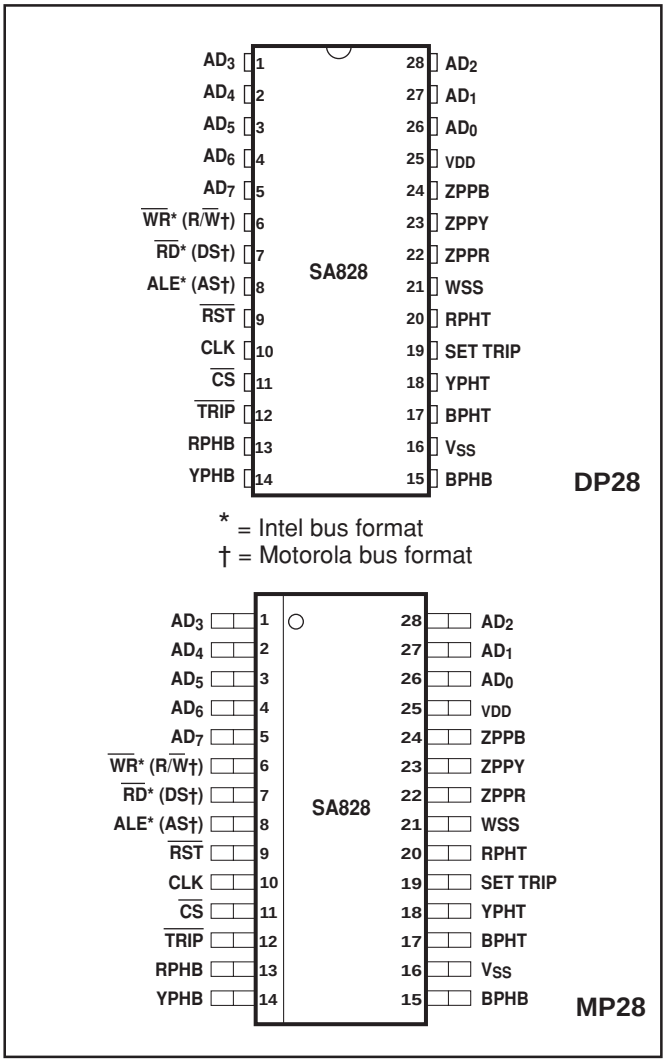


Fig. 1 Pin connections – top view (not to scale)

FEATURES

- Fully Digital Operation
- Interfaces with Most Microprocessors
- Wide Power-Frequency Range
- 12-Bit Speed Control Accuracy
- Carrier Frequency Selectable up to 24kHz
- Waveform Stored in Internal ROM
- Double Edged Regular Sampling
- Selectable Minimum Pulse Width and Underlap Time
- DC Injection Braking

ORDERING INFORMATION

SA8281/IG/DP1S (28-lead DIL, sine + third harmonic waveform)

SA8282/IG/DP1S (28-lead DIL, sine waveform)

SA8281/IG/MP1S (28-lead SOIC, Sine + third harmonic waveform)

SA8382/IG/MP1S (28-lead SOIC, sine waveform)

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ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

V_{DD} = +5V ±5%, T_{AMB} = +25°C

DC Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Input high voltage	V_{IH}	2			V	
Input low voltage	V_{IL}			0·8	V	
Input leakage current	I_{IN}			10	µA	$V_{IN} = V_{SS}$ or V_{DD}
Output high voltage	V_{OH}	4·0	>4·5		V	I_{OH} = – 12mA
Output low voltage	V_{OL}		<0·2	0·4	V	I_{OL} = 12mA
Supply current (static)	$I_{DD\ (static)}$			100	µA	All outputs open circuit
Supply current (dynamic)	$I_{DD\ (dynamic)}$		<10	20	mA	f_{CLK} = 10MHz
Supply voltage	V_{DD}	4·5	5·0	5·5	V	

AC Characteristics

Characteristic	Symbol	Value			Units	Conditions
			Typ.	Max.		
Clock frequency	f_{CLK}			12·5	MHz	M : S ratio = 1 : 1 ±20%
Clock duty cycle	D_{CLK}	40	-	60	%	
SET TRIP = 1 → outputs tripped	t_{TRIP}		$2/f_{CLK}$	$3/f_{CLK}$	µs	f_{CLK} in MHz
→$\overline{TRIP}$ = 0			$2/f_{CLK}$	$3/f_{CLK}$	µs	f_{CLK} in MHz

NOTE 1. For microprocessor interface timings, see Intel and Motorola bus timings (Tables 1 and 2).

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	7V
Voltage on any pin	V_{SS} –0·3V to V_{DD} +0·3V
Current through any I/O pin	±10mA
Storage temperature	–65°C to +125°C
Operating temperature range	–40°C to +85°C

The temperature ranges quoted apply to all package types. Many package types are available and extended temperature ranges can be offered for some. Further information is available on request.

Stresses above those listed in the Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

PIN DESCRIPTIONS

Pin No.	Name	Type	Function	Pin No.	Name	Type	Function
1	AD_3	I	Multiplexed Address/Data	13	RPHB	O	Red Phase, Bottom power switch
2	AD_4	I	Multiplexed Address/Data	14	YPHB	O	Yellow Phase, Bottom power switch
3	AD_5	I	Multiplexed Address/Data	15	BPHB	O	Blue Phase, Bottom power switch
4	AD_6	I	Multiplexed Address/Data	16	V_{SS}	P	Negative power supply (0V)
5	AD_7	I	Multiplexed Address/Data(MSB)	17	BPHT	O	Blue Phase, Top power switch
6	Intel: $\overline{WR}$ Motorola: R/$\overline{W}$	I	Intel bus control: $\overline{Write}$ Strobe Motorola bus control: Read/$\overline{Write}$ select	18	YPHT	O	Yellow Phase, Top power switch
				19	SET TRIP	I	Set output trip. 120kΩ internal pull-up resistor
7	Intel: $\overline{RD}$ Motorola: DS	I	Intel bus control: $\overline{Read}$ Strobe Motorola bus control: Data Strobe	20	RPHT	O	Red Phase, Top power switch
				21	WSS	O	Waveform Sampling Synchronisation
8	Intel: ALE Motorola: AS	I	Intel bus control: Address Latch Enable Motorola bus control: Address Strobe	22	ZPPR	O	Zero Phase Pulse, Red phase
				23	ZPPY	O	Zero Phase Pulse, Yellow phase
				24	ZPPB	O	Zero Phase Pulse, Blue phase
9	$\overline{RST}$	I	Reset internal counters, active low	25	V_{DD}	P	Positive power supply
10	CLK	I	Clock input	26	AD_0	I	Multiplexed Address/Data (LSB)
11	$\overline{CS}$	I	Chip Select input, active low	27	AD_1	I	Multiplexed Address/Data
12	$\overline{TRIP}$	O	Output trip status; low = output tripped	28	AD_2	I	Multiplexed Address/Data

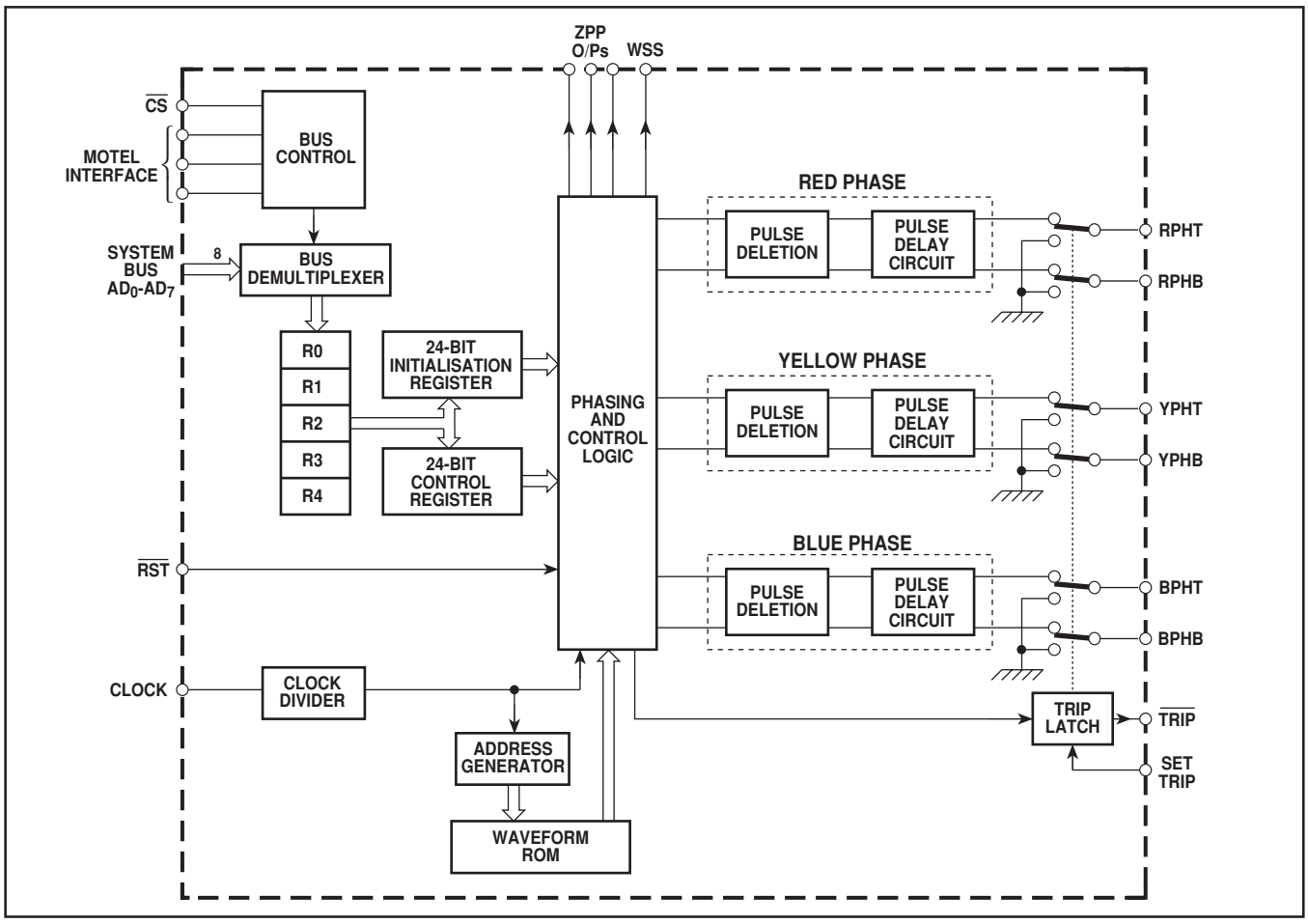


Fig. 2 SA828 internal block diagram

FUNCTIONAL DESCRIPTION

An asynchronous method of PWM generation is used with uniform or 'double-edged' regular sampling of the waveform stored in the internal ROM as illustrated in Fig. 3.

The triangle carrier wave frequency is selectable up to 24kHz (assuming the maximum clock frequency of 12.5MHz is used), enabling ultrasonic operation for noise critical applications. With 12.5MHz clock, power frequency ranges of up to 4kHz are possible, with the actual output frequency resolved to 12-bit accuracy within the chosen range in order to give precise motor speed control and smooth frequency changing. The output phase sequence of the PWM outputs can also be changed to allow both forward and reverse motor operation.

PWM output pulses can be 'tailored' to the inverter characteristics by defining the minimum allowable pulse width (the SA828 will delete all shorter pulses from the 'pure' PWM pulse train) and the pulse delay (underlap) time, without the need for external circuitry. This gives cost advantages in both component savings and in allowing the same PWM circuitry to be used for control of a number of different motor drive circuits simply by changing the microprocessor software.

Power frequency amplitude control is also provided with an overmodulation option to assist in rapid motor braking. Alternatively, braking may be implemented by setting the rotational speed to 0Hz. This is termed 'DC injection braking', in which the rotation of the motor is opposed by allowing DC to flow in the windings.

A trip input allows the PWM outputs to be shut down immediately, overriding the microprocessor control in the event of an emergency.

The Waveform Sampling Synchronisation (WSS) output may be used in conjunction with the ZPP signals to provide feedback of the actual rotational speed from the rotor. This is of particular use in slip compensated systems.

Other possible SA828 applications are as a 3-phase waveform generator as part of a switched-mode power supply (SMPS) or of an uninterruptible power supply (UPS). In such applications the high carrier frequency allows a very small switching transformer to be used.

MICROPROCESSOR INTERFACE

The SA828 interfaces to the controlling microprocessor by means of a multiplexed bus of the MOTEL format. This interface bus has the ability to adapt itself automatically to the format and timing of both MOTorola and IntEL interface buses (hence MOTEL). Internally, the detection circuitry latches the status of the DS/$\overline{RD}$ line when AS/ALE goes high. If the result is high then the Intel mode is used; if the result is low then the Motorola mode is used. This procedure is carried out each time that AS/ALE goes high. In practice this mode selection is transparent to the user. For bus connection and timing information refer to the description relevant to the microprocessor/controller being used.

Industry standard microprocessors such as the 8085, 8088, etc. and microcontrollers such as the 8051, 8052 and 6805 are all compatible with the interface on the SA828. This interface consists of 8 data lines, AD_0 - AD_7 (write-only in this instance), which are multiplexed to carry both the address and data information, 3 bus control lines, labelled $\overline{WR}$,$\overline{RD}$ and ALE in Intel mode and R/$\overline{W}$, DS and AS in Motorola mode, and a Chip Select input, $\overline{CS}$, which allows the SA828 to share the same bus as other microprocessor peripherals. It should be noted that all bus timings are derived from the microprocessor and are independent of the SA828 clock input.

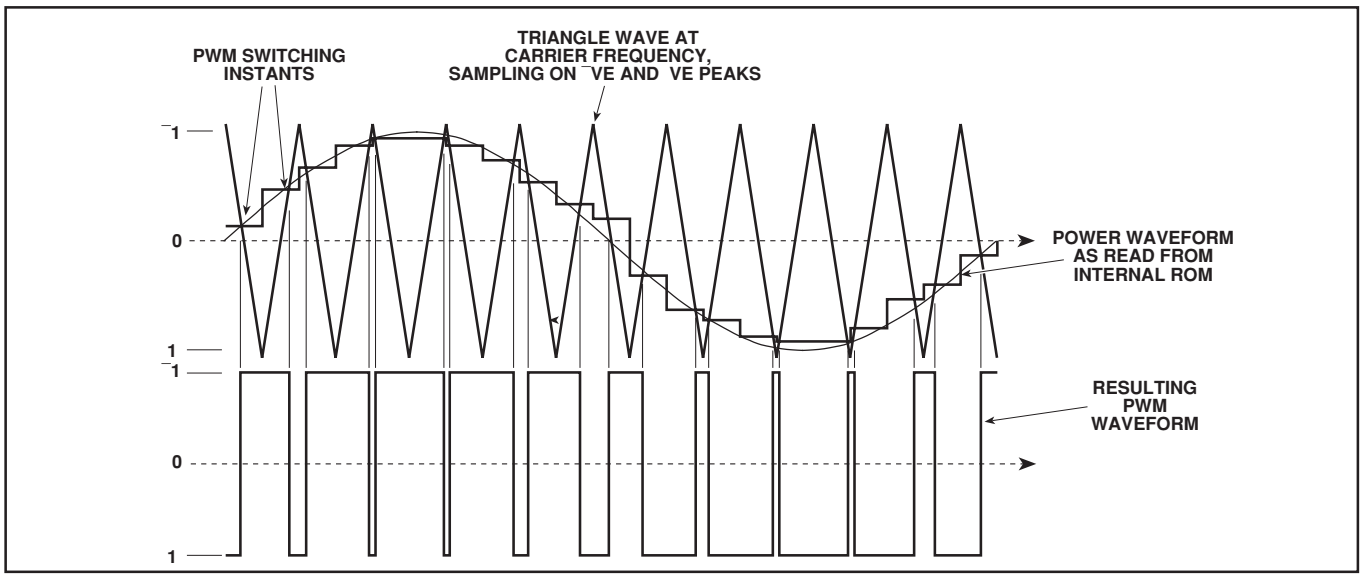


Fig. 3 Asynchronous PWM generation with'double-edged' regular sampling as used by the SA828

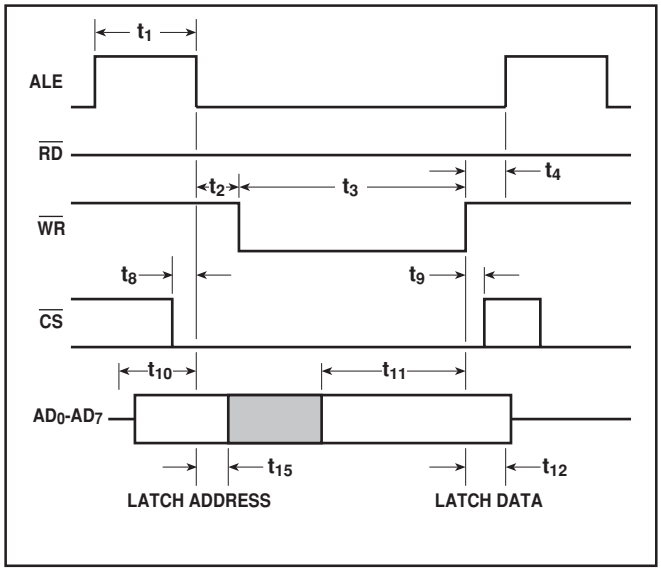


Fig. 4 Intel bus timing definitions

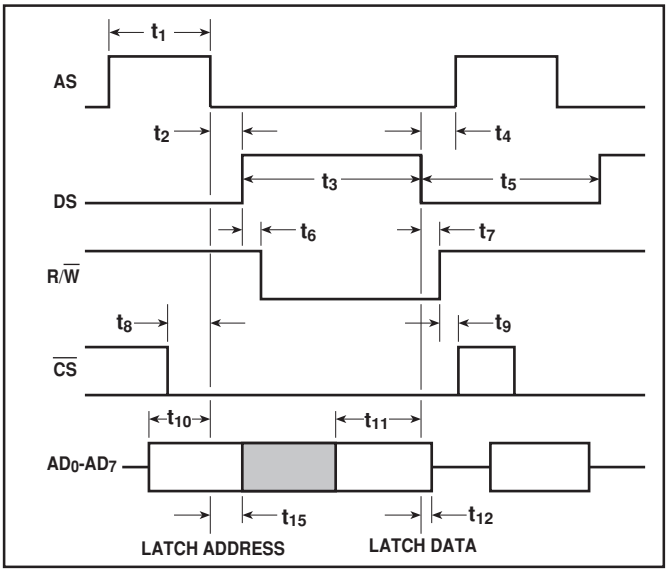


Fig. 5 Motorola bus timing definitions

Parameter	Symbol	Min.	Units
ALE high period	t_1	70	ns
Delay time, ALE to $\overline{WR}$	t_2	40	ns
$\overline{WR}$ low period	t_3	200	ns
Delay time, $\overline{WR}$ high to ALE high	t_4	40	ns
$\overline{CS}$ setup time	t_8	20	ns
$\overline{CS}$ hold time	t_9	0	ns
Address setup time	t_{10}	30	ns
Address hold time	t_{15}	30	ns
Data setup time	t_{11}	100	ns
Data hold time	t_{12}	25	ns

Table 1 Intel bus timings at V_{DD} = 5V, T_{AMB} = +25°C

Parameter	Symbol	Min.	Units
AS high period	t_1	90	ns
Delay time, as low to DS high	t_2	40	ns
DS high period	t_3	210	ns
Delay time, DS low to AS high	t_4	40	ns
DS low period	t_5	200	ns
DS high to R/$\overline{W}$ low setup time	t_6	10	ns
R/$\overline{W}$ hold time	t_7	10	ns
$\overline{CS}$ setup time	t_8	20	ns
$\overline{CS}$ hold time	t_9	0	ns
Address setup time	t_{10}	30	ns
Address hold time	t_{15}	30	ns
Write data setup time	t_{11}	110	ns
Write data hold time	t_{12}	30	ns

Table 2 Motorola bus timings at V_{DD} = 5V, T_{AMB} = +25°C

MICROPROCESSOR BUS TIMING

Intel Mode (Fig. 4 and Table 1)

The address is latched by the falling edge of ALE. Data is written from the bus into the SA828 on the rising edge of $\overline{WR}$. $\overline{RD}$ is not used in this mode because the registers in the SA828 are write only. However, this pin must be connected to $\overline{RD}$ (or tied high) to enable the SA828 to select the correct interface format.

Motorola Mode (Fig. 5 and Table 2)

The address is latched on the falling edge of the AS line. Data is written from the bus into the SA828 (only when R/$\overline{W}$ is low) on the falling edge of DS (providing $\overline{CS}$ is low).

CONTROLLING THE SA828

The SA828 is controlled by loading data into two 24-bit registers via the microprocessor interface. These registers are the initialisation register and the control register.

The initialisation register would normally be loaded before motor operation (i.e., prior to the PWM outputs being activated) and sets up the basic operating parameters associated with the motor and inverter. This data would not normally be updated during motor operation.

The control register is used to control the PWM outputs (and hence the motor) during operation e.g., stop/start, speed, forward/reverse etc. and would normally be loaded and changed only after the initialisation register has been loaded.

As the MOTEL bus interface is restricted to an 8-bit wide format, data to be loaded into either of the 24-bit registers is first written to three 8-bit temporary registers R0, R1 and R2 before being transferred to the desired 24-bit register. The data is accepted (and acted upon) only when transferred to one of the 24-bit registers.

Transfer of data from the temporary registers to either the initialisation register or the control register is achieved by a write instruction to a dummy register. Writing to dummy register R3 results in data transfer from R0, R1 and R2 to the control register, while writing to dummy register R4 transfers data from R0, R1 and R2 to the initialisation register. It does not matter what data is written to the dummy registers R3 and R4 as they are not real registers. It is merely the write instruction to either of these registers which is acted upon in order to load the initialisation and control registers.

AD_2	AD_1	AD_0	Register	Comment
0	0	0	R0	Temporary register R0
0	0	1	R1	Temporary register R1
0	1	0	R2	Temporary register R2
0	1	1	R3	Transfers control data
1	0	0	R4	Transfers initialisation data

Table 3 SA828 register addressing

Initialisation Register Function

The 24-bit initialisation register contains parameters which, under normal operation, will be defined during the power-up sequence. These parameters are particular to the drive circuitry used, and therefore changing these parameters during a PWM cycle is not recommended. Information in this register should only be modified while $\overline{RST}$ is active (i.e. low) so that the PWM outputs are inhibited (low) during the updating process.

The parameters set in the initialisation register are as follows:

Carrier frequency

Low carrier frequencies reduce switching losses whereas high carrier frequencies increase waveform resolution and can allow ultrasonic operation.

Power frequency range

This sets the maximum power frequency that can be carried within the PWM output waveforms. This would normally be set to a value to prevent the motor system being operated outside its design parameters.

Pulse delay time ('underlap')

For each phase of the PWM cycle there are two control signals, one for the top switch connected to the positive inverter DC supply and one for the bottom switch connected to the negative inverter DC supply. In theory, the states of these two switches are always complementary. However, due to the finite and non-equal turn-on and turn- off times of power devices, it is desirable when changing the state of the output pair, to provide a short delay time during which both outputs are off in order to avoid a short circuit through the switching elements.

Pulse deletion time

A pure PWM sequence produces pulses which can vary in width between 0% and 100% of the duty cycle. Therefore, in theory, pulse widths can become infinitesimally narrow. In practice this causes problems in the power switches due to storage effects and therefore a minimum pulse width time is required. All pulses shorter than the minimum specified are deleted.

Counter reset

This facility allows the internal power frequency counter of the SA828 to be set to zero, disabling the normal frequency control and giving a 50% output duty cycle.

Initialisation Register Programming

The initialisation register data is loaded in 8-bit segments into the three 8-bit temporary registers R0-R2. When all the initialisation data has been loaded into these registers it is transferred into the 24-bit initialisation register by writing to the dummy register R4.

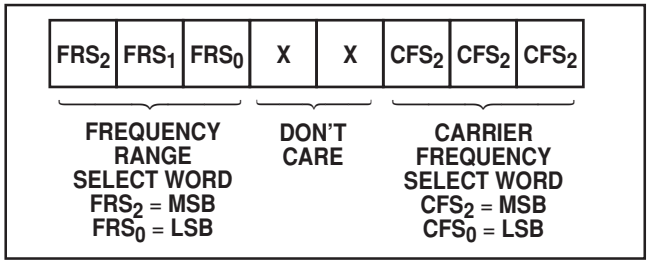


Fig. 6 Temporary register R1

Carrier frequency selection

The carrier frequency is a function of the externally applied clock frequency and a division ratio *n*, determined by the 3-bit CFS word set during initialisation. The values of *n* are selected as shown in Table 4.

CFS word	101	100	011	010	001	000
Value of n	32	16	8	4	2	1

Table 4 Values of clock division ratio n

The carrier frequency, f_{CARR}, is then given by:

$$f_{CARR} = \frac{k}{512 \times n}$$

where k = clock frequency and n = 1, 2, 4, 8, 16 or 32 (as set by CFS)

Power frequency range selection

The power frequency range selected here defines the maximum limit of the power frequency. The operating power frequency is controlled by the 12-bit Power Frequency Select (PFS) word in the control register but may not exceed the value set here.

The power frequency range is a function of the carrier waveform frequency (f_{CARR}) and a multiplication factor *m*, determined by the 3-bit FRS word. The value of *m* is determined as shown in Table 5.

FRS word	110	101	100	011	010	001	000
Value of m	64	32	16	8	4	2	1

Table 5 Values of carrier frequency multiplicaion factor m

The power frequency range, f_{RANGE}, is then given by:

$$f_{RANGE} = \frac{f_{CARR}}{384} \times m$$

where f_{CARR} = carrier frequency and *m* = 1, 2, 4, 8, 16, 32 or 64 (as set by FRS).

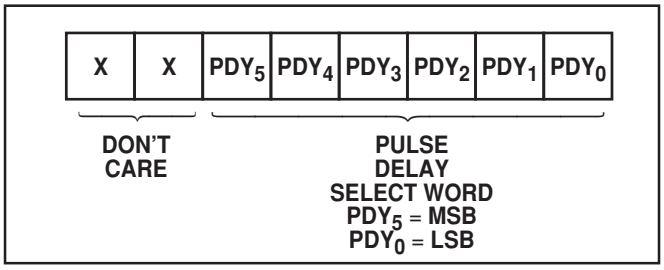


Fig. 7 Temporary register R2

Pulse delay time

The pulse delay time affects all six PWM outputs by delaying the rising edges of each of the outputs by an equal amount.

The pulse delay time is a function of the carrier waveform frequency and *pdy*, defined by the 6-bit pulse delay time select word (PDY). The value of *pdy* is selected as shown in Table 6.

PDY word	111111	111110	...etc...	000000
Value of pdy	1	2	...etc...	64

Table 6 Values of pdy

The pulse delay time, t_{pdy}, is then given by:

$$t_{pdy} = \frac{pdy}{f_{CARR} \times 512}$$

where *pdy* = 1- 64 (as set by PDY) and f_{CARR} = carrier frequency.

Fig 8 shows the eftect of the pulse delay circuit.

It should be noted that as the pulse delay circuit follows the pulse deletion circuit (see Fig. 2), the minimum pulse width seen at the PWM outputs will be shorter than the pulse deletion time set in the initialisation register. The actual shortest pulse generated is given by $t_{pd} - t_{pdy}$.

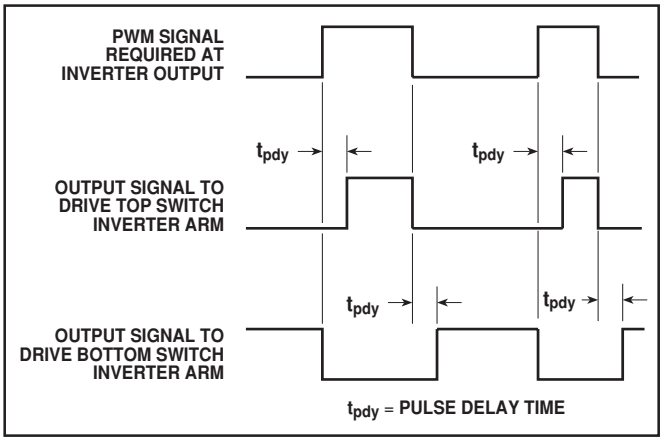


Fig. 8 Effect of pulse delay on PWM pulse train

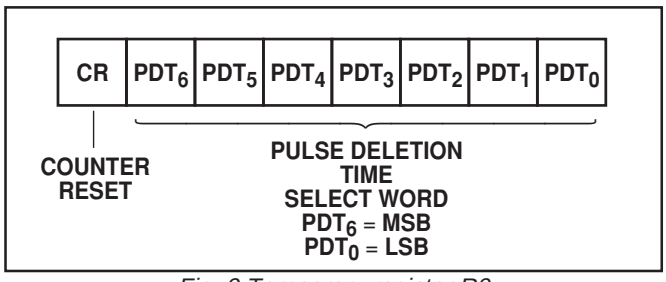


Fig. 9 Temporary register R0

Pulse deletion time

To eliminate short pulses the true PWM pulse train is passed through a pulse deletion circuit. The pulse deletion circuit compares pulse widths with the pulse deletion time set in the initialisation register. If a pulse (either positive or negative) is greater than or equal in duration to the pulse deletion time, it is passed through unaltered, otherwise the pulse is deleted.

The pulse deletion time, t_{pd} , is a function of the carrier wave frequency and *pdt*, defined by the 7-bit pulse deletion time word (PDT). The value of *pdt* is selected as shown in Table 7.

PDT word	1111111	1111110	...etc...	0000000
Value of pdt	1	2	...etc...	128

Table 7 Values of pdt

The pulse deletion time, t_{pd}, is then given by:

$$t_{pd} = \frac{pdt}{f_{CARR} \times 512}$$

where *pdt* = 1-128 (as set by PDT) and f_{CARR} = carrier frequency.

Fig. 10 shows the effect of pulse deletion on a pure PWM waveform.

Counter reset

When the CR bit is active (i.e., low) the internal power frequency phase counter is set to 0 degrees for the red phase. It will remain at 0 degrees until the CR bit is released (i.e., high).

Control Register Function

This 24-bit register contains the parameters that would normally be modified during PWM cycles in order to control the operation of the motor.

The parameters set in the control register are as follows:

Power frequency (speed)

Allows the power frequency of the PWM outputs to be adjusted within the range specified in the initialisation register

Forward/reverse

Allows the direction of rotation of the AC motor to be changed by changing the phase sequence of the PWM outputs.

Power frequency amplitude

By altering the widths of the PWM output pulses while maintaining their relative widths, the amplitude of the power waveform is effectively altered whilst maintaining the same power frequency.

Overmodulation

Allows the output waveform amplitude to be doubled so that a quasi-squarewave is produced. A combination of overmodulation and a lower power frequency can be used to achieve rapid braking in AC motors.

Output inhibit

Allows the outputs to be set to the low state while the PWM generation continues internally. Useful for temporarily inhibiting the outputs without having to to change other register contents.

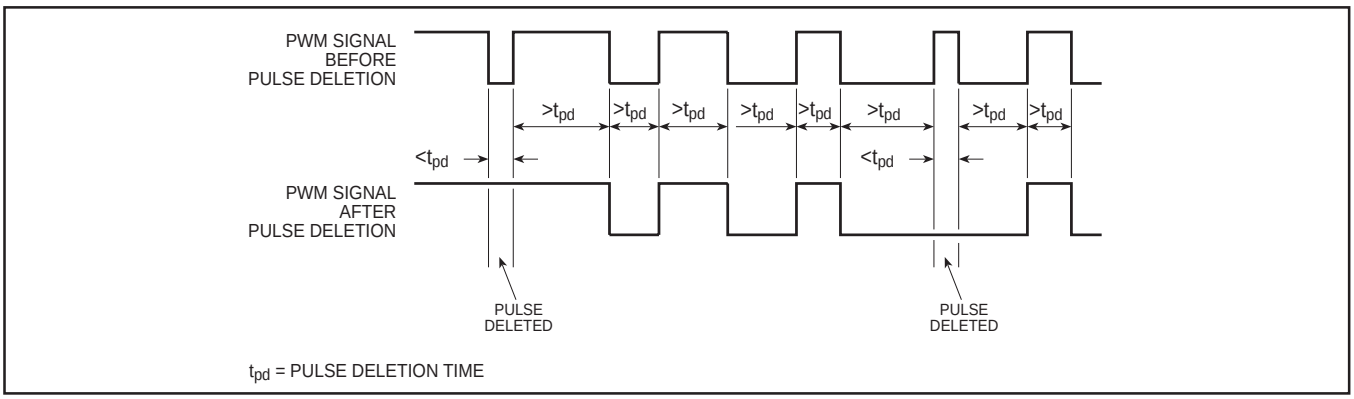


Fig. 10 The effect of the pulse deletion circuit

Control Register Programming

The control register should only be programmed once the initialisation register contains the basic operating parameters of the SA828.

As with the initialisation register, control register data is loaded into the three 8-bit temporary registers R0 - R2. When all the data has been loaded into these registers it is transferred into the 24-bit control register by writing to the dummy register R3. It is recommended that all three temporary registers are updated before writing to R3 in order to ensure that a conformal set of data is transferred to the control register for execution.

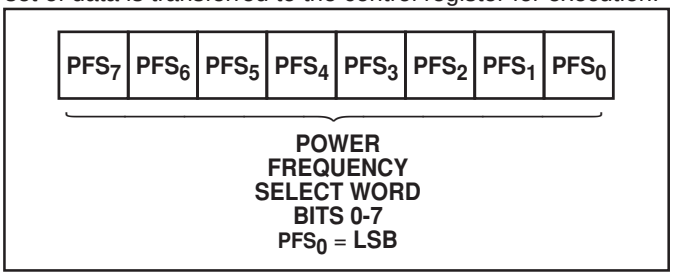


Fig. 11 Temporary register R0

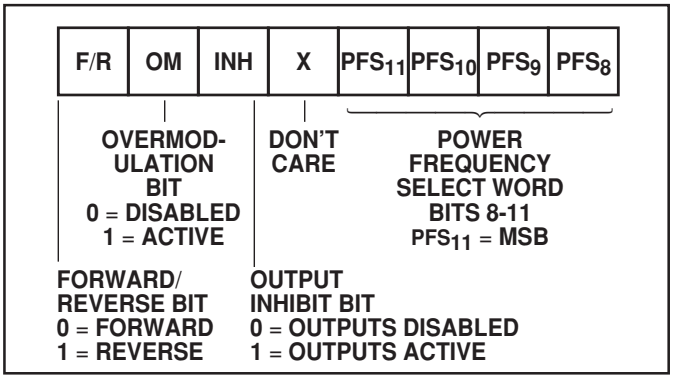


Fig. 12 Temporary register R1

Power frequency selection

The power frequency is selected as a proportion of the power frequency range (defined in the initialisation register) by the 12-bit power frequency select word, PFS, allowing the power frequency to be defined in 4096 equal steps. As the PFS word spans the two temporary registers R0 and R1 it is therefore essential, when changing the power frequency, that both these registers are updated before writing to R3.

The power frequency (f_{POWER}) is given by:

$$f_{POWER} = \frac{f_{RANGE}}{4096} \times pfs$$

where *pfs* = decimal value of the 12-bit PFS word and f_{RANGE} = power frequency range set in the initialisation register.

Output inhibit selection

When active (i.e., low) the output inhibit bit INH sets all the PWM outputs to the off (low) state. No other internal operation of the device is affected. When the inhibit is released the PWM outputs continue immediately. Note that as the inhibit is asserted after the pulse deletion and pulse delay circuits, pulses shorter than the normal minimum pulse width may be produced initially.

Overmodulation selection

The overmodulation bit OM is, in effect, the ninth bit (MSB) of the amplitude word. When active (i.e., high) the output waveform will be controlled in the 100% to 200% range by the amplitude word.

The percentage amplitude control is now given by:

Overmodulated Amplitude = A_{POWER} + 100%

where A_{POWER} = the power amplitude

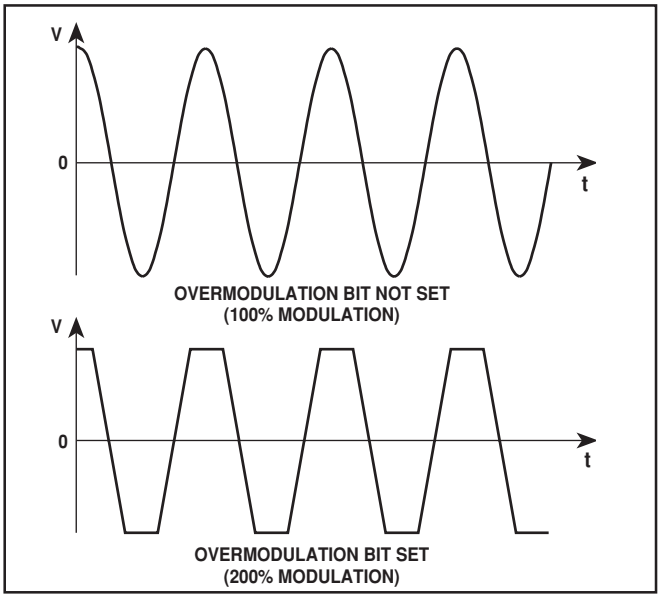


Fig. 13 Current waveforms as seen at the motor terminals, showing the effect of setting the overmodulation bit

Forward/ reverse selection

The phase sequence of the three-phase PWM output waveforms is controlled by the Forward/Reverse bit F/R. The actual effect of changing this bit from 0 (forward) to 1 (reverse) is to reverse the power frequency phase counter from incrementing the phase angle to decrementing it. The required output waveforms are all continuous with time during a forward/ reverse change.

In the forward mode the output phase sequence is red-yellow-blue and in the reverse mode the sequence is blue-yellow-red.

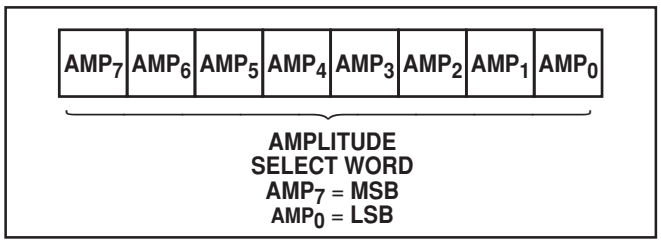


Fig.14 Temporary register R2

Amplitude selection

The power waveform amplitude is determined by scaling the amplitude of the waveform samples stored in the ROM by the value of the 8-bit amplitude select word (AMP).

The percentage amplitude control is given by:

$$\text{Power Amplitude, } A_{POWER} = \frac{A}{255} \times 100\%$$

where A = decimal value of AMP.

POWER-UP C0NDITIONS

All bits in both the Initialisation and Control registers power-up in an unidentified state. Holding $\overline{RST}$ low or using the SET TRIP input will ensure that the PWM outputs remain inactive (i.e., low) until the device is initialised.

SA828 PROGRAMMING EXAMPLE

The following example assumes that a master clock of 12·288 MHz is used (12·288 MHz crystals are readily available). This clock frequency will allow a maximum carrier frequency of 24 kHz and a maximum power frequency of 4 kHz.

Initialisation Register Programming Example

A power waveform range of up to 250Hz is required with a carrier frequency of 6kHz, a pulse deletion time of 10µs and an underlap of 5µs.

1. Setting the carrier frequency

The carrier frequency should be set first as the power frequency, pulse deletion time and pulse delay time are all defined relative to the carrier frequency.

We must calculate the value of n that will give the required carrier frequency:

$$f_{CARR} = \frac{k}{512 \times n}$$

$$\Rightarrow \mathbf{n} = \frac{k}{512 \times f_{CARR}} = \frac{12{\cdot}288 \times 10^6}{512 \times 6 \times 10^3} = \mathbf{4}$$

From Table 4, n = 4 corresponds to a 3-bit CFS word of 010 in temporary register R1.

2. Setting the power frequency range

We must calculate the value of m that will give the required power frequency:

$$f_{RANGE} = \frac{f_{CARR}}{384} \times m$$

$$\Rightarrow \mathbf{m} = \frac{f_{RANGE} \times 384}{f_{CARR}} = \frac{250 \times 384}{6 \times 10^3} = \mathbf{16}$$

From Table 5, m = 16 corresponds to a 3-bit FRS word of 100 in temporary register R1.

3. Setting the pulse delay time

As the pulse delay time affects the actual minimum pulse width seen at the PWM outputs, it is sensible to set the pulse delay time before the pulse deletion time, so that the effect of the pulse delay time can be allowed for when setting the pulse deletion time.

We must calculate the value of *pdy* that will give the required pulse delay time:

$$t_{pdy} = \frac{pdy}{f_{CARR} \times 512}$$

$$\Rightarrow \mathbf{pdy} = t_{pdy} \times f_{CARR} \times 512$$

$$= 5 \times 10^{-6} \times 6 \times 10^3 \times 512 = \mathbf{15{\cdot}4}$$

However, the value of *pdy* must be an integer. As the purpose of the pulse delay is to prevent 'shoot-through' (where both top and bottom arms of the inverter are on simultaneously), it is sensible to round the pulse delay time up to a higher, rather than a lower figure.

Thus, if we assign the value 16 to *pdy* this gives a delay time of 5·2µs. From Table 6, *pdy* = 16 corresponds to a 6-bit PDY word of 110000 in temporary register R2.

4. Setting the pulse deletion time

In setting the pulse deletion time (i.e., the minimum pulse width) account must be taken of the pulse delay time, as the actual minimum pulse width seen at the PWM outputs is equal to $t_{pd} - t_{pdy}$.

Therefore, the value of the pulse deletion time must, in this instance, be set 5·2µs longer than the minimum pulse length required

Minimum pulse length required = 10µs

$\therefore$ t_{PD} to be set to 10µs + 5·2µs = 15·2µs

Now,

$$t_{pd} = \frac{pdt}{f_{CARR} \times 512}$$

$$\Rightarrow \mathbf{pdt} = f_{pd} \times f_{CARR} \times 512$$

$$= 15{\cdot}2 \times 10^{-6} \times 6 \times 10^3 \times 512 = \mathbf{46{\cdot}7}$$

Again, *pdt* must be an integer and so must be either rounded up or down – the choice of which will depend on the application. Assuming we choose in this case the value 46 for *pdt*, this gives a value of t_{pd}, of 15 µs and an actual minimum pulse width of 15 – 5·2µs = 9·8µs.

From Table 7, *pdt* = 46 corresponds to a value of PDT, the 7-bit word in temporary register R0 of 1010010.

The data which must be programmed into the three temporary registers R0, R1 and R2 (for transfer into the initialisation register) in order to achieve the parameters in the example given, is shown in Fig. 15.

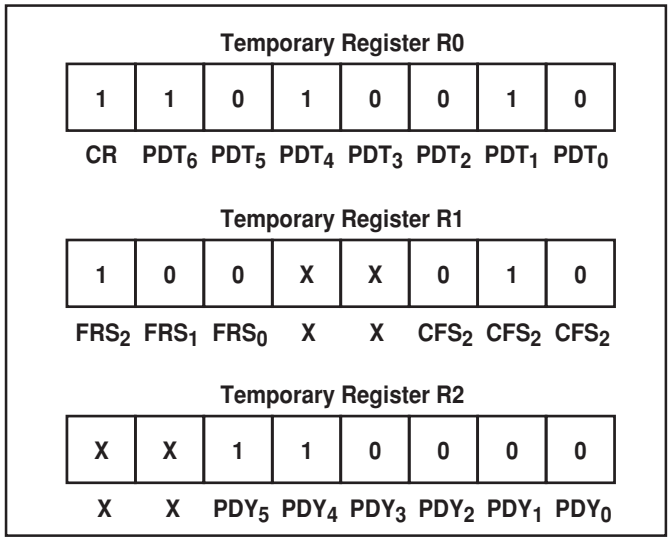


Fig. 15

Control Register Programming Example

The control register would normally be updated many times while the motor is running, but just one example is given here. It is assumed that the initialisation register has already heen programmed with the parameters given in the previous example.

A power waveform of 100Hz is required with a PWM waveform amplitude of 80% of that stored in the ROM. The phase sequence should be set to give forward motor rotation.The outputs should be enabled and no overmodulation is required.

1. Setting the power frequency

The power frequency, f_{POWER}, can be selected to 12-bit accuracy (i.e 4096 equal steps) from 0Hz to f_{RANGE} as defined in the initialisation register. In this case, with f_{RANGE} = 250Hz, the power frequency can be adjusted in increments of 0·06Hz.

$$f_{POWER} = \frac{f_{RANGE}}{4096} \times pfs$$

$$\Rightarrow \mathbf{pfs} = \frac{f_{POWER} \times 4096}{f_{RANGE}} = \frac{100 \times 4096}{250} = \mathbf{1638{\cdot}4}$$

We can only have *pfs* as an integer, so if we assign *pfs* = 1638 this gives f_{POWER} = 99.97 Hz.The 12-bit binary equivalent of this value gives a PFS word of 011001100110 in temporary registers R0 and R1.

2. Setting overmodulation, forward/reverse, output inhibit

Overmodulation is not required therefore OM = 0.

Forward motor control is required (i.e., the phase sequence of the PWM outputs should be red-yellow-blue) therefore forward/reverse bit F/R = 0.

Output inhibit should be inactive (i e., the outputs should be active), therefore INH= 1.

These bits are all set in temporary register R1.

3. Setting the power waveform amplitude

$$A_{POWER} = \frac{A}{225} \times 100\%$$

$$\Rightarrow \mathbf{A} = \frac{A_{POWER} \times 255}{100} = \frac{80 \times 255}{100} = \mathbf{204}$$

The 8-bit binary equivalent of this value gives an AMP word of 11001100 in temporary register R2. The data which must be programmed into the three temporary registers R0, R1 and R2 (for transfer into the control register) in order to achieve the parameters in the example given, is shown in Fig. 16.

Temporary Register R0

0	1	1	0	0	0	1	1
PFS_7	PFS_6	PFS_5	PFS_4	PFS_3	PFS_2	PFS_1	PFS_0

Temporary Register R1

0	0	1	X	0	1	1	0
F/R	OM	INH	X	PFS_{11}	PFS_{10}	PFS_9	PFS_8

Temporary Register R2

1	1	0	0	1	1	0	0
AMP_7	AMP_6	AMP_5	AMP_4	AMP_3	AMP_2	AMP_1	AMP_0

Fig. 16

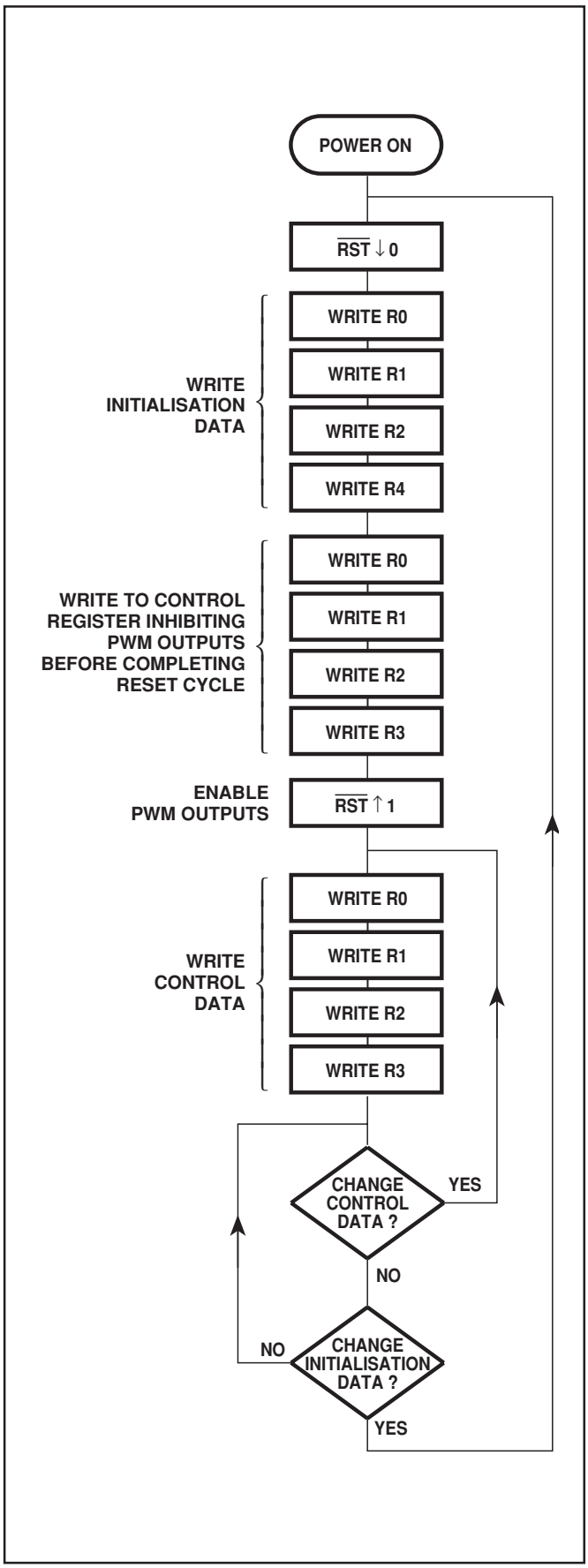


Fig. 17 Typical SA828 programming routine

HARDWARE INPUT/OUTPUT FUNCTIONS

Set Output Trip (SET TRIP input)

The SET TRIP input is provided separately from the microprocessor interface in order to allow an external source to override the microprocessor and provide a rapid shutdown facility. For example, logic signals from overcurrent sensing circuitry or the microprocessor 'watchdog' might be used to activate this input.

When the SET TRIP input is taken to a logic high, the output trip latch is activated. This results in the $\overline{TRIP}$ output and the six PWM outputs being latched low immediately. This condition can only be cleared by applying a reset cycle to the $\overline{RST}$ input.

It is essential that when not in use SET TRIP is tied low and isolated from potential sources of noise; on no account should it be left floating.

SET TRIP is latched internally at the master clock rate in order to reduce noise sensitivity.

Output Trip Status ($\overline{TRIP}$ output)

The $\overline{TRIP}$ output indicates the status of the output trip latch and is active low.

Reset ($\overline{RST}$ input)

The $\overline{RST}$ input performs the following functions when active (low):

1. All PWM outputs are forced low (if not already low) thereby turning off the drive switches.
2. All internal counters are reset to zero (this corresponds to 0° for the red phase output).
3. The rising edge of $\overline{RST}$ reactivates the PWM outputs resetting the output trip and setting the $\overline{TRIP}$ output high – assuming that the SET TRIP input is inactive (i.e. low).

A sixth register, R5, located at A2:O = 101 is used to place the device into a factory test mode. This is achieved by writing dummy data to R5 immediately after $\overline{RST}$ goes high. Care must be exercised to ensure that the microprocessor/controller cannot write to this register.

Zero Phase Pulses (ZPPR, ZPPY and ZPPB outputs)

The zero phase pulse outputs provide pulses at the same frequency as the power frequency with a 1 : 2 mark-space ratio. When in the forward mode of operation the falling edge of ZPPR corresponds to 0° for the red phase, the falling edge of ZPPY to 0° for the yellow phase and the ZPPB falling edge to 0° for the blue phase. In the reverse mode, the rising edge of a zero phase pulse corresponds to 0° for the relevant phase PWM output.

Waveform Sampling Synchronisation (WSS output)

This output provides a square wave signal of 50% duty cycle at a frequency 1536 times higher than the fundamental of the power waveform. Each successive pulse of WSS corresponds to the SA828 reading the next location of the waveform ROM. It may be used in conjunction with the ZPP signals to monitor the position of the machine rotor and may form part of a closed loop control system such as slip compensation.

Clock (CLK input)

The CLK input provides a timing reference used by the SA828 for all timings related to the PWM outputs. The microprocessor interface, however, derives all its timings from the microprocessor and therefore the microprocessor and the SA828 may be run either from the same or from different clocks.

WAVEFORM DEFINITION

The waveform amplitude data used to construct the PWM output sequences is read from the internal 384X8 ROM. This contains the 90° span of the waveform as shown in Fig. 18. Each successive 8-bit sample linearly represents the instantaneous amplitude of the waveform. It is assumed that the waveform is symmetrical about the 90°, 180° and 270° axes. The SA828 reconstructs the full 360° waveform by reading the 0°-90° section held in ROM and assigning negative values for the second half of the cycle.

These samples are used to calculate the instantaneous amplitudes for all three phases, which will be 120° transposed in the normal R-Y-B orientation for forward rotation or B-Y-R for reverse rotation. The 384 8-bit samples are regularly spaced over the 0° to 90° span, giving an angular resolution of approximately 0·23°.

Waveform segment	Sample number
0°- 30°	0 - 127
30·23°- 60°	128 - 255
60·23°- 89·77°	256 - 383

Table 8 90° of the 360° cycle is divided into 384 8-bit samples

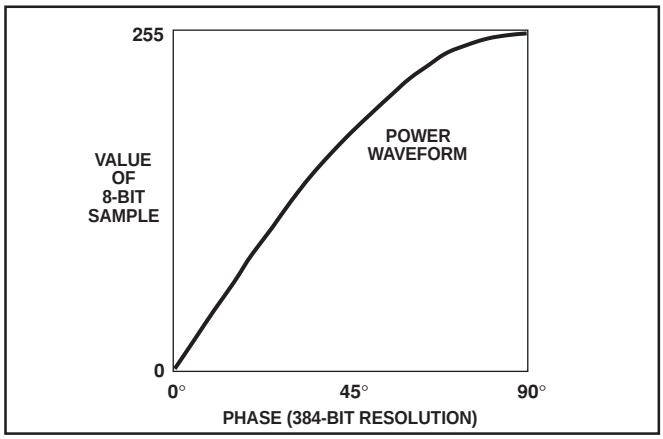


Fig. 18 90° sample of typical power waveform

PRODUCT DESIGNATION

Two standard options exist, defining waveform shape. These are designated SA828-1 and SA828-2 as follows:

SA828-1

Sine + third harmonic at one-sixth the amplitude of the fundamental:

$$x(t) = A\left[\sin(\omega t) + \frac{1}{6}\sin 3(\omega t)\right]$$

SA828-2

Pure sinewave:

$$x(t) = A\left[\sin(\omega t)\right]$$

Additional wave shapes can be implemented to order, provided they are symmetrical about the 90°, 180° and 270° axes. Contact your local Mitel Semiconductor Customer Service Centre for further details.

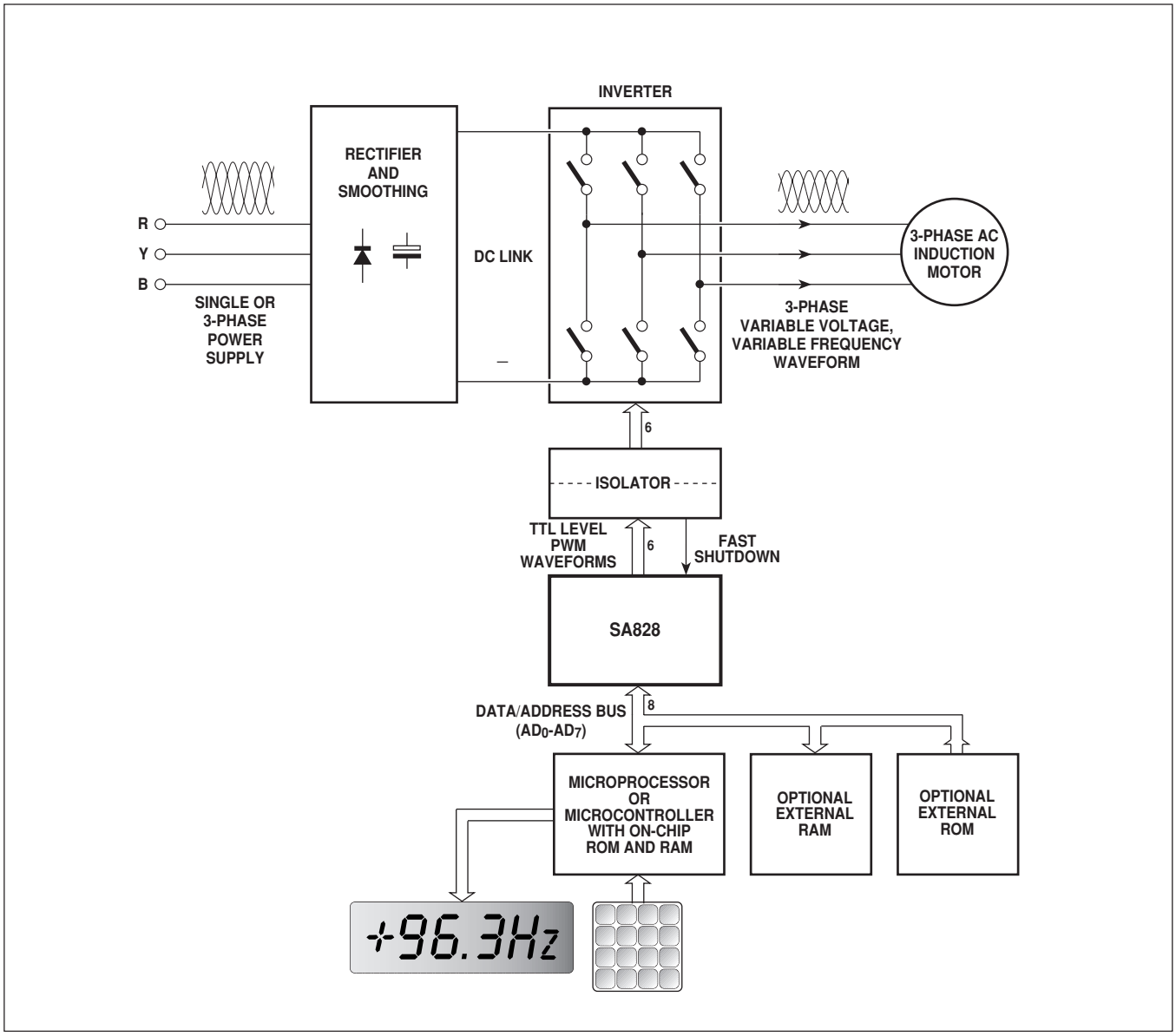
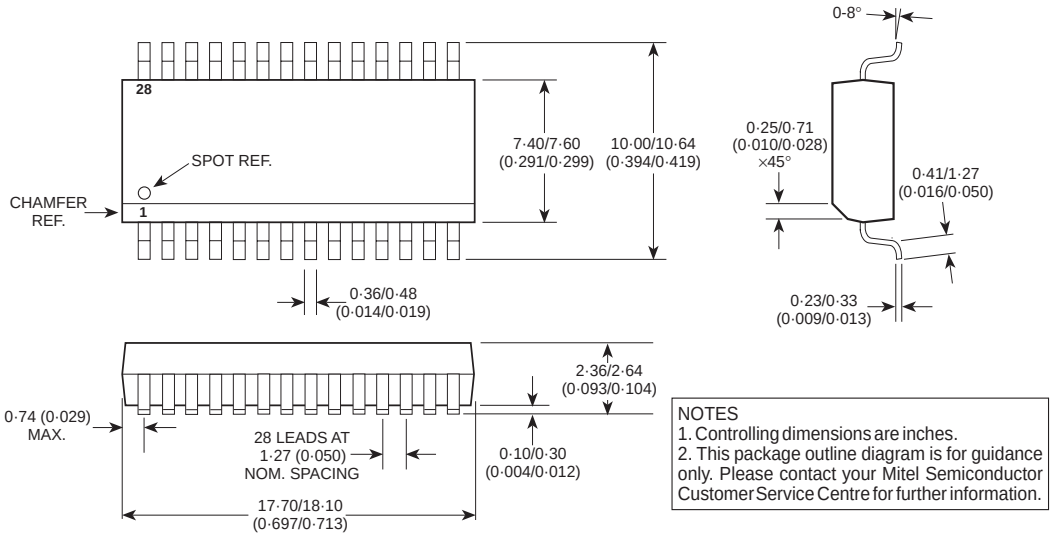


Fig. 19 A typical SA828 application

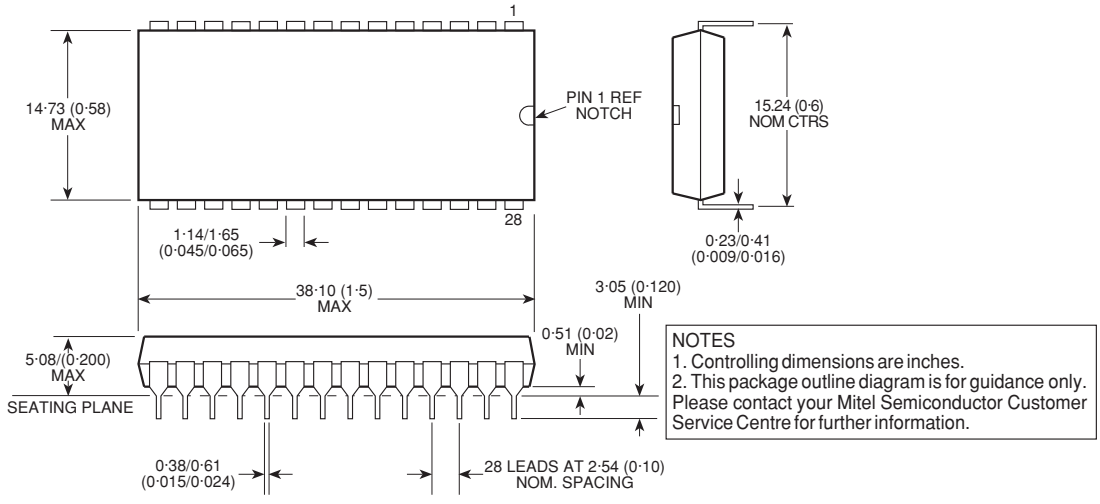
PACKAGE DETAILS

Dimensions are shown thus: mm (in). For further package information, please contact your local Customer Service Centre.



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your Mitel Semiconductor Customer Service Centre for further information.

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MITEL

SEMICONDUCTOR

HEADQUARTERS OPERATIONS
MITEL SEMICONDUCTOR
Cheney Manor, Swindon,
Wiltshire SN2 2QW, United Kingdom.
Tel: (01793) 518000
Fax: (01793) 518411

MITEL SEMICONDUCTOR
1500 Green Hills Road,
Scotts Valley, California 95066-4922
United States of America.
Tel (408) 438 2900
Fax: (408) 438 5576/6231

Internet: http://www.gpsemi.com
CUSTOMER SERVICE CENTRES
- **FRANCE & BENELUX** Les Ulis Cedex Tel: (1) 69 18 90 00 Fax : (1) 64 46 06 07
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- **SOUTH EAST ASIA** Singapore Tel:(65) 3827708 Fax: (65) 3828872
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