# SA58646

## UHF 900 MHz transceiver IC

Rev. 01 — 8 February 2007 Product data sheet

## 1. General description

The SA58646 is a BiCMOS integrated circuit that performs all functions from the antenna to the microcontroller for reception and transmission for both the base station and the handset in a 902 MHz to 928 MHz full-duplex radio. The SA58646 may be used in a UHF push-to-talk walkie-talkie or in a UHF to 900 MHz data transceiver. The SA58646 is a pin-compatible derivative of the UAA3515 with advanced features.

This IC integrates most of the functions required for a half-duplex or full-duplex radio in a single integrated circuit. Additionally, the programmability implemented reduces significantly external components count, board space requirements and external adjustments.

## 2. Features

- RF RX (single frequency conversion FM receiver):
  - Integrated LNA
  - Image reject mixer
  - FM detector at 10.7 MHz including an IF limiter, a wide band PLL demodulator, an output amplifier and a RSSI output
  - Carrier detection with programmable threshold
  - Programmable data amplifier (slicer) phase
- Synthesizer:
  - Crystal reference oscillator with integrated tuning capacitor
  - Reference frequency divider
  - Narrow band RX PLL including RX VCO with integrated varicaps
  - Narrow band TX PLL including TX VCO with integrated varicaps
  - VCO external inductors can be done with printed transmission lines on the PCB which offers substantial savings
  - Programmable clock divider with output buffer to drive a microcontroller
- Baseband RX section:
  - Programmable RX gain (enable phone volume control)
  - Expander with output noise level control
  - Earpiece amplifier with volume control feature
  - Data amplifier
- Baseband TX section:
  - Microphone amplifier
  - Compressor with automatic level control and hard limiter
  - Programmable TX gain

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- Microcontroller interface:
  - 3-wire serial interface
- Other features:
  - Voltage regulator to supply internal PLLs
  - Selectable voltage doubler
  - Programmable low battery detection time multiplexed with RSSI carrier detection

## 3. Applications

- 902 MHz to 928 MHz full-duplex radio
- UHF to 900 MHz data transceiver
- UHF push-to-talk walkie-talkie

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| SA58646BD | LQFP64 | plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm | SOT314-2 |



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## 5. Block diagram

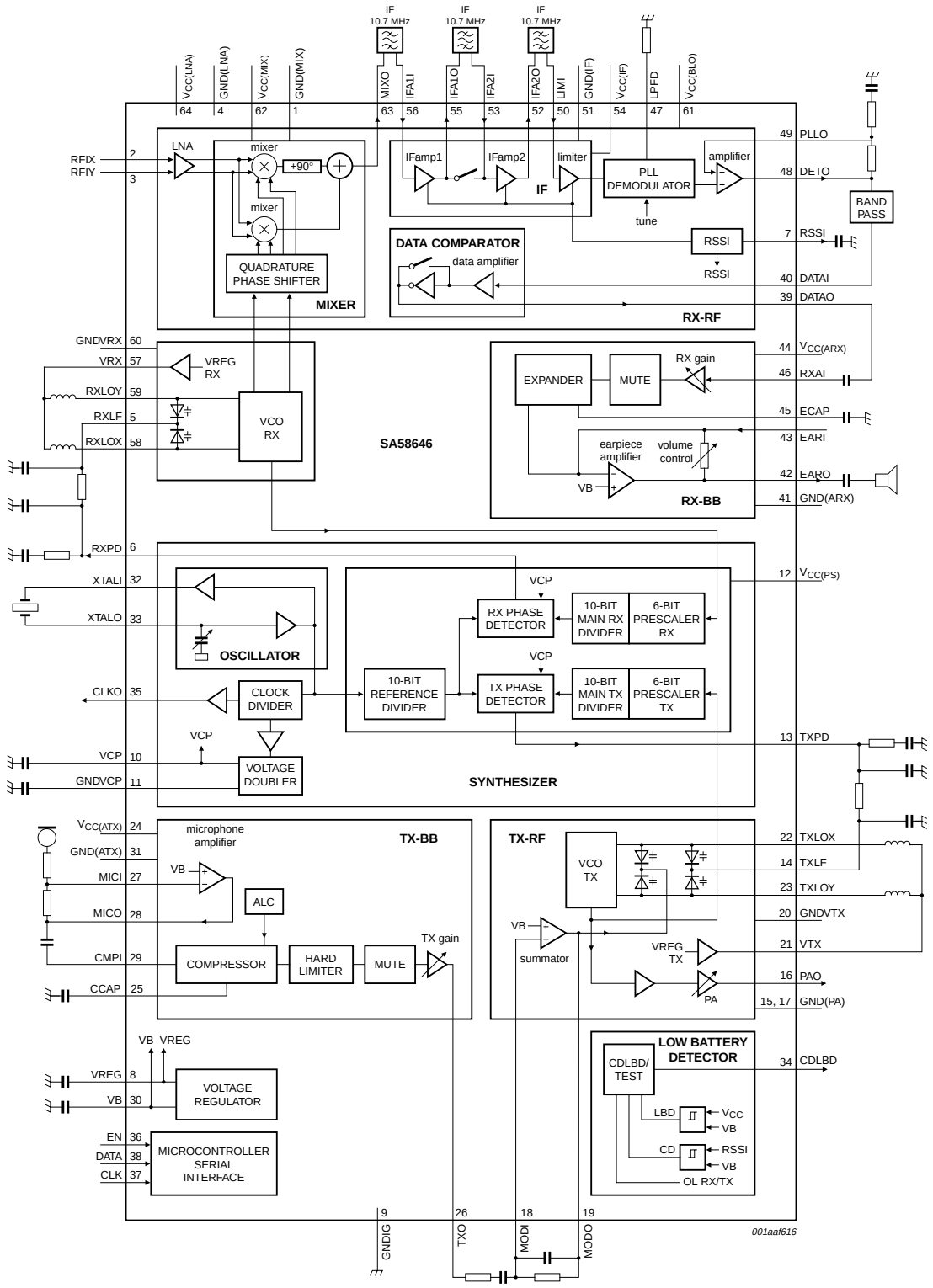



**Fig 1. Block diagram of SA58646**



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# 6. Pinning information

## 6.1 Pinning

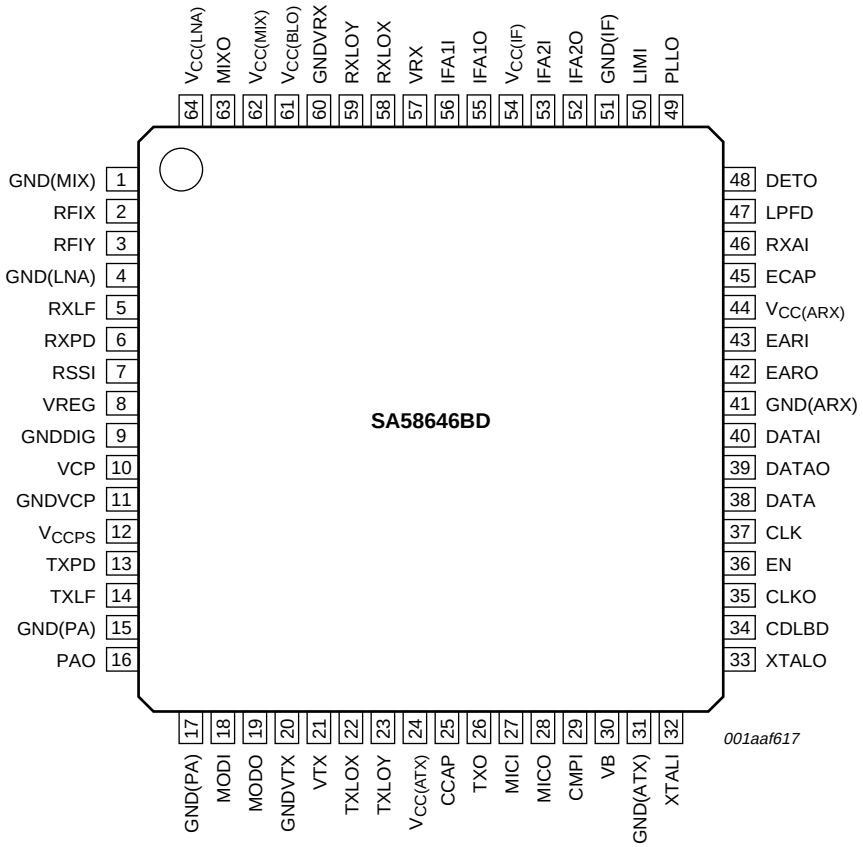



**Fig 2. Pin configuration**

## 6.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| GND(MIX) | 1 | mixer ground |
| RFIX | 2 | LNA input x |
| RFIY | 3 | LNA input y |
| GND(LNA) | 4 | LNA ground |
| RXLF | 5 | RX loop filter output |
| RXPD | 6 | RX phase detector output |
| RSSI | 7 | RSSI output |
| VREG | 8 | internal voltage regulator capacitor connection |
| GNDDIG | 9 | digital parts ground |
| VCP | 10 | charge pump voltage output |
| GNDVCP | 11 | charge pump ground |


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**Table 2. Pin description** *…continued*

| Symbol | Pin | Description |
|---|---|---|
| $V_{CC(PS)}$ | 12 | prescaler supply |
| TXPD | 13 | TX phase detector output |
| TXLF | 14 | TX loop filter output |
| GND(PA) | 15 | PA ground |
| PAO | 16 | PA output |
| GND(PA) | 17 | PA ground |
| MODI | 18 | summator amplifier input |
| MODO | 19 | summator amplifier output |
| GNDVTX | 20 | VCO TX ground |
| VTX | 21 | VCO TX voltage output |
| TXLOX | 22 | VCO TX coil connection x |
| TXLOY | 23 | VCO TX coil connection y |
| $V_{CC(ATX)}$ | 24 | audio TX supply |
| CCAP | 25 | external capacitor connection for compressor |
| TXO | 26 | audio TX output |
| MICI | 27 | microphone amplifier input |
| MICO | 28 | microphone amplifier output |
| CMPI | 29 | compressor input |
| VB | 30 | voltage reference capacitor connection |
| GND(ATX) | 31 | audio TX ground |
| XTALI | 32 | crystal input |
| XTALO | 33 | crystal output |
| CDLBD | 34 | carrier detector or low battery detector output (out-of-lock synthesizer RX and/or TX in Test mode) |
| CLKO | 35 | clock output |
| EN | 36 | serial interface enable input |
| CLK | 37 | serial interface clock input |
| DATA | 38 | serial interface data input |
| DATAO | 39 | data amplifier output |
| DATAI | 40 | data amplifier input |
| GND(ARX) | 41 | audio RX ground |
| EARO | 42 | earpiece amplifier output |
| EARI | 43 | earpiece amplifier input |
| $V_{CC(ARX)}$ | 44 | audio RX supply |
| ECAP | 45 | external capacitor connection for expander |
| RXAI | 46 | audio RX input |
| LPFD | 47 | demodulator loop filter |
| DETO | 48 | inverting demodulator amplifier output |
| PLLO | 49 | demodulator amplifier negative input |
| LIMI | 50 | limiter input |
| GND(IF) | 51 | IF ground |



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**Table 2. Pin description** *…continued*

| Symbol | Pin | Description |
|---|---|---|
| IFA2O | 52 | IF second amplifier output |
| IFA2I | 53 | IF second amplifier input |
| $V_{CC(IF)}$ | 54 | IF supply |
| IFA1O | 55 | IF first amplifier output |
| IFA1I | 56 | IF first amplifier input |
| VRX | 57 | VCO RX voltage output |
| RXLOX | 58 | VCO RX coil connection x |
| RXLOY | 59 | VCO RX coil connection y |
| GNDVRX | 60 | VCO RX ground |
| $V_{CC(BLO)}$ | 61 | RX LO buffer supply |
| $V_{CC(MIX)}$ | 62 | mixer supply |
| MIXO | 63 | mixer output |
| $V_{CC(LNA)}$ | 64 | LNA supply |



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# 7. Functional description

Refer to Figure 1 “Block diagram of SA58646”.

## 7.1 Power supply and power management

### 7.1.1 Power supply voltage

This circuit is used in a full-duplex radio handset and base unit. The handset unit is battery powered and can operate on three NiCad cells. The minimum supply voltage of the IC is $V_{CC}$ = 2.9 V.

### 7.1.2 Power-saving operation modes

When the circuit is used in a handset, it is important to reduce the current consumption. There are 3 main modes of operation:

- Active mode (talk): all blocks are powered
- RX mode: all circuitry in the RF receiver part is active
- Inactive mode: all circuitry is powered down except the serial interface. In this latter mode the crystal reference oscillator, output clock buffer, voltage regulator and voltage doubler can be disabled separately.

A low current consumption mode on the crystal oscillator and clock output can be programmed. Latch memory is maintained in all modes. Table 3 shows which blocks are powered in each mode.

**Table 3. Powered blocks**

| Circuit block | Mode | | |
|---|---|---|---|
| | Active | RX | Inactive |
| VB reference | X | X | - |
| RX-RF | X | X | - |
| RX PLL | X | X | - |
| RX and TX audio | X | - | - |
| TX-RF (and PA if enabled) | X | - | - |

Some blocks can be activated separately: crystal oscillator, voltage regulator (adjustment is always disabled), power amplifier, voltage doubler, hard limiter, automatic level control, output clock buffer and earpiece amplifier. Table 4 shows which block can be activated in each mode.



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**Table 4. Activated blocks**

| Circuit block | Mode | | |
|---|---|---|---|
| | Active | RX | Inactive |
| Crystal active[1] | X | X | X |
| Clock output not disabled | X | X | X |
| Voltage regulator active[2] | X | X | X |
| Power amplifier active | X | - | - |
| Doubler enabled[3] | X | X | X |
| Hard limiter or automatic level control not disabled | X | - | - |
| Earpiece amplifier enabled | X | X | -[4] |

[1] In RX and TX mode, the crystal oscillator is automatically activated. An external frequency can be forced to pins XTALI and XTALO.

[2] In RX and TX mode, the voltage regulator with adjustment is automatically enabled; bit REG can be either logic 1 or logic 0.

[3] If the voltage doubler is enabled, the crystal oscillator is automatically activated.

[4] In Inactive mode, the earpiece amplifier is automatically disabled.

### 7.1.3 Control bits in power saving modes

Table 5 shows the control bit values for selection of each mode and the typical current consumption for those modes.

**Table 5. Control bit values**

*$V_{CC}$ = 3.3 V; $T_{amb}$ = 25 °C; $f_{xtal}$ = 10.24 MHz.*

| Power saving mode | MODE[1:0] | | Conditions | | | | Typical current consumption |
|---|---|---|---|---|---|---|---|
| | Bit 1 | Bit 0 | Voltage doubler | Crystal oscillator | Voltage regulator | Clock output | |
| Active mode | 1 | 1 | - | - | - | - | 76 mA |
| RX mode | 1 | 0 | - | - | - | - | 58 mA |
| Inactive mode | 0 | X | inactive | disabled | disabled | disabled | < 10 µA |
| | | | | XTAL_H = 0 | | | 210 µA |
| | | | | XTAL_H = 1 | | | 300 µA |
| | | | inactive | XTAL_H = 1 | enabled | disabled | 550 µA |
| | | | active | | | | 690 µA |

When the clock output is activated, an extra power consumption is applied which is proportional to the programmed bit CLKO. If bit XTAL_H = 0, then the crystal loss is less than 50 Ω to ensure reliable start-up.

**Table 6. Extra power consumption**

| Divider ratio | Extra current consumption | |
|---|---|---|
| Bits CLK_DIV[2:0] | Bit CLKO = 0 | Bit CLKO = 1 |
| XXX (1, 2, 2.5, 4, 128) | 520 µA | 350 µA |
| 000 (off) | 0 µA | 0 µA |



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## 7.2 FM receiver part

The FM receiver has a single frequency conversion architecture. The image reject mixer enables the user to save an RF filter. The side band select feature (bit SBS) enables the user to choose its frequency plan with RX LO in or out of ISM band and have the same IC for both base and handset. An IF channel filtering compromise between price and performance can be achieved using two or three 10.7 MHz external filters. The integrated FM PLL demodulator with limiter enables consistent saving on external components and pins.

The data comparator is an inverting hysteresis comparator. The open-collector output is current limited to control the output signal slew rate. An external band-pass filter is connected between pins DETO and DATAI (AC coupled). The external resistor should be 180 kΩ at maximum $V_{CC}$. An external capacitor can be added to further reduce the slew rate.

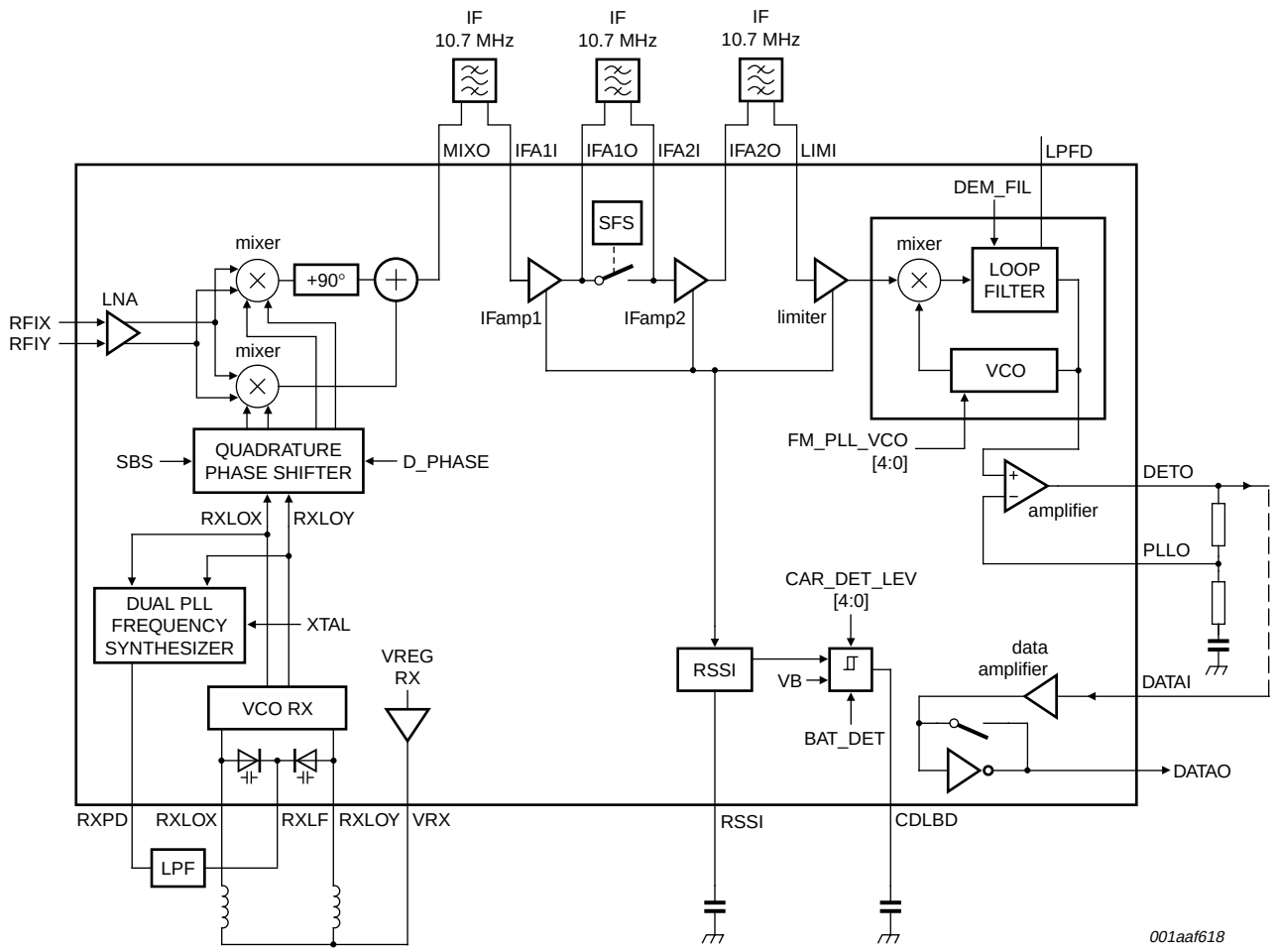



**Fig 3. FM receiver part**



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## 7.3 Transmitter part

The transmitter architecture is of the direct modulation type. The transmit VCO will be frequency modulated by either speech or data (see Figure 4).

Before the VCO, an amplifier sums the modulating signal and the data TX signal. VCO varicaps are integrated. External inductors that are in series with bonding wires and lead frame are needed to obtain the right frequency. The power amplifier is capable of driving 50 Ω. The output level is programmed through the serial bus interface.

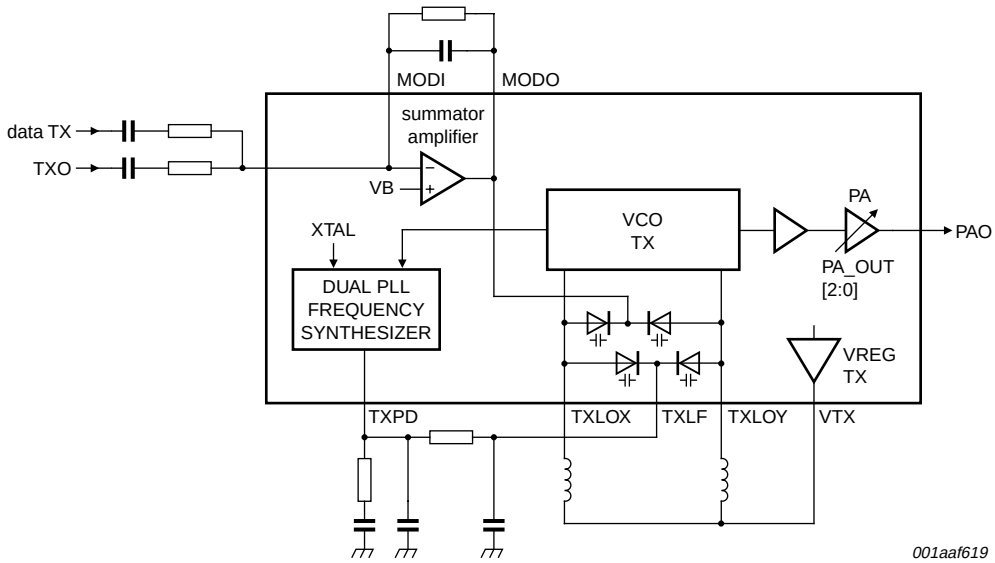



**Fig 4. Transmit part**

## 7.4 Synthesizer

The crystal local oscillator and reference divider provide the reference frequency for the RX and TX PLLs. The 10-bit programmed divider value for the reference divider is selected based on the crystal frequency, the desired RX and TX reference frequency values. The crystal frequency of 16.348 MHz is chosen to provide to the microcontroller the standard 4.096 MHz frequency when programming the clock divider value to 4. Then the 16.384 MHz crystal frequency is proposed. The clock divider value will be programmed to 1, 2, 2.5, 4 and 128. The clock divider value of 128 is chosen to place the SA58646 in Sleep mode which enables current saving in the microcontroller. The clock output is an emitter follower type.

The 16-bit TX counter is programmed for the desired transmit channel frequency. The 16-bit RX counter is programmed for the desired local oscillator frequency. The counters are built with a 6-bit prescaler (divider value R from 64 to 127) and a 10-bit divider (divider value C from 8 to 1023). The full counter then provides a divider value from 512 to 65535. To calculate the settings of the two counters, the following procedure is used:

$C = \text{int}(M / 64)$

$R = M - C \times 64$

where M being the division ratio between the VCO frequency and the reference frequency.


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**Example:** RF RX f = 903 MHz, VCO RX f = 892.3 MHz, IF f = 10.7 MHz, VCO TX f = 925.6 MHz and the internal comparison frequency f = 20 kHz ($f_{xtal}$ = 10.24 MHz):

REF_DIV[9:0] = 512 (10 0000 0000),

For RX: M = $892.3 \times 10^6 / 20 \times 10^3$ = 44615, C = 697 (10 1011 1001), R = 7 (00 0111),

For TX: M = $925.6 \times 10^6 / 20 \times 10^3$ = 46280, C = 723 (10 1101 0011), R = 8 (00 1000).

VCOs and varicaps are integrated. The total equivalent inductance is comprised of the bonding wires, lead frame of the package and external inductors. External inductors can be done with printed transmission lines on the PCB, which allows substantial savings.

An on-chip selectable voltage doubler is provided to enable a larger tuning range of the VCOs.

The phase detectors have current drive type outputs. Current can be chosen between 400 μA and 800 μA.

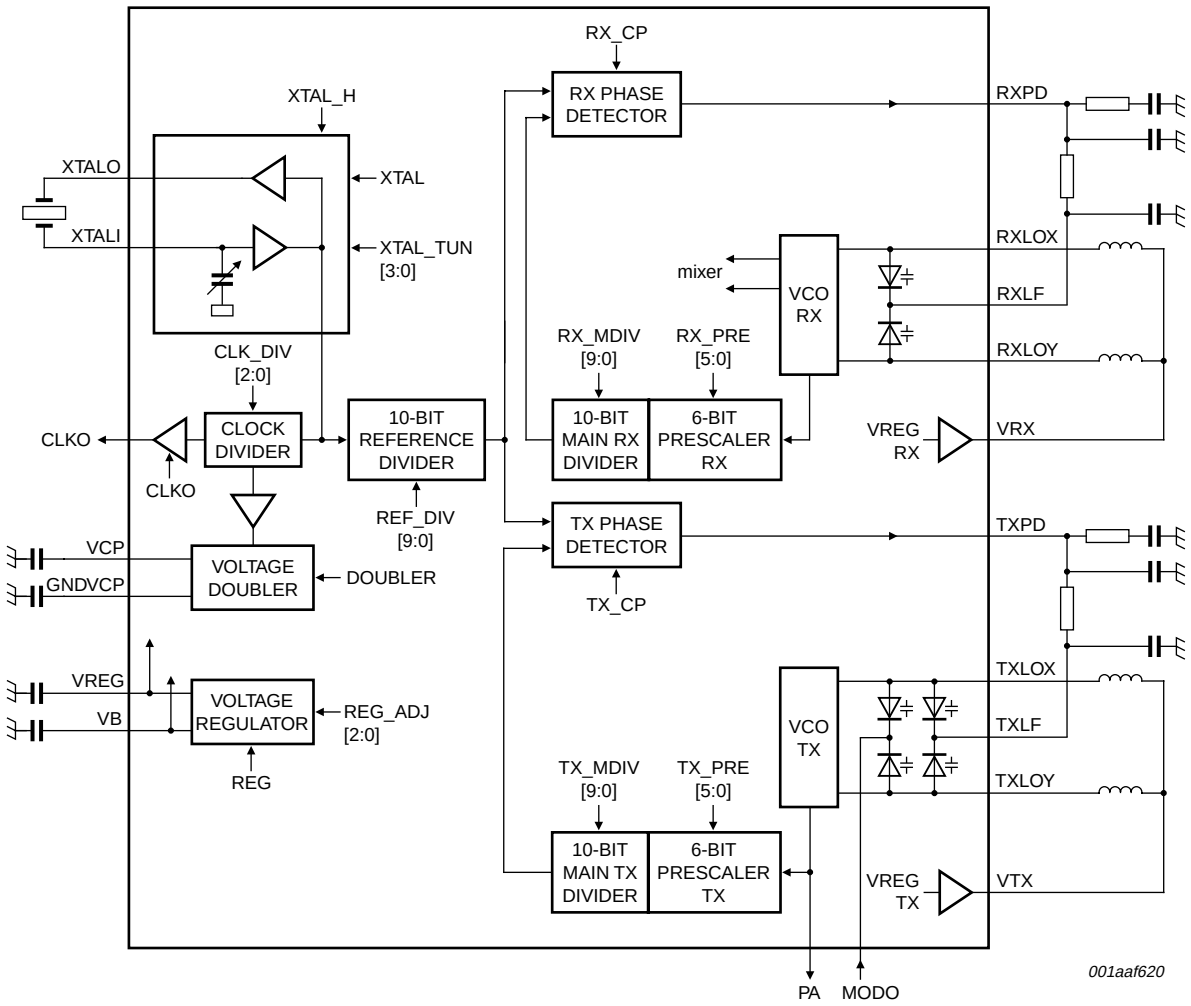



**Fig 5. Synthesizer part**



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## 7.5 RX baseband

This section covers the RX audio path from pins RXAI to EARO. The RXAI input signal is AC-coupled. The microcontroller sets the value of the RX gain with 32 linear steps of 0.5 dB. The RX baseband has a mute and an expander with the characteristics shown in Figure 7. The audio level is programmable over a dynamic range of 31 dB by the RX gain control. The expander slope multiplies the RX gain step by 2 to achieve 1 dB steps on the earpiece output. Noise coming from, and within, the RX baseband can be shaped thanks to a 'noise control' programmability. It provides the possibility to attenuate the expander gain at low input level. Figure 7 provides some information about the noise shaper function. The earpiece amplifier is an inverting rail-to-rail operational amplifier. The non-inverting input is connected to the internal VB reference voltage. Software volume control on the earpiece amplifier is done by integrated switched feedback resistances. Volume control tuning range is 14 dB. Hardware volume control is done by externally switching the earpiece feedback resistance.

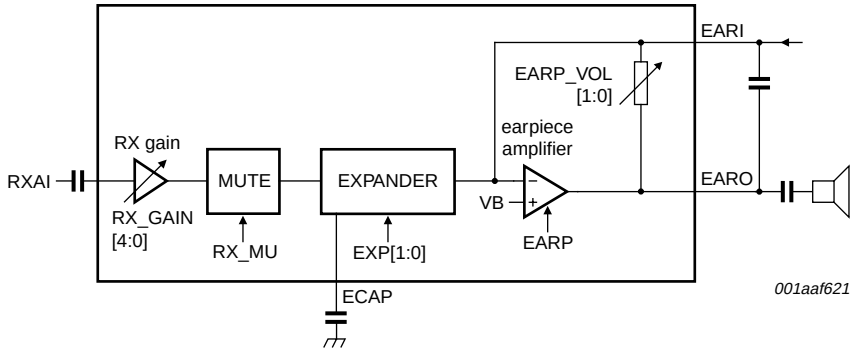
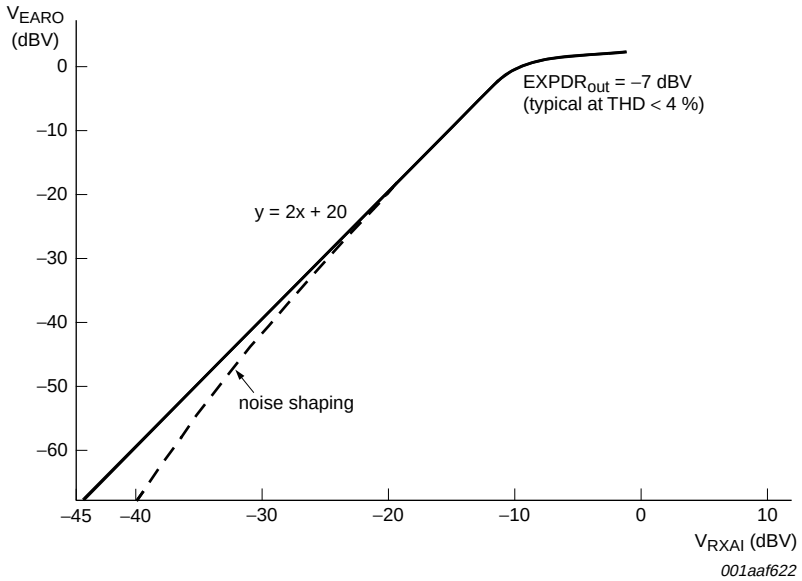



**Fig 6. RX baseband part**




RX gain adjustment at 0 dB; volume earpiece at 0 dB; no external resistance.

**Fig 7. Expander characteristic**



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## 7.6 TX baseband

This section covers the TX audio path from pins MICI to TXO. The input signal at pin MICI is AC-coupled. The microphone amplifier output is also AC-coupled.

The microphone amplifier is an inverting operational amplifier whose gain can be set by external resistors. The non-inverting input is connected to the internal VB reference voltage. External resistors are used to set the gain and frequency response.

The TX baseband has a compressor with the characteristic shown in Figure 9. The Automatic Level Control (ALC) provides a 'soft' limit to the output signal swing as the input voltage increases slowly (that is, a sine wave is maintained at the output). A hard limiter clamps the compressor output voltage at 1.26 V (p-p). The ALC and hard limiter can be disabled via the microcontroller interface. The hard limiter is followed by a mute. The TX gain is digitally programmable with 32 steps of 0.5 dB.

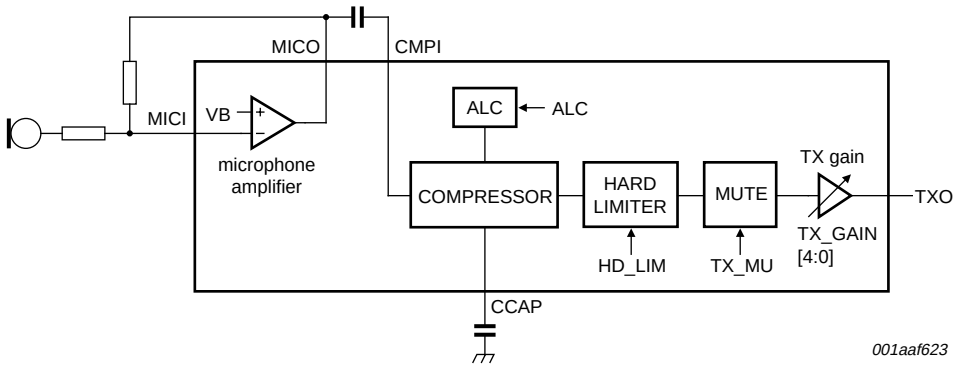



**Fig 8. TX baseband part**

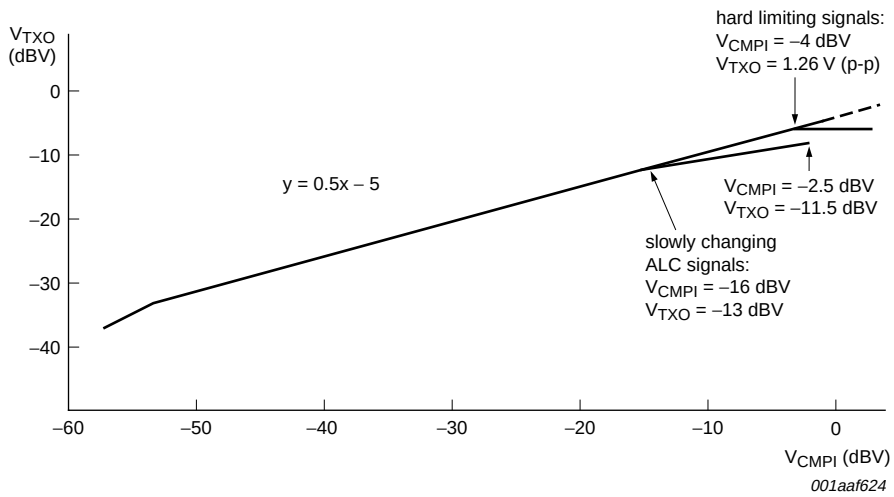



**Fig 9. Compressor characteristic**



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## 7.7 Other features

### 7.7.1 Voltage regulator

Regulator voltage VREG is the internal supply for the RX and TX PLLs. It is regulated at 2.7 V nominal voltage. Two capacitors with 4.7 µF and 100 nF values must be connected to pin VREG to filter and stabilize this regulated voltage. The tolerance of the regulated voltage is initially ±8 % but is improved to ±2 % after the internal band gap voltage reference is adjusted via the microcontroller interface. In Inactive mode, the regulator voltage adjustment is automatically disabled.

### 7.7.2 Low battery detector

The low battery detector measures the supply voltage $V_{CC}$ with a resistor divider and a comparator. One input of the comparator is connected to reference voltage VB and the other is connected to the middle point of the resistor divider. To prevent spurious switching the comparator has a built-in hysteresis. The precision of the detection depends on the divider accuracy, the comparator offset and the accuracy of the reference voltage. The output is multiplexed at pin CDLBD. When the battery voltage level is under the threshold voltage, the CDLBD output is set at LOW level.

## 7.8 Microcontroller serial interface

The serial interface is used for programming the IC. To program the IC, 19 bits are used: 16 bits for data and 3 bits for register addresses. The serial interface requires 3 pins: DATA, CLK, EN (see Figure 10).

The serial interface pins are supplied by regulator voltage VREG. The ESD protection diodes on these pins are connected to the supply voltage $V_{CC}$. Digital outputs (CDLBD and DATAO) have open-collector or open-drain; CLKO is an emitter-follower output.

The DATA, CLK and EN pins provide a 3-wire unidirectional serial interface for programming the reference counters, the transmit and receive channel divider counters, and the control functions.

The interface consists of 19-bit shift registers connected to a matrix of registers organized as 7 words of 16 bits (all control registers). The data is entered with the most significant bit first. The leading 16 bits include the data (D15 to D0), while the trailing 3 bits set up the address (AD2 to AD0). The first bit entered is D15, the last bit AD0.

The DATA and CLK pins are used to load data into the shift registers. Data is clocked into the shift registers on negative clock transitions.

A new clock divider ratio is enabled thanks to an extra EN rising edge. Minimum hold time is 50 ns. During that time, no clock cycle is allowed. These extra EN edges can be applied to all the data programmed, but will have no effect on the serial interface programming.

# 8. Data registers and addresses

D15 is the most significant bit, and is written first. Table 7 shows the data latches and addresses which are used to select each of the registers.



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**Table 7. Data registers including preset values at power-on**

| Addr | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 000 | SBS | EARP_VOL[1:0] | | EARP | RX_GAIN[4:0] | | | | | SFS | D_PHASE | FM_PLL_VCO[4:0] | | | | |
| | 0 | 11 | | 0 | 0 1111 | | | | | 1 | 0 | 0 1111 | | | | |
| 001 | RX_PRE[5:0] | | | | | | RX_MDIV[9:0] | | | | | | | | | |
| | XX XXXX | | | | | | XX XXXX XXXX | | | | | | | | | |
| 010 | [1] | | | | | | REF_DIV[9:0] | | | | | | | | | |
| | 00 0000 | | | | | | XX XXXX XXXX | | | | | | | | | |
| 011 | TX_PRE[5:0] | | | | | | TX_MDIV[9:0] | | | | | | | | | |
| | XX XXXX | | | | | | XX XXXX XXXX | | | | | | | | | |
| 100 | TM2 | CLKO | TM1 | DOUBLER | TX_GAIN[4:0] | | | | | TX_MU | HD_LIM | ALC | XTAL | RX_MU | DEM_FIL | [1] |
| | 0 | 0 | 0 | 0 | 01111 | | | | | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 101 | REG | MODE[1:0] | | XTAL_H | CAR_DET_LEV[4:0] | | | | | L_BAT_DET[2:0] | | | BAT_DET | CLK_DIV[2:0] | | |
| | 1 | 00 | | 1 | 0 0000 | | | | | 000 | | | 1 | 100 | | |
| 110 | PA_OUT[2:0] | | | TX_CP | RX_CP | REG_ADJ[2:0] | | | EXP[1:0] | | TM0 | [1] | XTAL_TUN[3:0] | | | |
| | 010 | | | 0 | 0 | 011 | | | 00 | | 0 | 0 | 0111 | | | |

[1] Undefined zone should always be programmed with logic 0.



SA58646_1

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## 8.1 Data register 0

**Table 8. Data register 0 (address 000h) bit description**

*Legend: * reset value.*

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 15 | SBS | | **Side band select**. The image reject mixer can be programmed to either reject the image frequency at the LO upper frequency or at the LO lower frequency. It enables the user to have the RX LO in or out of ISM band and to use the same IC in both handset and base. |
| | | 0* | frequency LO – IF is rejected |
| | | 1 | frequency LO + IF is rejected |
| 14 to 13 | EARP_VOL[1:0] | | **Earpiece volume control.** Software gain control on the earpiece amplifier is done with integrated switch feedback resistances. |
| | | 00 | $R_{fbck}$ = 14 kΩ, $G_{ctrl}$ = 0 dB |
| | | 01 | $R_{fbck}$ = 24 kΩ, $G_{ctrl}$ = 4.7 dB |
| | | 10 | $R_{fbck}$ = 41 kΩ, $G_{ctrl}$ = 9.3 dB |
| | | 11* | $R_{fbck}$ = 70.2 kΩ, $G_{ctrl}$ = 14 dB |
| 12 | EARP | | **Earpiece** |
| | | 0* | earpiece disable |
| | | 1 | earpiece enable; can be used in RX mode for specific feature |
| 11 to 7 | RX_GAIN[4:0] | | **RX gain setting** |
| | | 0 1111* | for values, see Table 9 |
| 6 | SFS | | **Second filter select.** Depending on the features of the IF filters used, the user might not need to use the second IF filter. IF filters having 4.5 dB insertion loss are recommended. |
| | | 0 | second IF filter not selected |
| | | 1* | second IF filter selected |
| 5 | D_PHASE | | **Data phase shifter.** The SBS bit is used to invert the phase of the data. Depending on the SBS bit value and the protocol chosen, the data can be inverted between the base and handset data transmission. To correct the data polarity, bit D_PHASE is set. |
| | | 0* | inverter is bypassed |
| | | 1 | inverter is used |
| 4 to 0 | FM_PLL_VCO[4:0] | | **PLL center frequency calibration**. This programming allows calibration of the center frequency of the VCO within the FM PLL to align the frequency as close as possible to the nominal 10.7 MHz frequency. |
| | | 0 1111* | For values, see Table 10 |



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**Table 9. TX and RX gain**

| Select | RX_GAIN[4:0] and TX_GAIN[4:0] | | | | | RX and TX gain (dB) | Earpiece output (dB) |
|---|---|---|---|---|---|---|---|
| | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | | |
| 0 | 0 | 0 | 0 | 0 | 0 | −7.5 | −15.0 |
| 1 | 0 | 0 | 0 | 0 | 1 | −7.0 | −14.0 |
| 2 | 0 | 0 | 0 | 1 | 0 | −6.5 | −13.0 |
| 3 | 0 | 0 | 0 | 1 | 1 | −6.0 | −12.0 |
| 4 | 0 | 0 | 1 | 0 | 0 | −5.5 | −11.0 |
| 5 | 0 | 0 | 1 | 0 | 1 | −5.0 | −10.0 |
| 6 | 0 | 0 | 1 | 1 | 0 | −4.5 | −9.0 |
| 7 | 0 | 0 | 1 | 1 | 1 | −4.0 | −8.0 |
| 8 | 0 | 1 | 0 | 0 | 0 | −3.5 | −7.0 |
| 9 | 0 | 1 | 0 | 0 | 1 | −3.0 | −6.0 |
| 10 | 0 | 1 | 0 | 1 | 0 | −2.5 | −5.0 |
| 11 | 0 | 1 | 0 | 1 | 1 | −2.0 | −4.0 |
| 12 | 0 | 1 | 1 | 0 | 0 | −1.5 | −3.0 |
| 13 | 0 | 1 | 1 | 0 | 1 | −1.0 | −2.0 |
| 14 | 0 | 1 | 1 | 1 | 0 | −0.5 | −1.0 |
| 15 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 16 | 1 | 0 | 0 | 0 | 0 | +0.5 | +1.0 |
| 17 | 1 | 0 | 0 | 0 | 1 | +1.0 | +2.0 |
| 18 | 1 | 0 | 0 | 1 | 0 | +1.5 | +3.0 |
| 19 | 1 | 0 | 0 | 1 | 1 | +2.0 | +4.0 |
| 20 | 1 | 0 | 1 | 0 | 0 | +2.5 | +5.0 |
| 21 | 1 | 0 | 1 | 0 | 1 | +3.0 | +6.0 |
| 22 | 1 | 0 | 1 | 1 | 0 | +3.5 | +7.0 |
| 23 | 1 | 0 | 1 | 1 | 1 | +4.0 | +8.0 |
| 24 | 1 | 1 | 0 | 0 | 0 | +4.5 | +9.0 |
| 25 | 1 | 1 | 0 | 0 | 1 | +5.0 | +10.0 |
| 26 | 1 | 1 | 0 | 1 | 0 | +5.5 | +11.0 |
| 27 | 1 | 1 | 0 | 1 | 1 | +6.0 | +12.0 |
| 28 | 1 | 1 | 1 | 0 | 0 | +6.5 | +13.0 |
| 29 | 1 | 1 | 1 | 0 | 1 | +7.0 | +14.0 |
| 30 | 1 | 1 | 1 | 1 | 0 | +7.5 | +15.0 |
| 31 | 1 | 1 | 1 | 1 | 1 | +8.0 | +16.0 |

The TX and RX audio signal paths each have a programmable gain block. If a TX or RX voltage gain other than the nominal power-up default is desired, it can be programmed via the microcontroller interface. The gain blocks can be used during final test of the radio to electronically adjust for gain tolerances in the radio system. The RX and TX gain have steps of 0.5 dB covering a dynamic range from −7.5 dB to +8 dB. At the earpiece output, the RX gain steps are multiplied by 2 due to the expander slope. The volume control feature for the earpiece amplifier allows for compensation of gain tolerances from −15 dB to +16 dB. Volume control is preferably done on the earpiece amplifier (bits EARP_VOL[1:0]).



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**Table 10. PLL center frequency calibration**

| Select | FM_PLL_VCO[4:0] | | | | | Center frequency shift (MHz) |
|---|---|---|---|---|---|---|
| | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | +3.0 |
| 1 | 0 | 0 | 0 | 0 | 1 | +2.8 |
| 2 | 0 | 0 | 0 | 1 | 0 | +2.6 |
| 3 | 0 | 0 | 0 | 1 | 1 | +2.4 |
| 4 | 0 | 0 | 1 | 0 | 0 | +2.2 |
| 5 | 0 | 0 | 1 | 0 | 1 | +2.0 |
| 6 | 0 | 0 | 1 | 1 | 0 | +1.8 |
| 7 | 0 | 0 | 1 | 1 | 1 | +1.6 |
| 8 | 0 | 1 | 0 | 0 | 0 | +1.4 |
| 9 | 0 | 1 | 0 | 0 | 1 | +1.2 |
| 10 | 0 | 1 | 0 | 1 | 0 | +1.0 |
| 11 | 0 | 1 | 0 | 1 | 1 | +0.8 |
| 12 | 0 | 1 | 1 | 0 | 0 | +0.6 |
| 13 | 0 | 1 | 1 | 0 | 1 | +0.4 |
| 14 | 0 | 1 | 1 | 1 | 0 | +0.2 |
| 15 | 0 | 1 | 1 | 1 | 1 | 0 |
| 16 | 1 | 0 | 0 | 0 | 0 | −0.2 |
| 17 | 1 | 0 | 0 | 0 | 1 | −0.4 |
| 18 | 1 | 0 | 0 | 1 | 0 | −0.6 |
| 19 | 1 | 0 | 0 | 1 | 1 | −0.8 |
| 20 | 1 | 0 | 1 | 0 | 0 | −1.0 |
| 21 | 1 | 0 | 1 | 0 | 1 | −1.2 |
| 22 | 1 | 0 | 1 | 1 | 0 | −1.4 |
| 23 | 1 | 0 | 1 | 1 | 1 | −1.6 |
| 24 | 1 | 1 | 0 | 0 | 0 | −1.8 |
| 25 | 1 | 1 | 0 | 0 | 1 | −2.0 |
| 26 | 1 | 1 | 0 | 1 | 0 | −2.2 |
| 27 | 1 | 1 | 0 | 1 | 1 | −2.4 |
| 28 | 1 | 1 | 1 | 0 | 0 | −2.6 |
| 29 | 1 | 1 | 1 | 0 | 1 | −2.8 |
| 30 | 1 | 1 | 1 | 1 | 0 | −3.0 |
| 31 | 1 | 1 | 1 | 1 | 1 | −3.2 |

This programming allows calibration of the center frequency of the VCO within the FM PLL to align the frequency as close as possible to the nominal 10.7 MHz frequency.



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## 8.2 Data register 1

**Table 11. Data register 1 (address 001h) bit description**

*Legend: * reset value.*

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 15 to 10 | RX_PRE[5:0] | - | **RX prescaler** |
| 9 to 0 | RX_MDIV[9:0] | - | **RX main divider** |

## 8.3 Data register 2

**Table 12. Data register 2 (address 010h) bit description**

*Legend: * reset value.*

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 15 to 10 | reserved | 00 0000* | undefined; must always be set logic 0 |
| 9 to 0 | REF_DIV[9:0] | - | **Reference divider** |

## 8.4 Data register 3

**Table 13. Data register 3 (address 011h) bit description**

*Legend: * reset value.*

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 15 to 10 | TX_PRE[5:0] | - | **TX prescaler** |
| 9 to 0 | TX_MDIV[9:0] | - | **TX main divider** |

## 8.5 Data register 4

**Table 14. Data register 4 (address 100h) bit description**

*Legend: * reset value.*

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 15 | TM2 | 0* | **Test mode selection.** Test mode bits are only used for test in production and application tuning. Those bits have to be set to logic 0 for normal operation. See Table 22. |
| 14 | CLKO | 0* | **Clock output drive**. Depending on the microcontroller clock frequency and clock capacitive load, the output CLKO can be programmed to optimize current consumption. The clock output level is 1.5 V (p-p). Output CLKO is AC-coupled with pin XTALI of the microcontroller. The external resonator from the microcontroller is then removed. |
| | | 0* | 10 MHz at 10 pF |
| | | 1 | 10 MHz at 5 pF (or 5 MHz at 10 pF) |
| 13 | TM1 | 0* | **Test mode selection.** Test mode bits are only used for test in production and application tuning. Those bits have to be set to logic 0 for normal operation. See Table 22. |



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**Table 14. Data register 4 (address 100h) bit description** *...continued*

*Legend: * reset value.*

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 12 | DOUBLER | | **Voltage doubler.** The minimum supply voltage for the IC is 2.9 V which limits the voltage swing on both charge pumps to approximately 2.3 V. Using the voltage doubler or an external high supply voltage on pin VCP, allows the increased voltage range to enhance the tuning range of the VCO varicaps. To save current in Inactive mode, the voltage doubler clock frequency is the same as the CLKO clock (can be programmed to XTAL / 128); in Active mode, the voltage doubler clock is XTALI / 2. |
| | | 0* | doubler inactive |
| | | 1 | doubler active |
| 11 to 7 | TX_GAIN[4:0] | | **TX gain setting** |
| | | 01 1111* | for values, see Table 9 |
| 6 | TX_MU | | **TX channel mute** |
| | | 0 | not muted (normal operation) |
| | | 1* | muted |
| 5 | HD_LIM | | **Hard limiter** |
| | | 0* | disable |
| | | 1 | enable |
| 5 | ALC | | **Automatic level control** |
| | | 0* | enable (normal operation) |
| | | 1 | disable |
| 3 | XTAL | | **Crystal oscillator** |
| | | 0 | on |
| | | 1* | off |
| 2 | RX_MU | | **RX channel mute** |
| | | 0 | not muted (normal operation) |
| | | 1* | muted |
| 1 | DEM_FIL | | **Demodulator filter.** An internal programmable filter limits the demodulator bandwidth. The –3 dB cut-off frequency is selected with this bit. The wider bandwidth provides a solution for audio and sub-audio digital applications. |
| | | 0* | 7 kHz |
| | | 1 | 100 kHz |
| 0 | reserved | 0* | undefined, must always be set to logic 0 |



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## 8.6 Data register 5

**Table 15. Data register 5 (address 101h) bit description**

*Legend: * reset value.*

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 15 | REG | | **Internal voltage regulator** |
| | | 0 | disable and tied to supply voltage $V_{CC}$ (in Inactive mode) |
| | | 1* | enable |
| 14 | MODE[1:0] | | **Active mode selection.** See details in Table 4 “Activated blocks”. |
| | | 00* | Inactive mode |
| | | 01 | Inactive mode |
| | | 10 | RX mode |
| | | 11 | Active mode |
| 13 | XTAL_H | | **Crystal high current.** In Inactive mode, the crystal oscillator is a major contributor to the full current consumption. |
| | | 0 | save current operation yields a full current consumption in Inactive mode at 230 μA; see details in Section 7.1.3 “Control bits in power saving modes” |
| | | 1* | crystal oscillator current is increased by 100 μA |
| 11 to 7 | CAR_DET_LEV[4:0] | | **Carrier detection threshold programming**. When bit BAT_DET = 0, the carrier detector is enabled and the signal *Carrier detection* is routed to the output pin CDLBD. If RSSI is above the programmed RSSI level, pin CDLBD = LOW; if not then pin CDLBD = HIGH. The carrier detector gives an indication if a carrier signal is present on the selected channel. The nominal value and tolerance of the carrier detection threshold is given in the carrier detector specification. If a different carrier detection threshold value is desired, it can be programmed through the microcontroller interface. To scale the carrier detection range, connect an external resistor from pin RSSI to ground. The value 1 0011 corresponds to RSSI = 0.86 V (typical DC value). |
| | | 0 0000* | For values, see Table 16 |
| 6 to 4 | L_BAT_DET[2:0] | | **Low battery detector voltage**. When bit BAT_DET = 1, the low battery detector is enabled and the signal *BDout* is routed to the output pin CDLBD. If the supply voltage is below the programmed level, pin CDLBD = LOW and if not, pin CDLBD = $V_{CC}$. |
| | | 000* | 3.5 V |
| | | 001 | 3.4 V |
| | | 010 | 3.3 V |
| | | 011 | 3.2 V |
| | | 100 | 3.1 V |
| | | 101 | 3.0 V |
| | | 110* | 2.9 V |
| | | 111 | 2.8 V |



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**Table 15. Data register 5 (address 101h) bit description** *...continued*

*Legend: * reset value.*

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 3 | BAT_DET | | **Battery detection** |
| | | 0 | disable |
| | | 1* | enable |
| 2 to 0 | CLK_DIV[2:0] | | **Clock output divider.** The *Clockout* signal is derived from the crystal oscillator and is used to drive a microcontroller (bit CLKO). The crystal signal is divided down with a programmable divider value. To supply the clock to the microcontroller and save current in the handset, an external low power resonator may be used and with the clock output disable (bits CLK_DIV[2:0] = 000) as well as the crystal oscillator not active (bit XTAL = 1). In Power-saving mode, the divider ratio is programmed down to 128 to reduce the microcontroller power consumption. |
| | | 100* | for values, see Table 17 |

**Table 16. Carrier detection**

| Select | CAR_DET_LEV[4:0] | | | | | RSSI threshold detection voltage (V) |
|---|---|---|---|---|---|---|
| | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0.1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 0.14 |
| 2 | 0 | 0 | 0 | 1 | 0 | 0.18 |
| 3 | 0 | 0 | 0 | 1 | 1 | 0.22 |
| 4 | 0 | 0 | 1 | 0 | 0 | 0.26 |
| 5 | 0 | 0 | 1 | 0 | 1 | 0.3 |
| 6 | 0 | 0 | 1 | 1 | 0 | 0.34 |
| 7 | 0 | 0 | 1 | 1 | 1 | 0.38 |
| 8 | 0 | 1 | 0 | 0 | 0 | 0.42 |
| 9 | 0 | 1 | 0 | 0 | 1 | 0.46 |
| 10 | 0 | 1 | 0 | 1 | 0 | 0.5 |
| 11 | 0 | 1 | 0 | 1 | 1 | 0.54 |
| 12 | 0 | 1 | 1 | 0 | 0 | 0.58 |
| 13 | 0 | 1 | 1 | 0 | 1 | 0.62 |
| 14 | 0 | 1 | 1 | 1 | 0 | 0.66 |
| 15 | 0 | 1 | 1 | 1 | 1 | 0.7 |
| 16 | 1 | 0 | 0 | 0 | 0 | 0.74 |
| 17 | 1 | 0 | 0 | 0 | 1 | 0.78 |
| 18 | 1 | 0 | 0 | 1 | 0 | 0.82 |
| 19 | 1 | 0 | 0 | 1 | 1 | 0.86 |
| 20 | 1 | 0 | 1 | 0 | 0 | 0.9 |
| 21 | 1 | 0 | 1 | 0 | 1 | 0.94 |
| 22 | 1 | 0 | 1 | 1 | 0 | 0.98 |
| 23 | 1 | 0 | 1 | 1 | 1 | 1.02 |



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**Table 16. Carrier detection** *…continued*

| Select | CAR_DET_LEV[4:0] | | | | | RSSI threshold detection voltage (V) |
|---|---|---|---|---|---|---|
| | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| 24 | 1 | 1 | 0 | 0 | 0 | 1.06 |
| 25 | 1 | 1 | 0 | 0 | 1 | 1.1 |
| 26 | 1 | 1 | 0 | 1 | 0 | 1.14 |
| 27 | 1 | 1 | 0 | 1 | 1 | 1.18 |
| 28 | 1 | 1 | 1 | 0 | 0 | 1.22 |
| 29 | 1 | 1 | 1 | 0 | 1 | 1.26 |
| 30 | 1 | 1 | 1 | 1 | 0 | 1.3 |
| 31 | 1 | 1 | 1 | 1 | 1 | 1.34 |

**Table 17. Clock output divider**

| Select | CLK_DIV[2:0] | | | Clock divider ratio |
|---|---|---|---|---|
| | Bit 2 | Bit 1 | Bit 0 | |
| 1 | 0 | 0 | 0 | output disable |
| 2 | 0 | 0 | 1 | 2 |
| 3 | 0 | 1 | 0 | 2.5 |
| 4 | 0 | 1 | 1 | 4 |
| 5 | 1 | 0 | 0 | 1 |
| 6 | 1 | 1 | 1 | 128 |

## 8.7 Data register 6

**Table 18. Data register 6 (address 110h) bit description**

*Legend: * reset value.*

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 15 to 13 | PA_OUT[2:0] | | **Power amplifier output level.** The power amplifier uses 2 bits to modify the output power. The PA is disabled for value 000. Duplexer matching from 300 Ω to 50 Ω is implemented with a parallel inductor and series C network. To get the power at the antenna, the duplexer insertion loss should be subtracted. At maximum power, the DC current consumption is increased by 3 mA over the minimum power current consumption. |
| | | 010* | The output power for a 50 Ω termination is specified in Table 20. |
| 12 | TX_CP | | **TX charge pump current**. The performance of the PLL can be improved by increasing charge pump current. |
| | | 0* | 400 µA |
| | | 1 | 800 µA |
| 11 | RX_CP | | **RX charge pump current**. The performance of the PLL can be improved by increasing charge pump current. |
| | | 0* | 400 µA |
| | | 1 | 800 µA |



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**Table 18. Data register 6 (address 110h) bit description** *...continued*

*Legend: * reset value.*

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 10 to 8 | REG_ADJ[2:0] | | **Voltage regulator adjustment.** An internal 1.5 V band gap voltage reference provides the voltage reference for the low battery detector circuits, the VREG regulator voltage, the VB reference voltage and all internal analog references. In Inactive mode, the adjustment is disabled. |
| | | 011* | for values, see Table 21 |
| 7 to 6 | EXP[1:0] | | **Expander noise level control.** Depending on the application noise floor specification, a noise level control can be applied. |
| | | 00* | expander disabled |
| | | 11 | expander maximum value |
| 5 | TM0 | 0* | **Test mode selection.** Test mode bits are only used for test in production and application tuning. Those bits have to be set to logic 0 for normal operation. See Table 22. |
| 4 | reserved | 0* | undefined; must always be set to logic 0 |
| 3 to 0 | XTAL_TUN[3:0] | | **Crystal tuning capacitors.** An on-chip crystal reference tuning is provided to compensate for frequency spread over process and temperature. The value of the external capacitor on pin XTALI is chosen to be around 3 pF lower than on pin XTALO. Internally, a programmable capacitance is in parallel with pin XTALI. Tuning capacitance values are in the range of 0 pF to 4.5 pF. |
| | | 0111* | for values, see Table 19 |

**Table 19. Crystal tuning capacitance**

| Select | XTAL_TUN[3:0] | | | | Capacitance (pF) |
|---|---|---|---|---|---|
| | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| 0 | 0 | 0 | 0 | 0 | 0.2 |
| 1 | 0 | 0 | 0 | 1 | 0.5 |
| 2 | 0 | 0 | 1 | 0 | 0.8 |
| 3 | 0 | 0 | 1 | 1 | 1.1 |
| 4 | 0 | 1 | 0 | 0 | 1.4 |
| 5 | 0 | 1 | 0 | 1 | 1.7 |
| 6 | 0 | 1 | 1 | 0 | 2.0 |
| 7 | 0 | 1 | 1 | 1 | 2.3 |
| 8 | 1 | 0 | 0 | 0 | 2.6 |
| 9 | 1 | 0 | 0 | 1 | 2.9 |
| 10 | 1 | 0 | 1 | 0 | 3.2 |
| 11 | 1 | 0 | 1 | 1 | 3.5 |
| 12 | 1 | 1 | 0 | 0 | 3.8 |
| 13 | 1 | 1 | 0 | 1 | 4.1 |
| 14 | 1 | 1 | 1 | 0 | 4.4 |
| 15 | 1 | 1 | 1 | 1 | 4.7 |



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**Table 20. Power amplifier output**

| Select | PA_OUT[2:0] | | | Power amplifier | | | |
|---|---|---|---|---|---|---|---|
| | Bit 2 | Bit 1 | Bit 0 | Output power (dBm) | Second harmonic (dBm) | Third harmonic (dBm) | Fourth harmonic (dBm) |
| - | 0 | X | X | PA inactive | - | - | - |
| 0 | 1 | 0 | 0 | 1.0 | –17 | –27 | –34 |
| 1 | 1 | 0 | 1 | 1.9 | –19 | –29 | –34 |
| 2 | 1 | 1 | 0 | 2.5 | –23 | –33 | –36 |
| 3 | 1 | 1 | 1 | 3.0 | –26 | –36 | –40 |

**Table 21. Voltage reference adjust**

| Select | REG_ADJ[2:0] | | | Nominal voltage reference |
|---|---|---|---|---|
| | Bit 2 | Bit 1 | Bit 0 | |
| 0 | 0 | 0 | 0 | –7 % |
| 1 | 0 | 0 | 1 | –5 % |
| 2 | 0 | 1 | 0 | –3 % |
| 3 | 0 | 1 | 1 | –1 % |
| 4 | 1 | 0 | 0 | +1 % |
| 5 | 1 | 0 | 1 | +3 % |
| 6 | 1 | 1 | 0 | +5 % |
| 7 | 1 | 1 | 1 | +7 % |

**Table 22. Test mode**

| TM2 | TM1 | TM0 | Select |
|---|---|---|---|
| 0 | 0 | 0 | normal operation |
| 0 | 0 | 1 | up or down RX |
| 0 | 1 | 0 | up or down TX |
| 0 | 1 | 1 | up or down RX or TX |
| 1 | 0 | 0 | reference divider output divided by 2 |
| 1 | 0 | 1 | prescaler and main divider RX divided by 2 |
| 1 | 1 | 0 | prescaler and main divider TX divided by 2 |
| 1 | 1 | 1 | double synthesizers charge pump are in 3-state |

Out-of-lock of synthesizers RX or TX can be indirectly monitored on pin CDLBD: the width of the ‘glitch’ gives a direct measure of the phase error on the PLL RX and/or PLL TX.

To tune the external RX and TX VCO inductors, a defined divider ratio has to be programmed on the dividers, and then the image of the VCO frequency can be read on pin CDLBD.

It can also be used to check the divider ratio: force a frequency on VCO or crystal pins and read the programmed frequency on pin CDLBD.

Before pin CDLBD, there is a divide-by-2, then all frequencies are divided by 2. When charge pumps are in 3-state, the VCOs can be measured in stand-alone.



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# 9. Limiting values

**Table 23. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | –0.3 | +6.0 | V |
| $T_{stg}$ | storage temperature | | –55 | +125 | °C |

# 10. Thermal characteristics

**Table 24. Thermal characteristics**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | 68 | K/W |

# 11. Characteristics

**Table 25. Supplies**

*$V_{CC}$ = 3.3 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 2.9 | 3.3 | 5.5 | V |
| $T_{amb}$ | ambient temperature | | –40 | +25 | +85 | °C |

**Table 26. Receiver part**

*$V_{CC}$ = 3.3 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Low noise amplifier and image reject mixer ($f_o$ = 903 MHz)** | | | | | | | |
| Input: pins RFIX and RFIY | | | | | | | |
| $R_{i(RF)}$ | RF input resistance | real part of the parallel input impedance; balanced; indicative value | | - | 110 | - | Ω |
| $C_{i(RF)}$ | RF input capacitance | imaginary part of the parallel input impedance; balanced; indicative value | | - | 0.7 | - | pF |
| $f_{i(RF)}$ | RF input frequency | | | 902 | 903 | 928 | MHz |
| LNA | | | | | | | |
| $\lvert s_{11(RF)}\rvert^2$ | RF input return loss | | [1] | 10 | - | - | dB |
| $G_{p(conv)}$ | conversion power gain | from balun input to pin MIXO matched to 330 Ω | | - | 22 | - | dB |
| $ICP_{1dB}$ | 1 dB input compression point | | [1] | - | –23 | - | dBm |
| IP3 | third-order intercept point | | | - | –13 | - | dBm |
| NF | noise figure | overall RF front-end (does not include the IF section) | | - | 4 | 5 | dB |
| $\alpha_{f(image)}$ | image frequency rejection | in band of interest | | 26 | 45 | - | dB |



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**Table 26. Receiver part** *...continued*

*$V_{CC}$ = 3.3 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Output: pin MIXO | | | | | | | |
| $R_L$ | load resistance | indicative value of IF resistive output load | | - | 330 | - | Ω |
| $C_L$ | load capacitance | indicative value of IF capacitive output load | | - | - | 3 | pF |
| **IF amplifier section ($f_o$ = 10.7 MHz)** | | | | | | | |
| G | gain | SFS = 0 | [2] | - | 43 | - | dB |
| | | SFS = 1; measured at amplifier output | [2] | | | | |
| | | first IF amplifier | | - | 22.5 | - | dB |
| | | second IF amplifier | | - | 25 | - | dB |
| NF | noise figure | IF amplifier | | - | 7.5 | - | dB |
| | | first IF amplifier | [2] | - | 7 | - | dB |
| | | second IF amplifier | [2] | - | 14 | - | dB |
| **PLL demodulator ($f_o$ = 10.7 MHz; Δf = ±25 kHz; $f_{mod}$ = 1 kHz)** | | | | | | | |
| $B_{-3dB(demod)}$ | demodulator −3 dB bandwidth | DEM_FIL = 0; loop filter: 4.7 kΩ, 1.8 nF and 150 pF | | - | 7 | - | kHz |
| | | DEM_FIL =1; loop filter: 15 kΩ, 150 pF and 12 pF | | - | 100 | - | kHz |
| VCO | | | | | | | |
| $f_{VCO}$ | VCO frequency | VCO center frequency (free running); open loop; all conditions | | 7.0 | 10.7 | 15.0 | MHz |
| Δf | frequency deviation | | | - | - | ±75 | kHz |
| $\Delta f_{VCO}/\Delta V_{VCO}$ | VCO frequency change to VCO voltage change ratio | after calibration | | - | 760 | - | kHz/V |
| $f_{VCO(step)}$ | VCO frequency step | | | - | 200 | - | kHz |
| $N_{step(f_VCO)}$ | number of VCO frequency steps | | | - | 32 | - | |
| Output: pin DETO | | | | | | | |
| $R_L$ | load resistance | | | 5 | - | - | kΩ |
| $V_{o(RMS)}$ | RMS output voltage | TX mode; $R_L$ = 10 kΩ; amplifier gain G = 10 | [3] | - | 100 | 350 | mV |
| $V_O$ | output voltage | adjust with microcontroller | | 1.2 | 1.4 | 1.6 | V |



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**Table 26. Receiver part** *...continued*

*$V_{CC}$ = 3.3 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **FM receiver system characteristics** | | | | | | |
| Conditions: $f_o$ = 903 MHz; Δf = ±25 kHz; $f_{mod}$ = 1 kHz; DEM_F = 0; pin EARO: $R_L$ = 150 Ω in series with 10 µF (all with ITU-T filter) | | | | | | |
| $S_{RX}$ | receiver sensitivity | measured at antenna with 3 dB duplexer insertion loss; B = 100 kHz | | | | |
| | | RX mode; input level for 9 dB SINAD | - | –115 | - | dBm |
| | | TX mode; PA = 10; $V_{EARO}$ = 200 mV (RMS); minimum TX-to-RX duplexer isolation = 35 dB | - | –113.5 | - | dBm |
| S/N | signal-to-noise ratio | $V_{i(RF)}$ = –80 dBm and –40 dBm; TX mode; PA_OUT[2:0] = 10; CLKO off; $V_{EARO}$ = 200 mV (RMS) | 25 | 38 | - | dB |
| THD | total harmonic distortion | at Δf = ±60 kHz (without ITU-T filter); $V_{i(RF)}$ = –80 dBm and –40 dBm; TX mode; PA_OUT[2:0] = 10; CLKO off; $V_{EARO}$ = 500 mV (RMS) | - | 0.6 | 2 | % |
| **RSSI or carrier detection: $V_{VB}$ = 1.5 V** | | | | | | |
| $I_{o(dyn)}$ | dynamic output current | on pin RSSI | - | 68 | - | dB |
| $N_{step(th)(cd)}$ | number of carrier detect threshold steps | programmable through microcontroller | - | 32 | - | |
| $V_{det}$ | detection voltage | | 0.05 | - | 1.6 | V |
| $V_{hys}$ | hysteresis voltage | | - | 45 | - | mV |
| $V_{det(step)}$ | detection voltage step | | - | 40 | - | mV |
| Output: pin RSSI | | | | | | |
| $R_{int}$ | internal resistance | measured between pin RSSI and $V_{CC}$ | - | 175 | - | kΩ |
| Output: pin CDLBD | | | | | | |
| $V_{OH}$ | HIGH-level output voltage | $V_{i(limiter)}$ = 0 mV (RMS); RSSI threshold level = 0.86 V | $0.9V_{CC}$ | - | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_{i(limiter)}$ = 100 mV (RMS); RSSI threshold level = 0.86 V | - | - | $0.1V_{CC}$ | V |
| **Data comparator** | | | | | | |
| Input: pin DATAI | | | | | | |
| $V_{i(p-p)}$ | peak-to-peak input voltage | | 100 | - | - | mV |
| $V_{hys(i)}$ | input hysteresis voltage | | 25 | 40 | 75 | mV |
| $V_{th}$ | threshold voltage | | - | $V_{CC}$ – 0.9 | - | V |
| $Z_i$ | input impedance | | 150 | 240 | - | kΩ |
| Output: pin DATAO | | | | | | |
| $V_{OH}$ | HIGH-level output voltage | $V_{DATAI} = V_{CC} – 1.4$ V | $0.9V_{CC}$ | - | - | V |



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**Table 26. Receiver part** *...continued*

*$V_{CC}$ = 3.3 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | LOW-level output voltage | $V_{DATAI} = V_{CC} - 0.4$ V | | - | - | $0.1V_{CC}$ | V |
| $I_{O(sink)}$ | output sink current | $V_{DATAI} = V_{CC} - 0.4$ V; $V_{DATAO} = 0.1V_{CC}$ | | - | 50 | - | µA |
| **RX voltage controlled oscillator** | | | | | | | |
| $f_{VCO}$ | VCO frequency | free running | [1] | - | 910 | - | MHz |
| $\Delta f_{VCO}/\Delta V_{VCO}$ | VCO frequency change to VCO voltage change ratio | $L_{ext}$ = 4.7 nH at 890 MHz; $L_{ext}$ = 3.9 nH at 935 MHz; control voltage | | | | | |
| | | $V_{RXLF}$ = 0.5 V | | - | 50 | - | MHz/V |
| | | $V_{RXLF}$ = 1.5 V | | - | 30 | - | MHz/V |
| $\varphi_n$ | phase noise | indicative value (cannot be directly measured | [4] | | | | |
| | | $f_{offset}$ = 1 kHz | | - | –58 | - | dBc/Hz |
| | | $f_{offset}$ = 10 kHz | | - | –82 | - | dBc/Hz |
| | | $f_{offset}$ = 100 kHz | | - | –102 | - | dBc/Hz |
| $Q_{min}$ | minimum quality factor | external inductor quality factor at 920 MHz; $L_{ext}$ = 3.9 nH | | 30 | - | - | |

[1] This specification will be measured and guaranteed only on the NXP Semiconductors SA58646 board.

[2] 330 Ω matched input and output.

[3] The level on pin RXAI will be higher in RX mode than in TX mode.

[4] Conditions: carrier = 892.3 MHz; $L_{ext}$ = 4.7 nH (3.9 nH for 935 MHz operation); loop filter: C1 = 3.9 nF; R2 = 6.8 kΩ; C2 = 47 nF (see application note).

**Table 27. Transmitter part**

*$V_{CC}$ = 3.3 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Summator amplifier** | | | | | | | |
| Input: pin MODI | | | | | | | |
| $V_{bias}$ | bias voltage | | | - | 2.2 | - | V |
| Output: pin MODO | | | | | | | |
| $V_{o(p-p)}$ | peak-to-peak output voltage | | | - | 94 | 240 | mV |
| $R_{fbck}$ | feedback resistance | between pins MODI and MODO | | 10 | - | - | kΩ |
| **TX voltage controlled oscillator** | | | | | | | |
| $f_{VCO}$ | VCO frequency | free running | [1] | - | 910 | - | MHz |
| $\Delta f_{VCO}/\Delta V_{VCO}$ | VCO frequency change to VCO voltage change ratio | control voltage | | | | | |
| | | $V_{TXLF}$ = 0.5 V | | - | 50 | - | MHz/V |
| | | $V_{TXLF}$ = 1.5 V | | - | 25 | - | MHz/V |
| | | modulation voltage | | | | | |
| | | $V_{MODO}$ = 2.2 V | | - | 530 | - | kHz/V |



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**Table 27. Transmitter part** *…continued*

*$V_{CC}$ = 3.3 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $\varphi_n$ | phase noise | VCO TX plus PA; output power at 0 dB | [2] | | | | |
| | | $f_{offset}$ = 20 MHz | | –139 | –150 | - | dBc/Hz |
| | | $f_{offset}$ = 10 kHz | | - | –85 | - | dBc/Hz |
| | | $f_{offset}$ = 1 kHz | | - | –60 | - | dBc/Hz |
| $Q_{min}$ | minimum quality factor | external inductor quality factor at 902 MHz to 928 MHz; $L_{ext}$ = 3.9 nH | | 30 | - | - | |
| **Power amplifier** | | | | | | | |
| $P_o$ | output power | subtract duplexer insertion loss to get power on antenna; see Table 20 | [3] | - | 3 | - | dBm |
| $\Delta P_o$ | output power variation | see Table 20 | [3] | - | 2 | - | dB |
| $N_{step(G_adj)}$ | number of gain adjustment steps | software control | | - | 4 | - | |
| **Transmit system** | | | | | | | |
| THD | total harmonic distortion | measured after demodulation; $V_{MODO}$ for demodulated $\Delta f$ = ±60 kHz; measured with ITU-T filter | | - | 1 | 2 | % |
| $P_{sp}$ | spurious output power | RX VCO spurious emission on PA output versus output power | [1] | - | –45 | - | dBc |

[1] This specification will be measured and guaranteed only on the NXP Semiconductors SA58646 board.

[2] TX-to-RX duplexer isolation = 35 dB; carrier = 925.6 MHz; $L_{ext}$ = 3.9 nH (for both base and handset); loop filter: C1 = 470 nF, R2 = 1.8 kΩ and C2 = 4.7 µF (see application note).

[3] Load: R = 50 Ω; $L_p$ = 22 nH; $C_s$ = 1.6 pF.

**Table 28. Synthesizer**

*$V_{CC}$ = 3.3 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Crystal oscillator; external capacitors on pins XTALO = 8.2 pF and XTALI = 5.6 pF (indicative)** | | | | | | |
| $f_{xtal}$ | crystal frequency | reference input frequency | 4 | 10.24 | 20 | MHz |
| $C_{i(XTALI)}$ | input capacitance on pin XTALI | indicative; XTAL_TUN[3:0] = 8 | - | 4 | - | pF |
| $C_{i(XTALO)}$ | input capacitance on pin XTALO | indicative | - | 1.5 | - | pF |
| $C_{tune(xtal)}$ | crystal tuning capacitance | on pin XTALI | - | 4.5 | - | pF |
| $N_{step(C_tune)}$ | number of tuning capacitance steps | XTAL_TUN[3:0] | - | 16 | - | |
| **Clock divider** | | | | | | |
| $D/D_{clk}$ | clock divider ratio | CLK_DIV[2:0] | 1 | - | 128 | |
| $t_{sw}$ | switching time | from one frequency f1 to frequency f2 | - | 2 / f2 | - | s |
| Output: pin CLKO | | | | | | |
| $C_L$ | load capacitance | external load | - | - | 20 | pF |



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**Table 28. Synthesizer** *...continued*

*$V_{CC}$ = 3.3 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{o(p-p)}$ | peak-to-peak output voltage | CLKO = 1; 10 MHz at 5 pF (or 5 MHz at 10 pF) | - | 1.5 | - | V |
| | | CLKO = 0; 10 MHz at 10 pF | - | 1.5 | - | V |
| **10-bit reference divider** | | | | | | |
| $D/D_{ref}$ | reference divider ratio | REF_DIV[9:0] | 8 | - | 1023 | |
| **TX and RX prescaler and main dividers** | | | | | | |
| $f_{i(RF)}$ | RF input frequency | | 902 | 903 | 928 | MHz |
| $D/D_{main}$ | main divider ratio | RX_MDIV[9:0]; TX_MDIV[9:0] | 8 | - | 1023 | |
| $D/D_{ps}$ | prescaler divider ratio | RX_PRE[5:0]; TX_PRE[5:0] | 64 | - | 127 | |
| **RX and TX charge pump: pins RXPD and TXPD** | | | | | | |
| $I_{o(cp)}$ | charge pump output current | RX_CP = 0; TX_CP = 0 | - | ±400 | - | µA |
| | | RX_CP = 1; TX_CP = 1 | - | ±800 | - | µA |
| $C_o$ | output capacitance | | - | - | 8 | pF |
| **Voltage doubler** | | | | | | |
| $V_{O(VCP)}$ | output voltage on pin VCP | DOUBLER = 1; $V_{CC}$ = 3 V | - | 5.2 | - | V |

**Table 29. RX baseband**

*$V_{CC}$ = 3.3 V; $T_{amb}$ = 25 °C; see Figure 6.*

*$V_{VB}$ = 1.5 V; $f_i$ = 1 kHz; RX gain set for 0 dB gain at −20 dBV on pin RXAI; earpiece volume at +4.7 dB; 560 pF between pins EARI and EARO; 150 Ω in series with 10 µF on pin EARO; all measured with a ITU-T filter except THD; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **RX audio path: RX gain adjust, mute and expander** | | | | | | | |
| THD | total harmonic distortion | $V_{RXAI}$ = −20 dBV | | - | 0.2 | 2 | % |
| $NF_M$ | peak noise figure | B = 300 Hz to 3.4 kHz | | - | −83 | - | dBV |
| Input: pin RXAI | | | | | | | |
| $V_{i(max)}$ | maximum input voltage | THD < 4 % | | - | 13 | - | dBV |
| $Z_i$ | input impedance | in TX mode | [1] | - | 15 | - | kΩ |
| | | in RX mode | [1] | 100 | - | - | kΩ |
| RX audio gain adjust | | | | | | | |
| $\Delta G_{adj}$ | gain adjustment range | RX_GAIN[4:0] | | | | | |
| | | on RX gain amplifier | | −7.5 | - | +8 | dB |
| | | on pin EARO | | −15 | - | +16 | dB |
| $N_{step(G_adj)}$ | number of gain adjustment steps | | | - | 32 | - | |
| $\alpha_{mute}$ | mute attenuation | $V_{RXAI}$ = −20 dBV | | - | −70 | −60 | dB |
| Expander | | | | | | | |
| $G_{expdr}$ | expander gain | $V_{RXAI}$ = −20 dBV | | −1 | 0 | +1 | dB |



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**Table 29. RX baseband** *...continued*

*$V_{CC}$ = 3.3 V; $T_{amb}$ = 25 °C; see Figure 6.*
*$V_{VB}$ = 1.5 V; $f_i$ = 1 kHz; RX gain set for 0 dB gain at −20 dBV on pin RXAI; earpiece volume at +4.7 dB; 560 pF between pins EARI and EARO; 150 Ω in series with 10 µF on pin EARO; all measured with a ITU-T filter except THD; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $\Delta G_{expdr}$ | expander gain change | referenced to $V_{RXAI}$ = −20 dBV with RX baseband audio noise tuning [2] | | | | |
| | | $V_{RXAI}$ = −30 dBV | −24 | −20 | −18 | dB |
| | | $V_{RXAI}$ = −35 dBV | −37 | −30 | −26 | dB |
| | | $V_{RXAI}$ = −45 dBV | - | −47 | −45 | dB |
| $t_{att(expdr)}$ | expander attack time | $C_{ECAP}$ = 0.47 µF | - | 2.0 | - | ms |
| $t_{rel(expdr)}$ | expander release time | $C_{ECAP}$ = 0.47 µF | - | 5.0 | - | ms |
| $\alpha_{ct(compr-expdr)}$ | compressor to expander crosstalk attenuation | from pins CMPI to EARO; $V_{CMPI}$ = −20 dBV; $V_{RXAI}$ = 0 V (RMS) | - | 80 | - | dB |
| $V_{o(max)}$ | maximum output voltage | indicative value; THD < 4 % | - | −7 | - | dBV |
| **Earpiece amplifier** | | | | | | |
| $G_{ctrl(dyn)}$ | dynamic gain control | | 13 | 14 | 15 | dB |
| $G_{ctrl}$ | gain control | no external resistor or capacitor used | | | | |
| | | EARP_VOL[1:0] = 00 | −1 | 0 | +1 | dB |
| | | EARP_VOL[1:0] = 01 | 3.7 | 4.7 | 5.7 | dB |
| | | EARP_VOL[1:0] = 10 | 8.3 | 9.3 | 10.3 | dB |
| | | EARP_VOL[1:0] = 11 | 13 | 14 | 15 | dB |
| Output: pin EARO | | | | | | |
| $V_{o(p-p)}$ | peak-to-peak output voltage | THD < 4 % | - | 2.2 | - | V |
| $R_L$ | load resistance | to keep amplifier stability; $R_L$ in series with 10 µF | - | 150 | 100000 | Ω |

[1] Pin RXAI level will be higher in RX mode than in TX mode.

[2] With expander output noise level control tuned for −65 dBV (max) and maximum gain tolerance of −4 dB at −35 dBV. With a larger gain tolerance at −35 dBV, the typical output noise can be reduced by 10 dB. See application note.

**Table 30. TX baseband**

*$V_{CC}$ = 3.3 V; $T_{amb}$ = 25 °C; see Figure 8.*
*$V_{VB}$ = 1.5 V; $f_i$ = 1 kHz; TX gain set for +10 dB gain at −30 dBV on pin CMPI; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Microphone amplifier** | | | | | | |
| G | gain | | 0 | - | 34 | dB |
| Output: pin MICO | | | | | | |
| $V_{o(max)}$ | maximum output voltage | $R_L$ = 10 kΩ; THD < 0.2 % | −12 | - | - | dBV |
| **Input: pin CMPI** | | | | | | |
| $Z_i$ | input impedance | | - | 15 | - | kΩ |
| **Compressor** | | | | | | |
| G | gain | $V_{CMPI}$ = −30 dBV; ALC off; hard limiter enabled | 9 | 10 | 11 | dB |



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**Table 30. TX baseband** *...continued*

*$V_{CC}$ = 3.3 V; $T_{amb}$ = 25 °C; see Figure 8.*
*$V_{VB}$ = 1.5 V; $f_i$ = 1 kHz; TX gain set for +10 dB gain at –30 dBV on pin CMPI; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ΔG | gain deviation | referenced to $V_{CMPI}$ = –30 dBV | | | | |
| | | $V_{CMPI}$ = –10 dBV | 8 | 10 | 12 | dB |
| | | $V_{CMPI}$ = –50 dBV | –14 | –10 | –8 | dB |
| $G_{max}$ | maximum gain | $V_{CMPI}$ = –70 dBV | - | 23 | - | dB |
| THD | total harmonic distortion | $V_{CMPI}$ = –10 dBV; ALC off | - | 0.5 | 2 | % |
| $t_{att(compr)}$ | compressor attack time | $C_{CCAP}$ = 0.47 µF | - | 4.0 | - | ms |
| $t_{rel(compr)}$ | compressor release time | $C_{CCAP}$ = 0.47 µF | - | 8.0 | - | ms |
| **Hard limiter** | | | | | | |
| $V_{o(p-p)}$ | peak-to-peak output voltage | $V_{CMPI}$ = –4 dBV; ALC off; hard limiter enabled | - | 1.26 | - | V |
| **TX mute** | | | | | | |
| $\alpha_{mute}$ | mute attenuation | $V_{CMPI}$ = –10 dBV; ALC off | - | –70 | –60 | dB |
| **TX gain adjust** | | | | | | |
| $\Delta G_{adj}$ | gain adjustment range | RX_GAIN[4:0] | –7.5 | - | +8 | dB |
| $N_{step(G_adj)}$ | number of gain adjustment steps | | - | 32 | - | |
| **Output: pin TXO** | | | | | | |
| $\alpha_{ct(expdr-compr)}$ | expander to compressor crosstalk attenuation | from pins RXAI to TXO; $V_{RXAI}$ = –10 dBV; $V_{CMPI}$ = 0 V (RMS) | - | 65 | - | dB |
| $Z_o$ | output impedance | | - | 500 | - | Ω |
| $V_{o(max)}$ | maximum output voltage | ALC on | | | | |
| | | $V_{CMPI}$ = –12 dBV | - | –12.5 | - | dBV |
| | | $V_{CMPI}$ = –10 dBV | - | –12.3 | - | dBV |
| | | $V_{CMPI}$ = –2.5 dBV | - | –11.5 | - | dBV |

**Table 31. Other features**

*$V_{CC}$ = 3.3 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **PLL voltage regulator: pin VREG** | | | | | | | |
| $V_O$ | output voltage | voltage regulator disabled | | - | $V_{CC}$ | - | V |
| | | voltage regulator enabled | | | | | |
| | | before $V_{ref}$ adjustment or in Inactive mode | | 2.5 | 2.7 | 2.9 | V |
| | | after $V_{ref}$ adjustment | | 2.65 | 2.7 | 2.75 | V |
| $I_O$ | output current | $C_{VREG}$ = 1 µF | | - | - | 3 | mA |
| **Low battery detector: battery detection enabled** | | | | | | | |
| $V_{det}$ | detection voltage | L_BAT_DET[2:0] | | 2.8 | - | 3.5 | V |
| $V_{hys}$ | hysteresis voltage | | [1] | - | 18 | - | mV |
| $N_{step(V_det)}$ | number of detection voltage steps | | | - | 8 | - | |


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**Table 31. Other features** *...continued*

*$V_{CC}$ = 3.3 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $\Delta V_{CC}/V_{CC}$ | supply voltage variation to supply voltage ratio | battery voltage detection accuracy after $V_{ref}$ adjust; L_BAT_DET[2:0] = 010 ($V_{CC}$ = 3 V) | - | 0.5 | 5 | % |
| Output: pin CDLBD | | | | | | |
| $I_{OL}$ | LOW-level output current | | 20 | - | - | mA |
| $V_{OL}$ | LOW-level output voltage | $R_L$ = 470 kΩ | - | - | $0.1V_{CC}$ | V |
| $V_{OH}$ | HIGH-level output voltage | $R_L$ = 470 kΩ | $0.9V_{CC}$ | - | - | V |

[1] $V_{hys} = (V_{high} - V_{low}) \times \frac{V_{VB}}{V_{th}}$

**Table 32. Microcontroller serial interface**

*$V_{CC}$ = 3.3 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Input and output: pins DATA, CLK and EN** | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | - | - | 0.5 | V |
| $V_{IH}$ | HIGH-level input voltage | | $V_{VREG}$ / 1.5 | - | $V_{CC}$ | V |
| $I_{IL}$ | LOW-level input current | $V_{IL}$ = 0.3 V | –5 | - | - | mA |
| $I_{IH}$ | HIGH-level input current | $V_{IH} = V_{VREG} - 0.3$ V | - | - | 5 | mA |
| $C_i$ | input capacitance | | - | - | 8 | pF |
| **Timing (see Figure 10)** | | | | | | |
| $t_{su(CLK-EN)}$ | CLK to EN set-up time | 50 % of signals | 50 | - | - | ns |
| $t_{su(DATA-CLK)}$ | DATA to CLK set-up time | 50 % of signals | 50 | - | - | ns |
| $t_{h(EN-CLK)}$ | EN to CLK hold time | 50 % of signals | 50 | - | - | ns |
| $f_{clk}$ | clock frequency | | - | - | 3 | MHz |
| $t_{r(i)}$ | input rise time | at 10 % to 90 % on pins DATA, CLK and EN; | - | - | 50 | ns |
| $t_{f(i)}$ | input fall time | at 10 % to 90 % on pins DATA, CLK and EN; | - | - | 50 | ns |
| $t_{h(CLK-EN)}$ | CLK to EN hold time | at end of word | 100 | - | - | ns |
| $t_{w(EN)}$ | pulse width on pin EN | [1] | 1 / $f_{comp}$ | - | - | ns |
| $t_{startup(MCU)}$ | MCU start-up time | 90 % of $V_{VREG}$ to pins DATA, CLK and EN | - | - | 200 | µs |

[1] The minimum pulse width $t_{w(EN)}$ should be equal to the period time of the comparison frequency. The synthesizer ensures that the internal EN signal does not occur during a comparison phase to avoid any phase error jump. This time can be reduced to 100 ns for:

a) Clock divider programming

b) Synthesizer programming: only for words which do not influence the synthesizer (word 1, 2, 3)



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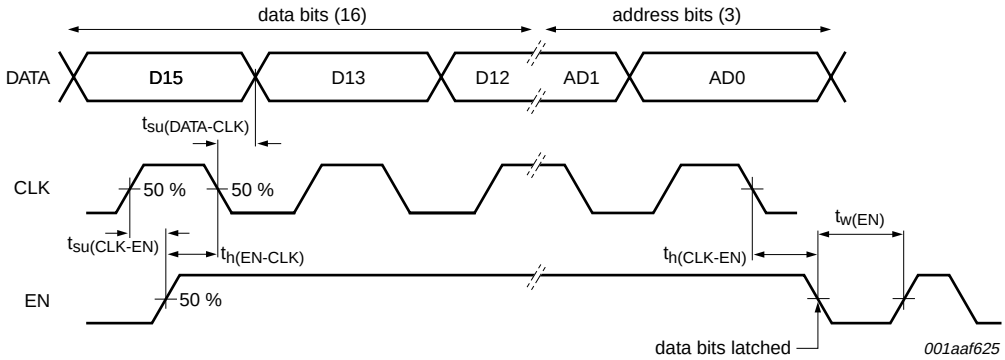



**Fig 10. Digital signal timing**

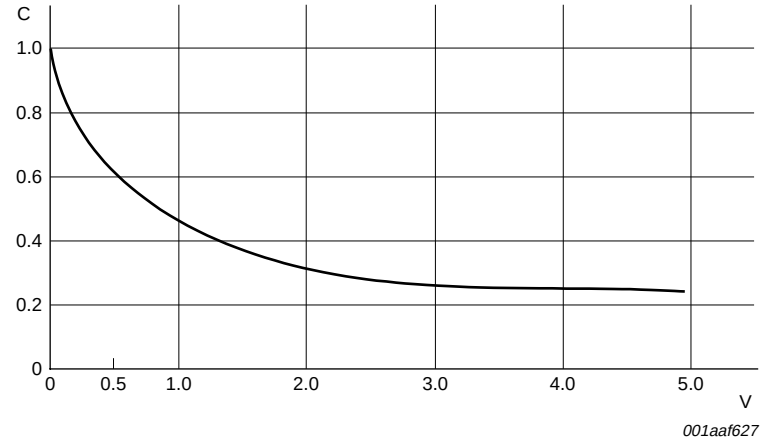


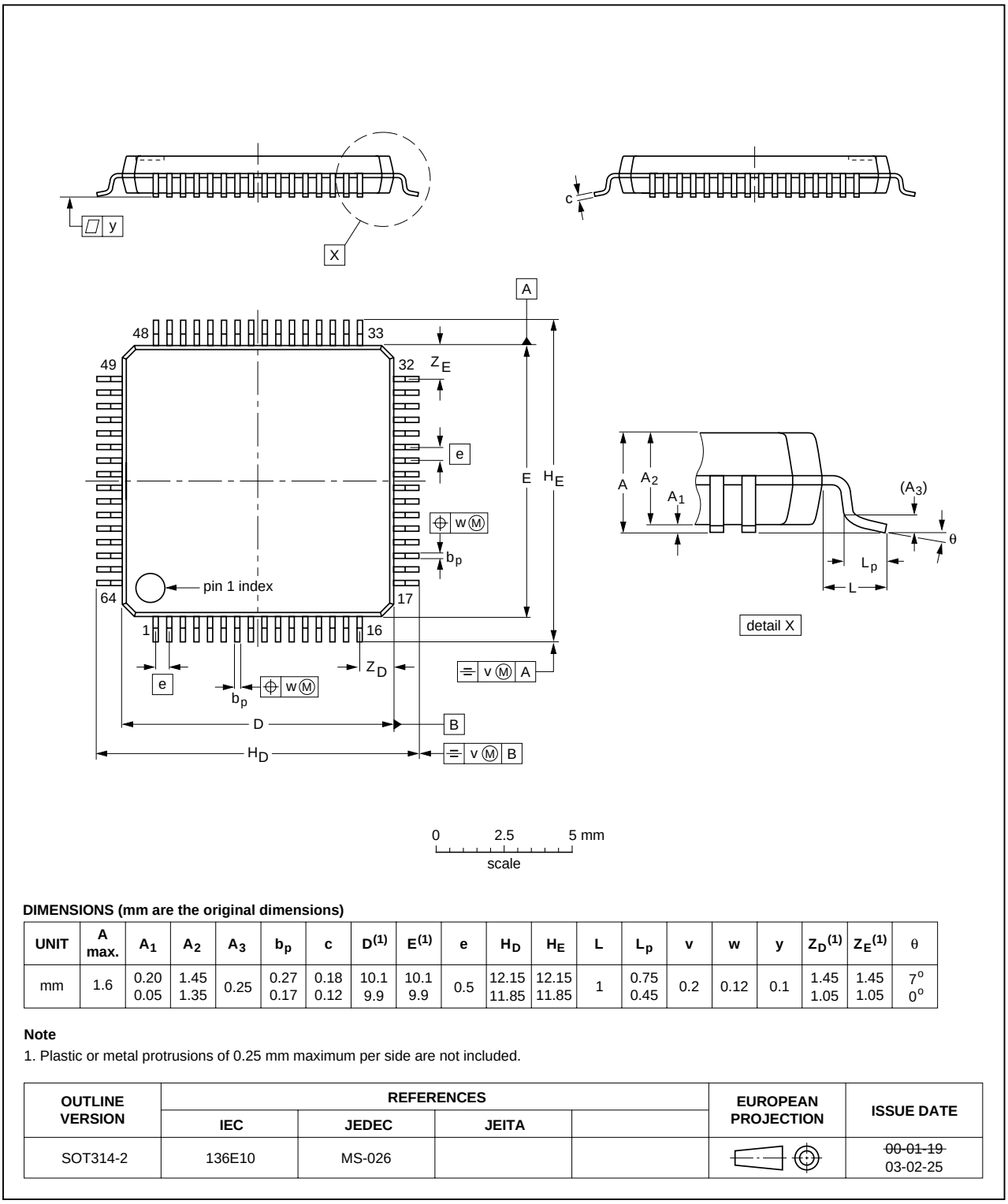

**Fig 11. Varicap behavior**



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## 12. Package outline

**LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm** **SOT314-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_D$ | $H_E$ | L | $L_p$ | v | w | y | $Z_D^{(1)}$ | $Z_E^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.6 | 0.20<br>0.05 | 1.45<br>1.35 | 0.25 | 0.27<br>0.17 | 0.18<br>0.12 | 10.1<br>9.9 | 10.1<br>9.9 | 0.5 | 12.15<br>11.85 | 12.15<br>11.85 | 1 | 0.75<br>0.45 | 0.2 | 0.12 | 0.1 | 1.45<br>1.05 | 1.45<br>1.05 | $7^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT314-2 | 136E10 | MS-026 | | | | ~~00-01-19~~<br>03-02-25 |

**Fig 12. Package outline SOT314-2 (LQFP64))**



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# 13. Handling information

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be completely safe you must take normal precautions appropriate to handling integrated circuits.

# 14. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

## 14.3 Wave soldering

Key characteristics in wave soldering are:



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- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 13) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 33 and 34

**Table 33. SnPb eutectic process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume ($mm^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

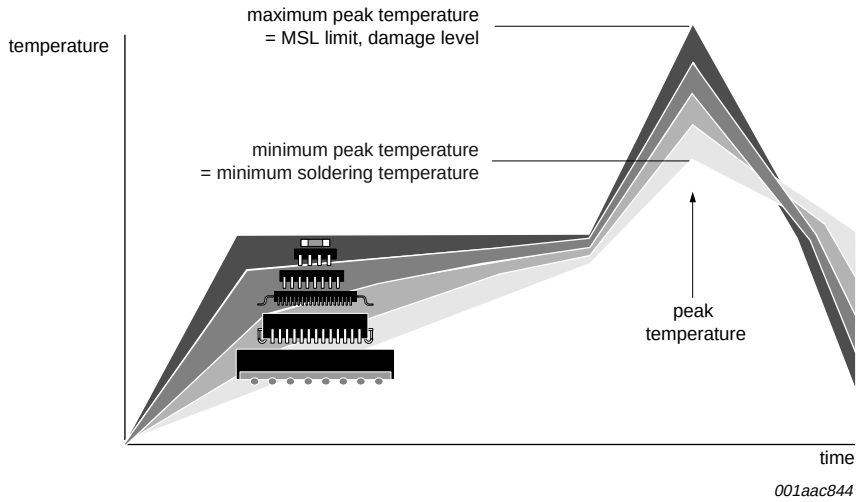
**Table 34. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume ($mm^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 13.


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MSL: Moisture Sensitivity Level

**Fig 13. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

## 15. Abbreviations

**Table 35. Abbreviations**

| Acronym | Description |
|---|---|
| ALC | Automatic Level Control |
| BiCMOS | Bipolar Complementary Metal Oxide Semiconductor |
| CMOS | Complementary Metal Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| FM | Frequency Modulation |
| IF | Intermediate Frequency |
| ISM | Industrial, Medical and Scientific |
| LNA | Low Noise Amplifier |
| LO | Local Oscillator |
| LPF | Low-Pass Filter |
| PA | Power Amplifier |
| PCB | Printed-Circuit Board |
| PLL | Phase-Locked Loop |
| RF | Radio Frequency |
| RSSI | Received Signal Strength Indicator |
| SINAD | Signal-plus-Noise-And-Distortion to noise-plus-distortion ratio |
| VCO | Voltage Controlled Oscillator |


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# 16. Revision history

**Table 36. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| SA58646_1 | 20070208 | Product data sheet | - | - |



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| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 19. Contents


**1 General description . . . . . 1**
**2 Features . . . . . 1**
**3 Applications . . . . . 2**
**4 Ordering information . . . . . 2**
**5 Block diagram . . . . . 3**
**6 Pinning information . . . . . 4**
6.1 Pinning . . . . . 4
6.2 Pin description . . . . . 4
**7 Functional description . . . . . 7**
7.1 Power supply and power management . . . . . 7
7.1.1 Power supply voltage . . . . . 7
7.1.2 Power-saving operation modes . . . . . 7
7.1.3 Control bits in power saving modes . . . . . 8
7.2 FM receiver part . . . . . 9
7.3 Transmitter part . . . . . 10
7.4 Synthesizer . . . . . 10
7.5 RX baseband . . . . . 12
7.6 TX baseband . . . . . 13
7.7 Other features . . . . . 14
7.7.1 Voltage regulator . . . . . 14
7.7.2 Low battery detector . . . . . 14
7.8 Microcontroller serial interface . . . . . 14
**8 Data registers and addresses . . . . . 14**
8.1 Data register 0 . . . . . 16
8.2 Data register 1 . . . . . 19
8.3 Data register 2 . . . . . 19
8.4 Data register 3 . . . . . 19
8.5 Data register 4 . . . . . 19
8.6 Data register 5 . . . . . 21
8.7 Data register 6 . . . . . 23
**9 Limiting values . . . . . 26**
**10 Thermal characteristics . . . . . 26**
**11 Characteristics . . . . . 26**
**12 Package outline . . . . . 36**
**13 Handling information . . . . . 37**
**14 Soldering . . . . . 37**
14.1 Introduction to soldering . . . . . 37
14.2 Wave and reflow soldering . . . . . 37
14.3 Wave soldering . . . . . 37
14.4 Reflow soldering . . . . . 38
**15 Abbreviations . . . . . 39**
**16 Revision history . . . . . 40**
**17 Legal information . . . . . 41**
17.1 Data sheet status . . . . . 41
17.2 Definitions . . . . . 41
17.3 Disclaimers . . . . . 41
17.4 Trademarks . . . . . 41
**18 Contact information . . . . . 41**
**19 Contents . . . . . 42**


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