SA58643

Single-Pole Double-Throw (SPDT) switch

Rev. 01 — 20 November 2006 Product data sheet

1. General description

The SA58643 is a wideband RF switch fabricated in BiCMOS technology and incorporating on-chip CMOS/TTL compatible drivers. Its primary function is to switch signals in the frequency range DC to 1 GHz from one 50 Ω channel to another. The switch is activated by a CMOS/TTL compatible signal applied to the enable channel 1 pin (ENCH1).

The extremely low current consumption makes the SA58643 ideal for portable applications. The excellent isolation and low loss makes this a suitable replacement for PIN diodes.

The SA58643 is available in an 8-pin TSSOP package.

2. Features

- Wideband (DC to 1 GHz)
- Low through loss (1 dB typical at 200 MHz)
- Unused input is terminated internally in 50 Ω
- Excellent overload capability (1 dB gain compression point +18 dBm at 300 MHz)
- Low DC power (170 μA from 5 V supply)
- Fast switching (20 ns typical)
- Good isolation (off channel isolation 60 dB at 100 MHz)
- Low distortion (IP3 intercept +33 dBm)
- Good 50 Ω match (return loss 18 dB at 400 MHz)
- Full ESD protection
- Bidirectional operation

3. Applications

- Digital transceiver front-end switch
- Antenna switch
- Filter selection
- Video switch
- FSK transmitter

NXP founded by Philips

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SA58643DP	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm	SOT505-1

5. Block diagram

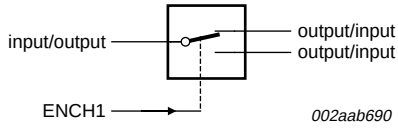


Fig 1. Block diagram of SA58643

6. Pinning information

6.1 Pinning

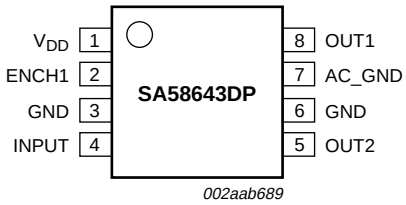


Fig 2. Pin configuration for TSSOP8

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{DD}	1	supply voltage
ENCH1	2	enable channel 1
GND	3, 6	ground
INPUT	4	input
OUT2	5	output
AC_GND	7	AC ground
OUT1	8	output

© NXP B.V. 2006. All rights reserved.

7. Equivalent circuit

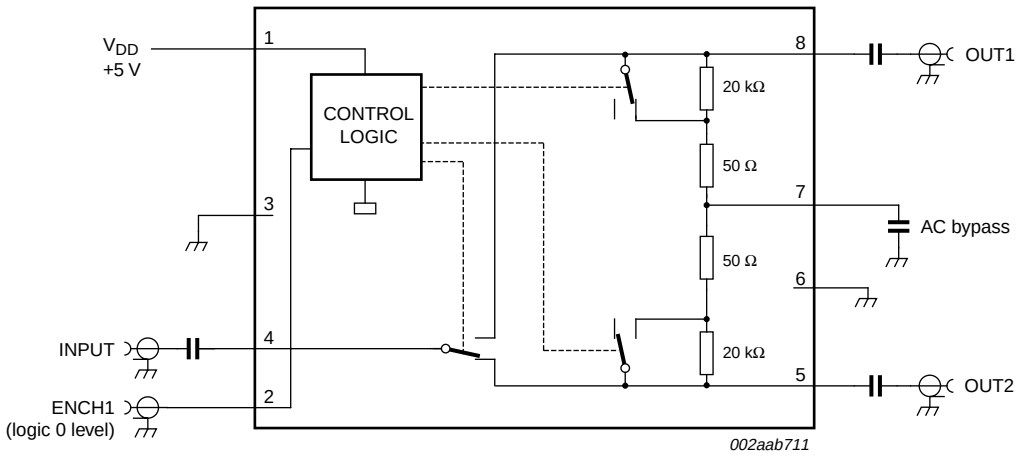


Fig 3. Equivalent circuit

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			–0.5	+5.5	V
P	power dissipation	T_{amb} = 25 °C (still air)	[1]	-	568	mW
$T_{j(max)}$	maximum junction temperature			-	150	°C
$P_{INPUT_OUT1_OUT2}$	power on pin INPUT or on pin OUT1 or on pin OUT2			-	20	dBm
T_{stg}	storage temperature			–65	+150	°C

[1] Maximum dissipation is determined by the operating ambient temperature and the thermal resistance, $R_{th(j-a)}$: TSSOP8: $R_{th(j-a)}$ = 220 K/W.

9. Recommended operating conditions

Table 4. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3.0	-	5.5	V
T_{amb}	ambient temperature	SA grade	–40	-	+85	°C
T_j	junction temperature	SA grade	–40	-	+105	°C

© NXP B.V. 2006. All rights reserved.

10. Static characteristics

Table 5. Static characteristics

V_{DD} = +5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DD}	supply current			40	170	300	µA
V_{th}	threshold voltage	TTL/CMOS logic	[1]	1.1	1.25	1.4	V
V_{IH}	HIGH-level input voltage	logic 1 level; enable channel 1		2.0	-	V_{DD}	V
V_{IL}	LOW-level input voltage	logic 0 level; enable channel 2		–3.0	-	+0.8	V
$I_{IL(ENCH1)}$	LOW-level input current on pin ENCH1	ENCH1 = 0.4 V		–1	0	+1	µA
$I_{IH(ENCH1)}$	HIGH-level input current on pin ENCH1	ENCH1 = 2.4 V		–1	0	+1	µA

[1] The ENCH1 input must be connected to a valid logic level for proper operation of the SA58643.

11. Dynamic characteristics

Table 6. Dynamic characteristics

V_{DD} = +5 V; T_{amb} = 25 °C; unless otherwise specified.
All measurements include the effects of the SA58643 evaluation board. Measurement system impedance is 50 Ω.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\|s_{21}\|^2$	insertion power gain	DC to 100 MHz		-	1	-	dB
		500 MHz		-	1.4	-	dB
		900 MHz		-	2	2.8	dB
$\|s_{12}\|^2$	isolation	10 MHz	[1]	70	80	-	dB
		100 MHz		-	60	-	dB
		500 MHz		-	50	-	dB
		900 MHz		24	30	-	dB
$\|s_{22}\|^2$	output return loss	DC to 400 MHz		-	20	-	dB
		900 MHz		-	12	-	dB
$\|s_{11}\|^2$	input return loss	DC to 400 MHz		-	17	-	dB
		900 MHz		-	13	-	dB
$t_{d(off)}$	turn-off delay time	50 % TTL to (90 % to 10 %) RF		-	20	-	ns
$t_{f(off)}$	turn-off fall time	90 % to 10 % RF		-	5	-	ns
$t_{r(on)}$	turn-on rise time	10 % to 90 % RF		-	5	-	ns
$V_{trt(p-p)}$	peak-to-peak transient voltage	switching transients		-	165	-	mV
$P_{L(1dB)}$	output power at 1 dB gain compression	DC to 1 GHz		-	+18	-	dBm
IP3	third-order intercept point	100 MHz		-	+33	-	dBm
IP2	second-order intercept point	100 MHz		-	+52	-	dBm
NF	noise figure	Z_o = 50 Ω					
		100 MHz		-	1.0	-	dB
		900 MHz		-	2.0	-	dB

[1] The placement of the AC bypass capacitor is critical to achieve these specifications. See Section 13 “Application information” for more details.

© NXP B.V. 2006. All rights reserved.

12. Performance curves

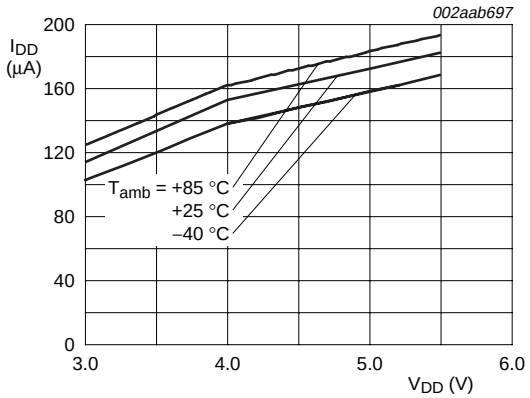
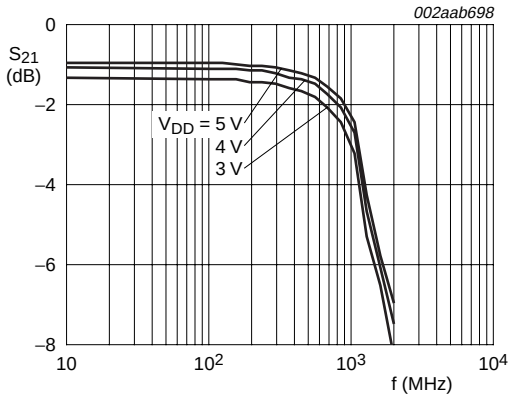
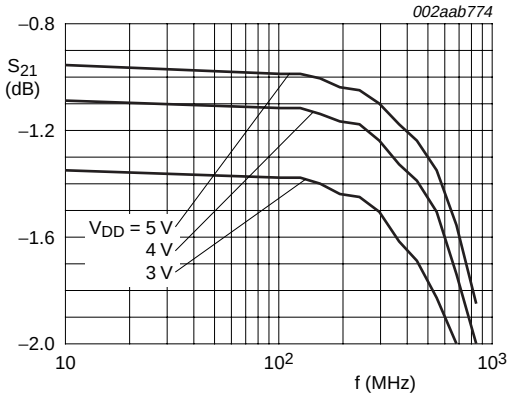


Fig 4. Supply current versus V_{DD} and temperature



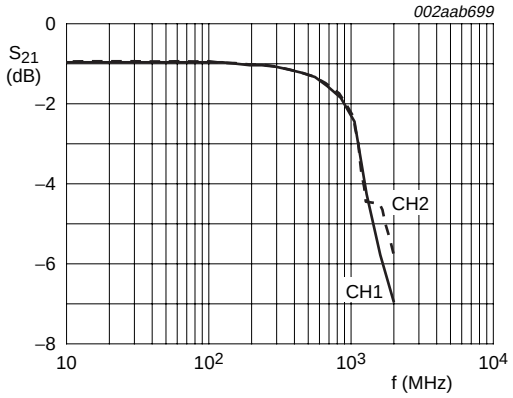
T_{amb} = +25 °C

Fig 5. Loss versus frequency and V_{DD}



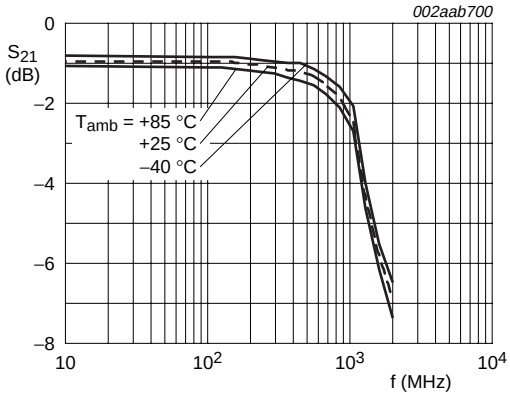
T_{amb} = +25 °C

Fig 6. Loss versus frequency and V_{DD}



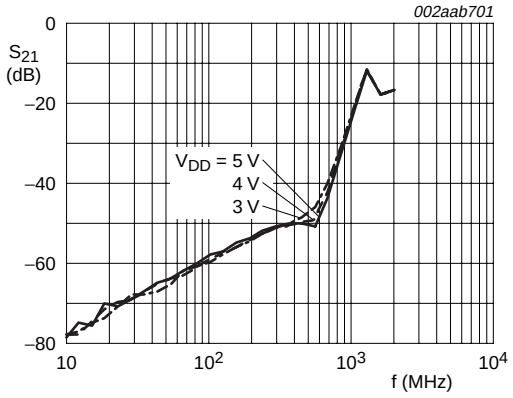
T_{amb} = +25 °C; V_{DD} = 5 V

Fig 7. Loss matching versus frequency; CH1 versus CH2



V_{DD} = 5 V

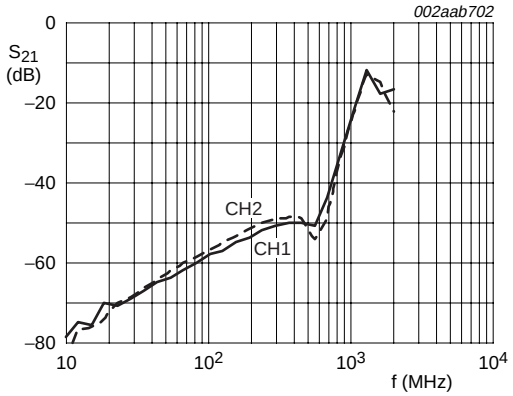
Fig 8. Loss versus frequency and temperature



T_{amb} = +25 °C

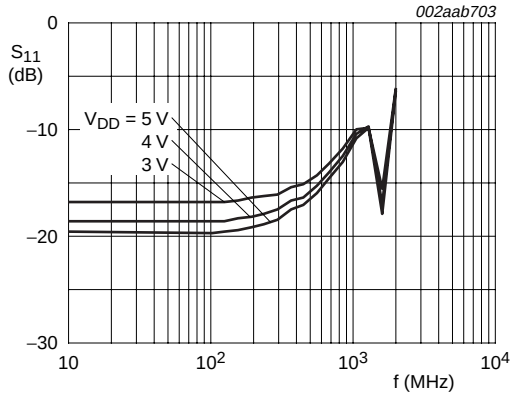
Fig 9. Isolation versus frequency and V_{DD}

© NXP B.V. 2006. All rights reserved.



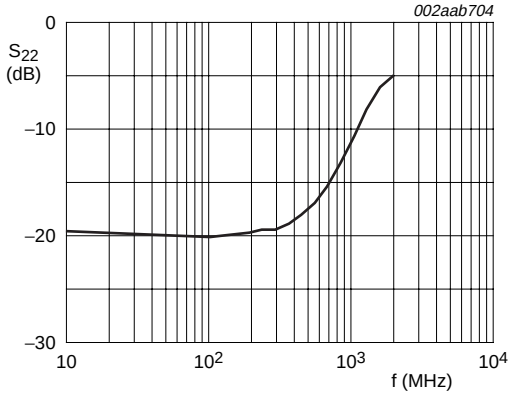
T_{amb} = +25 °C; V_{DD} = 5 V

Fig 10. Isolation matching versus frequency; CH1 versus CH2



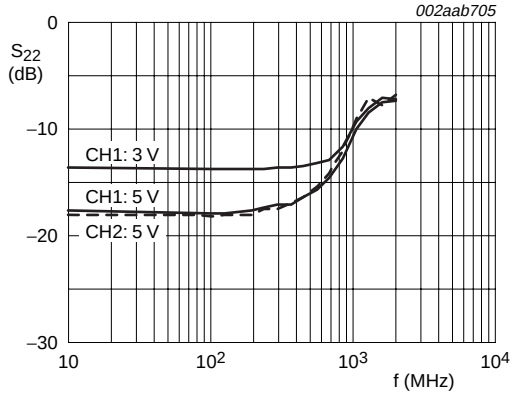
T_{amb} = +25 °C

Fig 11. Input match ON-channel versus frequency and V_{DD}



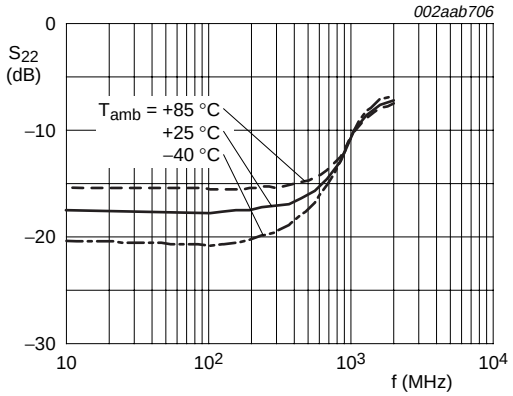
T_{amb} = +25 °C; V_{DD} = 5 V

Fig 12. Output match ON-channel versus frequency



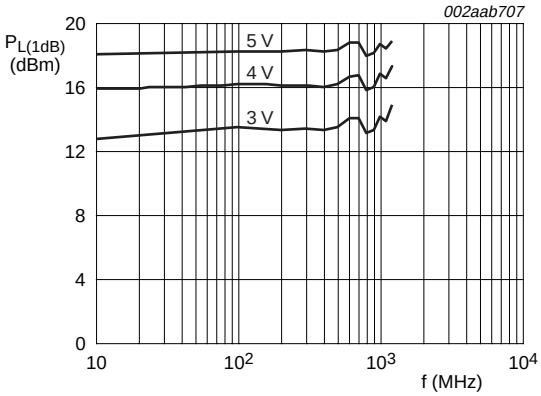
T_{amb} = +25 °C

Fig 13. OFF-channel match versus frequency and V_{DD}



V_{DD} = 5 V

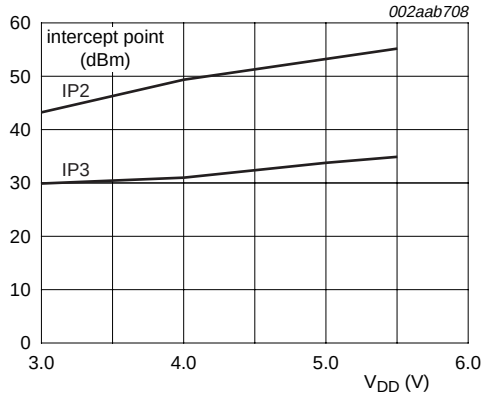
Fig 14. OFF-channel match versus frequency and temperature



T_{amb} = +25 °C

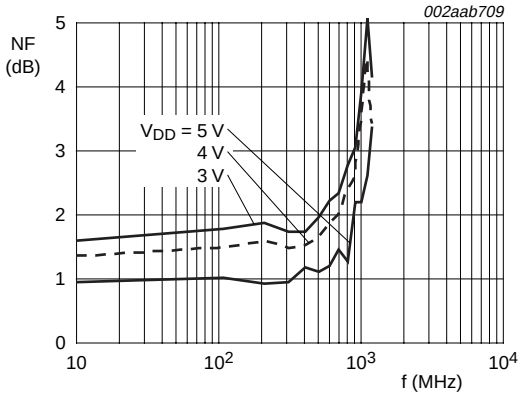
Fig 15. $P_{L(1dB)}$ versus frequency and V_{DD}

© NXP B.V. 2006. All rights reserved.



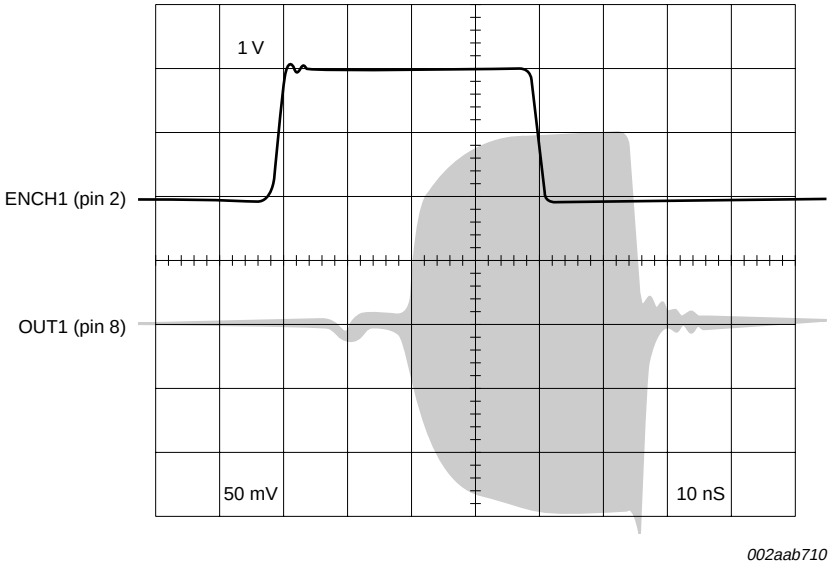
T_{amb} = +25 °C

Fig 16. Intercept points versus V_{DD}



T_{amb} = +25 °C; Z_o = 50 Ω

Fig 17. Noise Figure versus frequency and V_{DD}



f_i = 100 MHz at −6 dBm; V_{DD} = 5 V

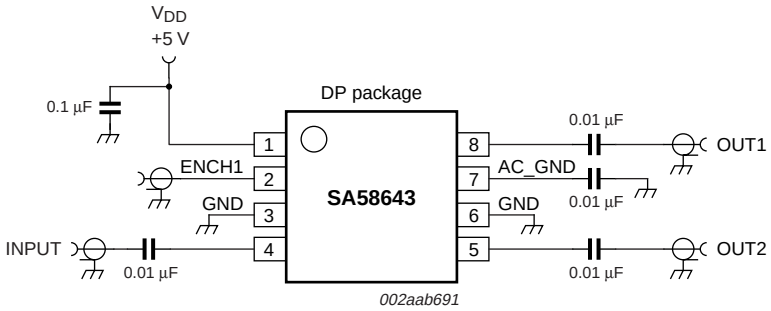
Fig 18. Switching speed

© NXP B.V. 2006. All rights reserved.

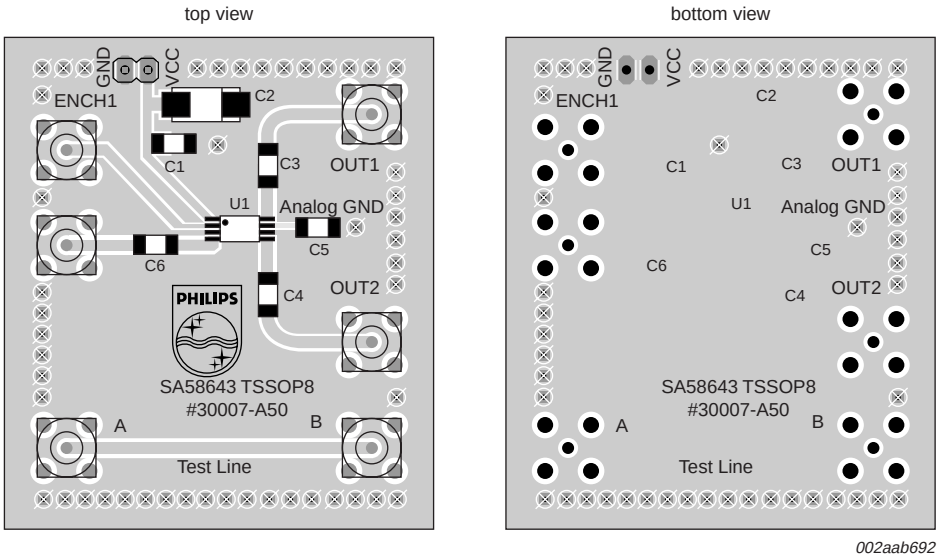
13. Application information

13.1 Evaluation demo board

The typical applications schematic and printed-circuit board layout of the SA58643 evaluation board is shown in Figure 19. The layout of the board is simple, but a few cautions need to be observed. The input and output traces should be 50 Ω. The placement of the AC bypass capacitor is extremely critical if a symmetric isolation between the two channels is desired. The trace from pin 7 (AC_GND) should be drawn back towards the package and then be routed downwards. The capacitor should be placed straight down as close to the device as practical. For better isolation between the two channels at higher frequencies, it is also advisable to run the two output/input traces at an angle. This also minimizes any inductive coupling between the two traces. The power supply bypass capacitor should be placed close to the device. Figure 5 shows the frequency response of the SA58643. The loss matching between the two channels is excellent to 1.2 GHz as shown in Figure 7.



a. Evaluation board schematic



b. SA58643 board layout

Fig 19. Evaluation board and layout

© NXP B.V. 2006. All rights reserved.

The SA58643DP evaluation demo board (see Figure 19b. SA58643 board layout) provides a stable RF layout. The demo circuit (see Figure 19a. Evaluation board schematic) is constructed on 2-layer, 1-ounce copper, FR4 PCB material. The overall thickness is 0.062 inches and has a dielectric constant, ε_r of 4.6. The transmission lines are modeled for coplanar waveguide with both top and bottom ground. The 50 Ω transmission line width is 1.388 mm, the gap from transmission line to top ground plane is 0.254 mm, and the dielectric thickness is 1.499 mm. To facilitate grounding, and support low inductance ground returns, the top and bottom grounds are connected by through-hole vias that are equal in diameter to the thickness of the PCB.

The top view in Figure 19b shows the placement of the circuit components. The RF input (pin 4) is connected via a 50 Ω transmission line to a SMA connector. Symmetrical 50 Ω transmission lines connect OUT1 and OUT2 (pins 5 and 8) to SMA connectors at Outputs 1 and 2. A 50 Ω through-transmission line is provided as a calibration standard. The outputs are selected via the DC logic level on ENCH1 (pin 2). Logic 1 level enables Output1 (that is, connects it to the common RF input); Logic 0 enables Output2. The positive supply, V_{DD} (pin 1) and AC_GND (pin 7) are decoupled using 100 nF, 0805 ceramic chip capacitors to ground.

13.2 Application examples

The SA58643 is a very versatile part and can be used in many applications. Figure 20 shows a block diagram of a typical digital RF transceiver front-end. In this application the SA58643 replaces the duplexer which is typically very bulky and lossy. Due to the low power consumption of the device, it is ideally suited for handheld applications such as in CT2 cordless telephones. The SA58643 can also be used to generate Amplitude Shift Keying (ASK) or On-Off Keying (OOK), and Frequency Shift Keying (FSK) signals for digital RF communications systems. Block diagrams for these applications are shown in Figure 21 and Figure 22, respectively.

For applications that require a higher isolation at 1 GHz than obtained from a single SA58643, several SA58643s can be cascaded as shown in Figure 23. The cascaded configuration will have a higher loss, but greater than 35 dB of isolation at 1 GHz and greater than 65 dB at 500 MHz can be obtained from this configuration. The isolation and matching of the two channels over frequency is shown in Figure 9 and Figure 10, respectively. By modifying the enable control, an RF multiplexer/demultiplexer or antenna selector can be constructed. The simplicity of the SA58643 coupled with its ease of use and high performance lends itself to many innovative applications.

The SA58643 switch terminates the OFF channel in 50 Ω. The 50 Ω resistor is internal and is in series with the external AC bypass capacitor. Matching to impedances other than 50 Ω can be achieved by adding a resistor in series with the AC bypass capacitor (that is, 25 Ω additional to match to a 75 Ω environment).

© NXP B.V. 2006. All rights reserved.

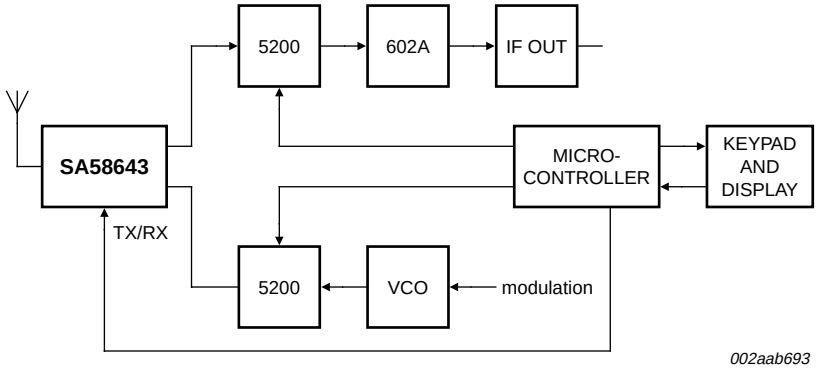


Fig 20. A typical TDMA/digital RF transceiver system front-end

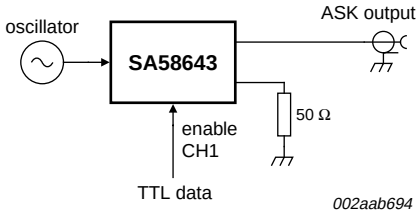


Fig 21. Amplitude Shift Keying (ASK) generator

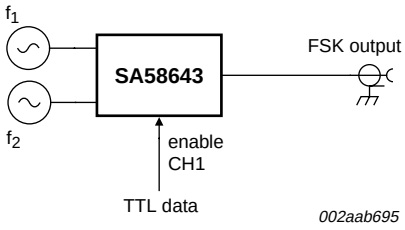


Fig 22. Frequency Shift Keying (FSK) generator

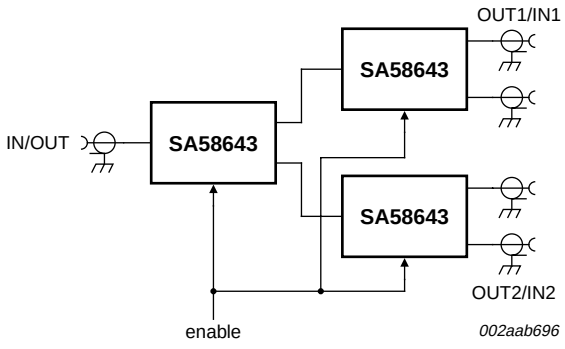
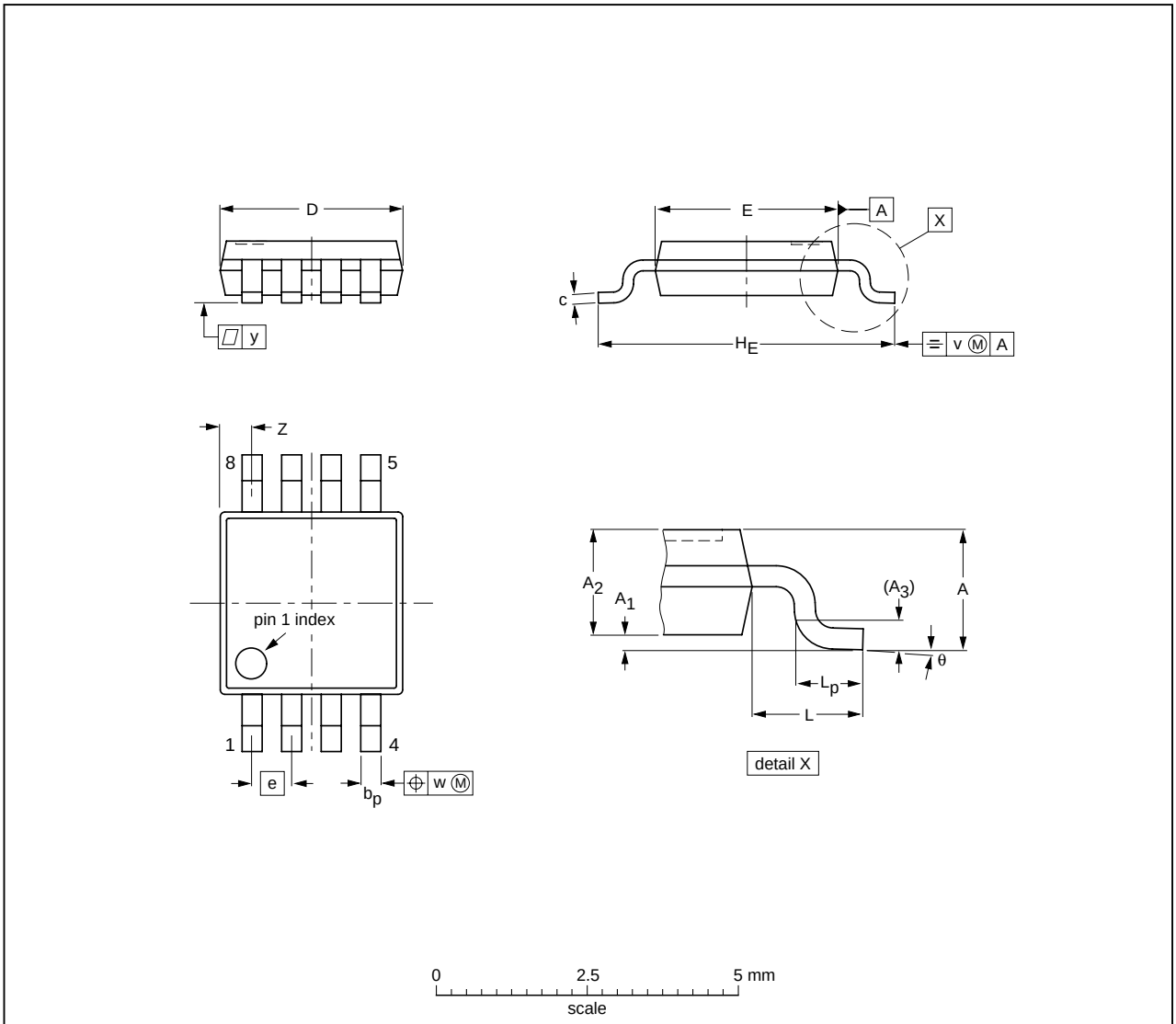


Fig 23. Cascaded configuration

© NXP B.V. 2006. All rights reserved.

14. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm **SOT505-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.45 0.25	0.28 0.15	3.1 2.9	3.1 2.9	0.65	5.1 4.7	0.94	0.7 0.4	0.1	0.1	0.1	0.70 0.35	6° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-1						~~99-04-09~~ 03-02-18

Fig 24. Package outline SOT505-1 (TSSOP8)

© NXP B.V. 2006. All rights reserved.

15. Soldering

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus PbSn soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

© NXP B.V. 2006. All rights reserved.

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 25) than a PbSn process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 7 and 8

Table 7. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

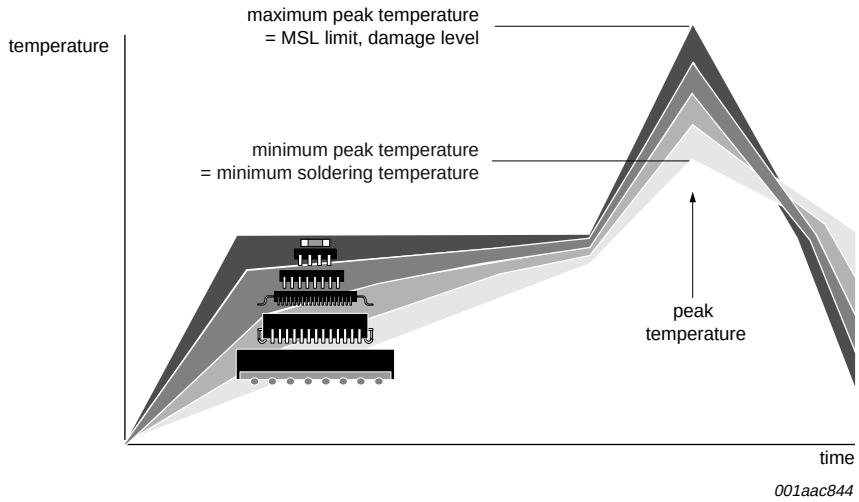
Table 8. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 25.

© NXP B.V. 2006. All rights reserved.



MSL: Moisture Sensitivity Level

Fig 25. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

16. Abbreviations

Table 9. Abbreviations

Acronym	Description
ASK	Amplitude Shift Keying
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
ESD	Electrostatic Discharge
FSK	Frequency Shift Keying
OOK	On-Off Keying
PIN	Positive Intrinsic Negative
RF	Radio Frequency
SMA	Sub-Miniature A
TTL	Transistor-Transistor Logic

17. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SA58643_1	20061120	Product data sheet	-	-

© NXP B.V. 2006. All rights reserved.

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

18.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

18.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of a NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

18.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

19. Contact information

For additional information, please visit: **http://www.nxp.com**

For sales office addresses, send an email to: **salesaddresses@nxp.com**

© NXP B.V. 2006. All rights reserved.

20. Contents

1	**General description**	**1**
2	**Features**	**1**
3	**Applications**	**1**
4	**Ordering information**	**2**
5	**Block diagram**	**2**
6	**Pinning information**	**2**
6.1	Pinning	2
6.2	Pin description	2
7	**Equivalent circuit**	**3**
8	**Limiting values**	**3**
9	**Recommended operating conditions**	**3**
10	**Static characteristics**	**4**
11	**Dynamic characteristics**	**4**
12	**Performance curves**	**5**
13	**Application information**	**8**
13.1	Evaluation demo board	8
13.2	Application examples	9
14	**Package outline**	**11**
15	**Soldering**	**12**
15.1	Introduction to soldering	12
15.2	Wave and reflow soldering	12
15.3	Wave soldering	12
15.4	Reflow soldering	13
16	**Abbreviations**	**14**
17	**Revision history**	**14**
18	**Legal information**	**15**
18.1	Data sheet status	15
18.2	Definitions	15
18.3	Disclaimers	15
18.4	Trademarks	15
19	**Contact information**	**15**
20	**Contents**	**16**

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2006. **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 20 November 2006
Document identifier: SA58643_1

founded by

PHILIPS