SA58637

2 × 2.2 W BTL audio amplifier

Rev. 01 — 25 February 2008 Product data sheet

1. General description

The SA58637 is a two-channel audio amplifier in an HVQFN20 package. It provides power output of 2.2 W per channel with an 8 Ω load at 9 V supply. The internal circuit is comprised of two Bridge-Tied Load (BTL) amplifiers with a complementary PNP-NPN output stage and standby/mute logic. The SA58637 is housed in a 20-pin HVQFN package, which has an exposed die attach paddle enabling reduced thermal resistance and increased power dissipation.

2. Features

- Low junction-to-ambient thermal resistance using exposed die attach paddle
- Gain can be fixed with external resistors from 6 dB to 30 dB
- Standby mode controlled by CMOS-compatible levels
- Low standby current < 10 μA
- No switch-on/switch-off plops
- High power supply ripple rejection: 50 dB minimum
- ElectroStatic Discharge (ESD) protection
- Output short circuit to ground protection
- Thermal shutdown protection

3. Applications

- Professional and amateur mobile radio
- Portable consumer products: toys and games
- Personal computer remote speakers

NXP founded by Philips

4. Quick reference data

Table 1. Quick reference data

V_{CC} = 6 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE} = 0 V; measured in test circuit Figure 3; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	operating		2.2	9	18	V
I_q	quiescent current	R_L = ∞ Ω	[1]	-	15	22	mA
I_{stb}	standby current	V_{MODE} = V_{CC}		-	-	10	µA
P_o	output power	THD+N = 10 %		1.2	1.5	-	W
		THD+N = 0.5 %		0.9	1.1	-	W
		THD+N = 10 %; V_{CC} = 9 V; application demo board		-	2.2	-	W
THD+N	total harmonic distortion-plus-noise	P_o = 0.5 W		-	0.15	0.3	%
PSRR	power supply rejection ratio	1 kHz	[2]	50	-	-	dB
		100 Hz to 20 kHz	[3]	40	-	-	dB

[1] With a load connected at the outputs the quiescent current will increase, the maximum of this increase being equal to the DC output offset voltage divided by R_L.

[2] Power supply rejection ratio is measured at the output with a source impedance of R_S = 0 Ω at the input. The ripple voltage is a sine wave with a frequency of 1 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.

[3] Power supply rejection ratio is measured at the output, with a source impedance of R_S = 0 Ω at the input. The ripple voltage is a sine wave with a frequency between 100 Hz and 20 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
SA58637BS	HVQFN20	plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 6 × 5 × 0.85 mm	SOT910-1

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6. Block diagram

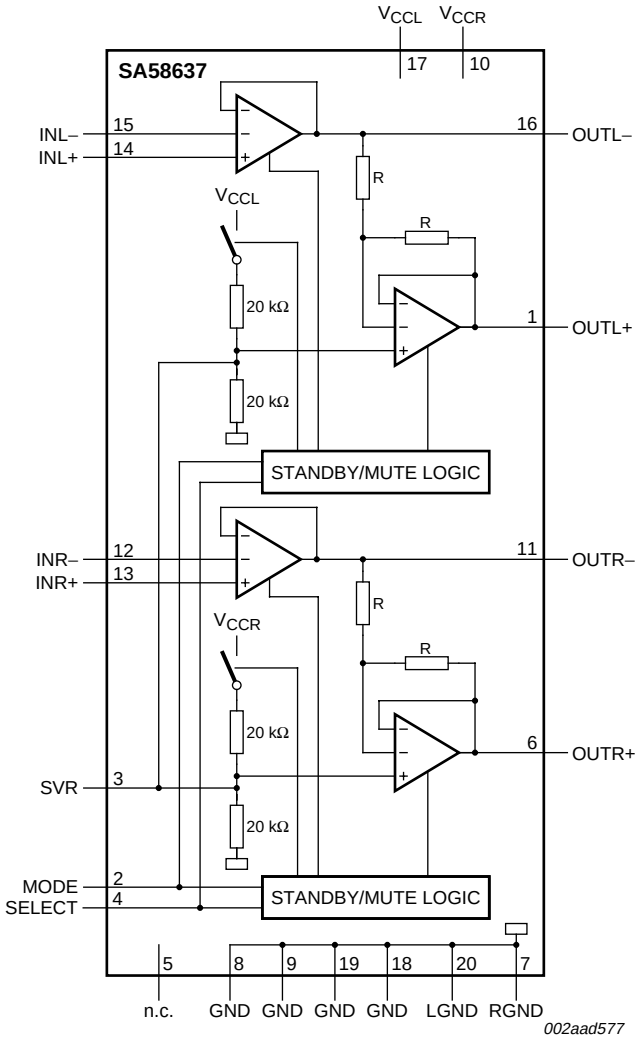

Fig 1. Block diagram of SA58637

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7. Pinning information

7.1 Pinning

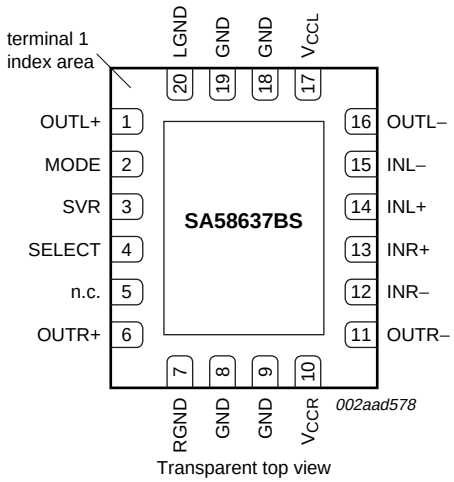

Fig 2. Pin configuration for HVQFN20

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
OUTL+	1	positive loudspeaker terminal, left channel
MODE	2	operating mode select (standby, mute, operating)
SVR	3	half supply voltage, decoupling ripple rejection
SELECT	4	BTL loudspeaker channel select (left, right, both channels)
n.c.	5	not connected
OUTR+	6	positive loudspeaker terminal, right channel
RGND	7	ground, right channel
GND	8, 9, 18, 19	ground[1]
V_{CCR}	10	supply voltage; right channel
OUTR–	11	negative loudspeaker terminal, right channel
INR–	12	negative input, right channel
INR+	13	positive input, right channel
INL+	14	positive input, left channel
INL–	15	negative input, left channel
OUTL–	16	negative output terminal, left channel
V_{CCL}	17	supply voltage, left channel
LGND	20	ground, left channel

[1] Pins 8, 9, 18 and 19 are connected to the lead frame and also to the substrate. They may be kept floating. When connected to the ground plane, the PCB can be used as heatsink.

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8. Functional description

The SA58637 is a two-channel BTL audio amplifier capable of delivering 2 × 1.5 W output power to an 8 Ω load at THD+N = 10 % using a 6 V power supply. It is also capable of delivering 2 × 2.2 W output power to an 8 Ω load at THD+N = 10 % using a 9 V power supply. Using the MODE pin, the device can be switched to standby and mute condition. The device is protected by an internal thermal shutdown protection mechanism. The gain can be set within a range of 6 dB to 30 dB by external feedback resistors.

8.1 Power amplifier

The power amplifier is a Bridge-Tied Load (BTL) amplifier with a complementary PNP-NPN output stage. The voltage loss on the positive supply line is the saturation voltage of a PNP power transistor and on the negative side the saturation voltage of an NPN power transistor. The total voltage loss is < 1 V.

8.2 Mode select pin (MODE)

The device is in Standby mode (with a very low current consumption) if the voltage at the MODE pin is greater than V_{CC} – 0.5 V, or if this pin is floating. At a MODE voltage in the range between 1.5 V and V_{CC} – 1.5 V the amplifier is in a mute condition. The mute condition is useful to suppress plop noise at the output, caused by charging of the input capacitor. The device is in Active mode if the MODE pin is grounded or less than 0.5 V (see Figure 6).

8.3 SELECT output configuration

The outputs differentially drives the speakers, so there is no need for coupling capacitors (see Figure 3). If the voltage at the SELECT pin is in the range between 1.5 V and V_{CC} – 1.5 V, or if it is kept floating, then both channels are operational. If the SELECT pin is set to a logic LOW or grounded, then only the right channel is operational and the left channel is in Standby mode. If the SELECT pin is set to logic HIGH or connected to V_{CC}, then only the left channel is operational and right channel is in Standby mode. Setting the SELECT pin to logic LOW or a logic HIGH voltage results in a reduction of quiescent current consumption by a factor of approximately 2. Switching the SELECT pin during operation is not plop-free, because the input capacitor of the channel which is coming out of standby needs to be charged first. For plop-free channel selecting the device has first to be set in mute condition with the MODE pin (between 1.5 V and V_{CC} – 1.5 V). The SELECT pin is then set to the new level and after a delay the MODE pin is set to a LOW level. The delay needed depends on the values of the input capacitors and the feedback resistors. Time needed is approximately 10 × C1 × (R1 + R2), so approximately 0.6 seconds for the values shown in Figure 3.

Table 4. Control pins MODE and SELECT versus status of output channels

Voltage levels at control pins at V_{CC} = 5 V; for other voltage levels see Figure 6 and Figure 7.

Control pin		Status of output channel		Typical I_q (mA)
MODE	**SELECT**	**Left channel**	**Right channel**	
HIGH[1]/n.c.[2]	X[3]	standby	standby	0
HVCC[4]	HVCC[4]/n.c.[2]	mute	mute	15
LOW[5]	HVCC[4]/n.c.[2]	on	on	15

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Table 4. Control pins MODE and SELECT versus status of output channels *...continued*

Voltage levels at control pins at V_{CC} = 5 V; for other voltage levels see Figure 6 and Figure 7.

Control pin		Status of output channel		Typical I_q (mA)
MODE	SELECT	Left channel	Right channel	
HVCC[4]/LOW[5]	HIGH[1]	mute/on	standby	8
HVCC[4]/LOW[5]	HVCC[4]/n.c.[2]	mute/on	mute/on	15
HVCC[4]/LOW[5]	LOW[5]	standby	mute/on	8

[1] HIGH = $V_{SELECT} > V_{CC} - 0.5$ V.

[2] n.c. = not connected or floating.

[3] X = don't care.

[4] HVCC = 1.5 V < $V_{SELECT} < V_{CC} - 1.5$ V.

[5] LOW = $V_{SELECT} < 0.5$ V.

9. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	operating	–0.3	+18	V
V_I	input voltage		–0.3	V_{CC} + 0.3	V
I_{ORM}	repetitive peak output current		-	1	A
T_{stg}	storage temperature	non-operating	–55	+150	°C
T_{amb}	ambient temperature	operating	–40	+85	°C
$V_{CC(sc)}$	supply voltage (short circuit)		-	10	V
P_{tot}	total power dissipation		-	2.2	W

10. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		80	K/W
		with heat spreader	[1]	22	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			3	K/W

[1] Thermal resistance is 22 K/W with DAP soldered to 64.5 mm^2 (10 in^2), 28.3 g (1 oz) copper heat spreader.

11. Static characteristics

Table 7. Static characteristics

V_{CC} = 6 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE} = 0 V; measured in test circuit Figure 3; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	supply voltage	operating		2.2	9	18	V
I_q	quiescent current	R_L = ∞ Ω	[1]	-	15	22	mA
I_{stb}	standby current	$V_{MODE} = V_{CC}$		-	-	10	µA

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Table 7. Static characteristics *...continued*

V_{CC} = 6 V; T_{amb} = 25 °C; R_L = 8 Ω; V_{MODE} = 0 V; measured in test circuit Figure 3; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_O	output voltage		[2]	-	2.2	-	V
$\Delta V_{O(offset)}$	differential output voltage offset			-	-	50	mV
I_{IB}	input bias current	pins INL+, INR+		-	-	500	nA
		pins INL–, INR–		-	-	500	nA
V_{MODE}	voltage on pin MODE	operating		0	-	0.5	V
		mute		1.5	-	V_{CC} – 1.5	V
		standby		V_{CC} – 0.5	-	V_{CC}	V
I_{MODE}	current on pin MODE	0 V < V_{MODE} < V_{CC}		-	-	20	µA
V_{SELECT}	voltage on pin SELECT	both channels on		1.5	-	V_{CC} – 1.5	V
		left channel on		V_{CC} – 0.5	-	V_{CC}	V
		right channel on		GND	-	0.5	V
$I_{I(SELECT)}$	input current on pin SELECT	V_{SELECT} = 0 V		-	-	100	µA

[1] With a load connected at the outputs the quiescent current will increase, the maximum of this increase being equal to the DC output offset voltage divided by R_L.

[2] The DC output voltage with respect to ground is approximately 0.5 × V_{CC}.

12. Dynamic characteristics

Table 8. Dynamic characteristics

V_{CC} = 6 V; T_{amb} = 25 °C; R_L = 8 Ω; f = 1 kHz; V_{MODE} = 0 V; measured in test circuit Figure 3; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P_o	output power	THD+N = 10 %		1.2	1.5	-	W
		THD+N = 0.5 %		0.9	1.1	-	W
		THD+N = 10 %; V_{CC} = 9 V; application demo board		-	2.2	-	W
THD+N	total harmonic distortion-plus-noise	P_o = 0.5 W		-	0.15	0.3	%
$G_{v(cl)}$	closed-loop voltage gain		[1]	6	-	30	dB
ΔZ_i	differential input impedance			-	100	-	kΩ
$V_{n(o)}$	output noise voltage		[2]	-	-	100	µV
PSRR	power supply rejection ratio	1 kHz	[3]	–50	-	-	dB
		100 Hz to 20 kHz	[4]	–40	-	-	dB
$V_{O(mute)}$	mute output voltage	mute condition	[5]	-	-	200	µV
α_{cs}	channel separation			–40	-	-	dB

[1] Gain of the amplifier is 2 × (R2 / R1) in test circuit of Figure 3.

[2] The noise output voltage is measured at the output in a frequency range from 20 Hz to 20 kHz (unweighted), with a source impedance of R_S = 0 Ω at the input.

[3] Power supply rejection ratio is measured at the output with a source impedance of R_S = 0 Ω at the input. The ripple voltage is a sine wave with a frequency of 1 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.

[4] Power supply rejection ratio is measured at the output, with a source impedance of R_S = 0 Ω at the input. The ripple voltage is a sine wave with a frequency between 100 Hz and 20 kHz and an amplitude of 100 mV (RMS), which is applied to the positive supply rail.

[5] Output voltage in mute position is measured with an input voltage of 1 V (RMS) in a bandwidth of 20 kHz, which includes noise.

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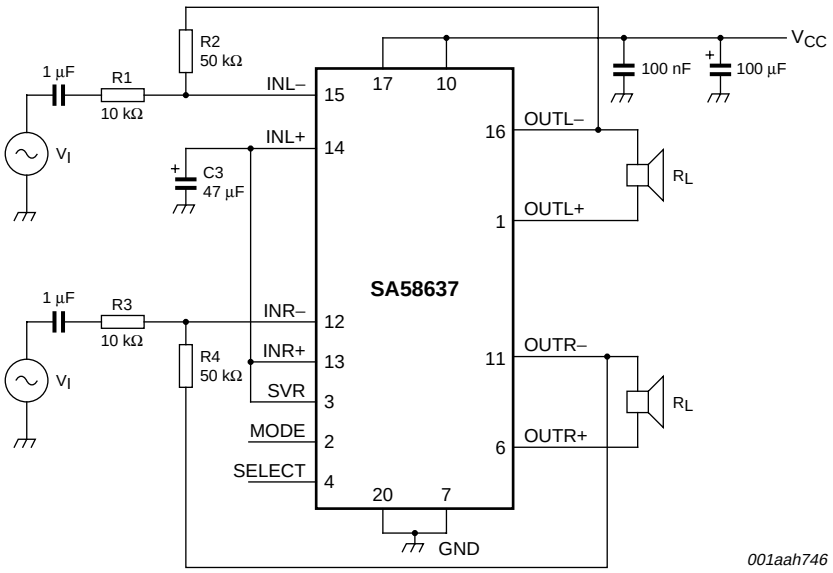
13. Application information

13.1 BTL application

T_{amb} = 25 °C, V_{CC} = 9 V, f = 1 kHz, R_L = 8 Ω, G_v = 20 dB, audio band-pass 22 Hz to 22 kHz. The single-ended input and BTL differential output diagram is shown in Figure 3.



$$Gain\ left = 2 \times \frac{R2}{R1}$$

$$Gain\ right = 2 \times \frac{R4}{R3}$$

Pins 8, 9, 18 and 19 connected to ground.

Fig 3. Application diagram of SA58637 single-ended input and BTL differential output configuration

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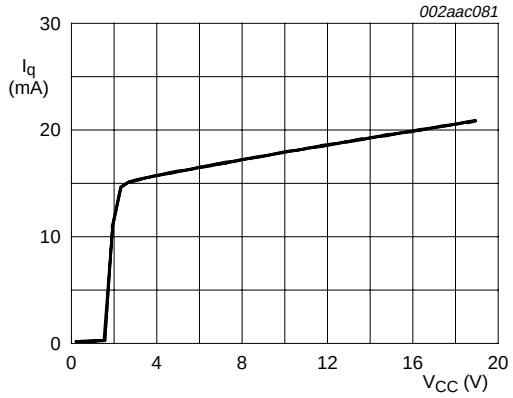
14. Test information

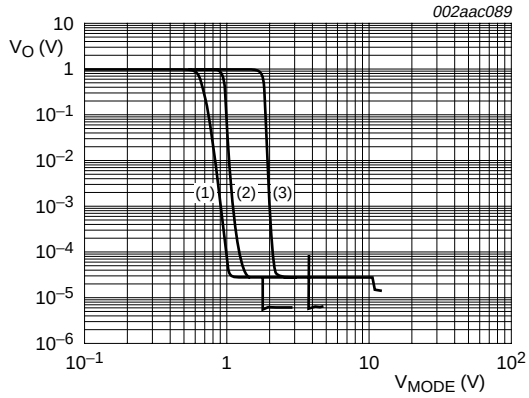
14.1 Static characterization

The quiescent current has been measured without any load impedance (Figure 4). Figure 6 shows three areas: operating, mute and standby. It shows that the DC switching levels of the mute and standby respectively depends on the supply voltage level.



$R_L = \infty\ \Omega$

Fig 4. Quiescent current as a function of supply voltage



Band-pass = 22 Hz to 22 kHz.

(1) V_{CC} = 3 V.

(2) V_{CC} = 5 V.

(3) V_{CC} = 12 V.

Fig 5. Output voltage as a function of voltage on pin MODE

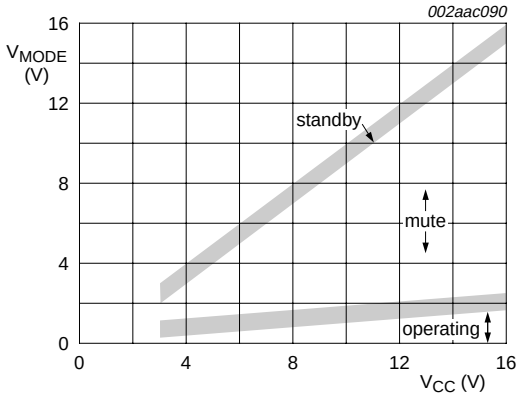


Fig 6. Voltage on pin MODE as a function of supply voltage

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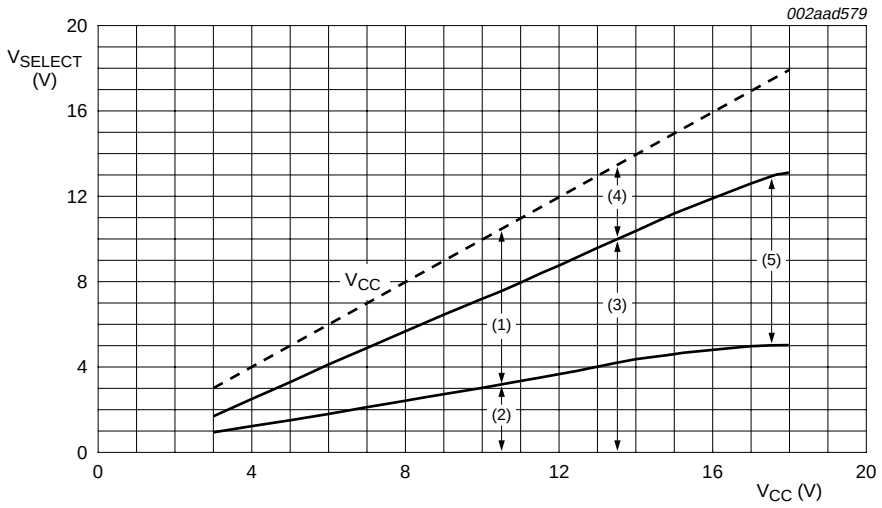

(1) Left channel on
(2) Left channel standby
(3) Right channel on
(4) Right channel standby
(5) Left channel + right channel on

Fig 7. Voltage on pin SELECT as a function of supply voltage

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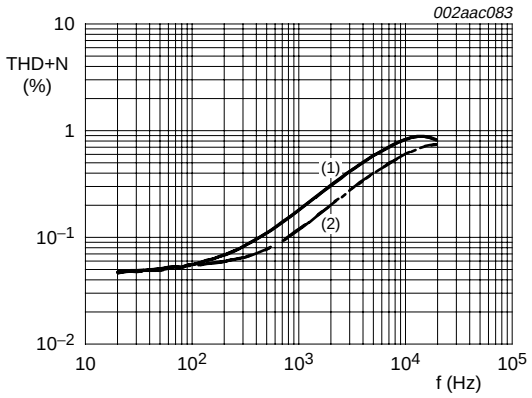
14.2 BTL dynamic characterization

The total harmonic distortion-plus-noise (THD+N) as a function of frequency (Figure 8) was measured with a low-pass filter of 80 kHz. The value of capacitor C3 influences the behavior of PSRR at low frequencies; increasing the value of C3 increases the performance of PSRR.

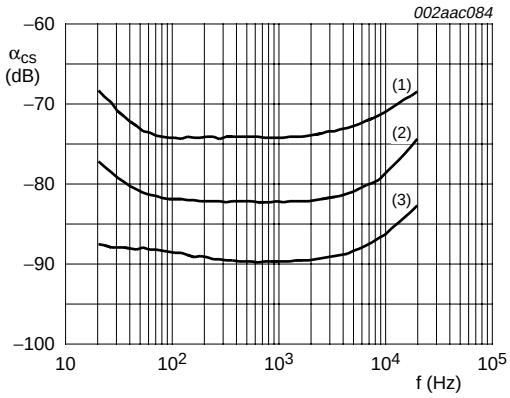


P_o = 0.5 W; G_v = 20 dB.

(1) V_{CC} = 6 V; R_L = 8 Ω.

(2) V_{CC} = 7.5 V; R_L = 16 Ω.

Fig 8. Total harmonic distortion-plus-noise as a function of frequency



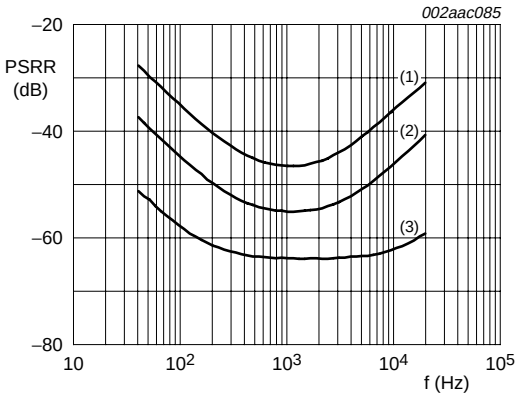
V_{CC} = 6 V; V_O = 2 V; R_L = 8 Ω.

(1) G_v = 30 dB.

(2) G_v = 20 dB.

(3) G_v = 6 dB.

Fig 9. Channel separation as a function of frequency



V_{CC} = 6 V; R_S = 0 Ω; V_{ripple} = 100 mV.

(1) G_v = 30 dB.

(2) G_v = 20 dB.

(3) G_v = 6 dB.

Fig 10. Power supply rejection ratio as a function of frequency

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14.3 Thermal behavior

The measured thermal performance of the HVQFN20 package is highly dependent on the configuration and size of the heat spreader on the application demo board. Data may not be comparable between different semiconductor manufacturers because the application demo boards and test methods are not standardized. The thermal performance of a package for a specific application may also differ from those presented here because the configuration of the application boards copper heat spreader may be significantly different.

NXP Semiconductors uses FR-4 type application boards with 28.3 g (1 oz) copper traces with solder coating.

The demo board (see Figure 16) has a 28.3 g (1 oz) copper heat spreader that runs under the IC and provides a mounting pad to solder to the die attach paddle of the HVQFN20 package. The heat spreader is symmetrical and provides a heat spreader on both top and bottom of the PCB. The heat spreader on top and bottom side of the demo board is connected through 2 mm diameter plated through holes. Directly under the DAP (Die Attach Paddle), the top and bottom side of the PCB are connected by four vias. The total top and bottom heat spreader area is 64.5 mm^2 (10 in^2).

The junction to ambient thermal resistance, $R_{th(j-a)}$ = 22 K/W for the HVQFN20 package when the exposed die attach paddle is soldered to a 32.3 mm^2 (5 in^2) area of 28.3 g (1 oz) copper heat spreader on the demo PCB. The maximum sine wave power dissipation for T_{amb} = 25 °C is:

$$\frac{150 - 25}{22} = 5.7 \text{ W}$$

Thus, for T_{amb} = 60 °C the maximum total power dissipation is:

$$\frac{150 - 60}{22} = 4.1 \text{ W}$$

The power dissipation as a function of ambient temperature curve (Figure 11) shows the power derating profiles with ambient temperature for three sizes of heat spreaders. For a more modest heat spreader using a 32.3 mm^2 (5 in^2) area on the top or bottom side of the PCB, the $R_{th(j-a)}$ is 31 K/W. When the package is not soldered to a heat spreader, the $R_{th(j-a)}$ increases to 60 K/W.

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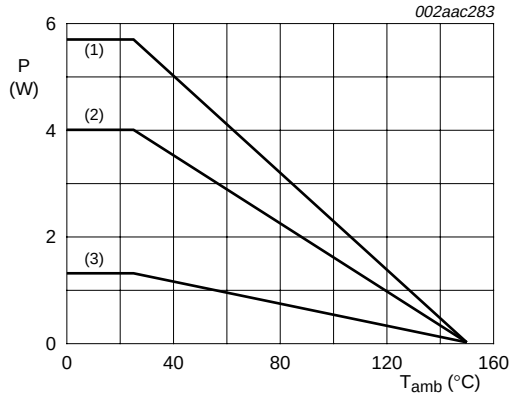


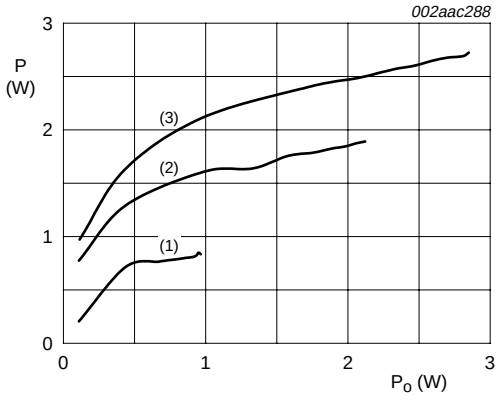
(1) 64.5 mm^2 (10 in^2) heat spreader top and bottom, 28.3 g (1 oz copper).

(2) 32.3 mm^2 (5 in^2) heat spreader top or bottom, 28.3 g (1 oz copper).

(3) No heat spreader.

Fig 11. Power dissipation as a function of ambient temperature

The characteristics curves (Figure 12a and Figure 12b, Figure 13, Figure 14, and Figure 15a and Figure 15b) show the room temperature performance for SA58637 using the demo PCB shown in Figure 16. For example, Figure 12 “Power dissipation as a function of output power” (a and b) show the performance as a function of load resistance and supply voltage. Worst case power dissipation is shown in Figure 13. Figure 15a shows that the part delivers typically 2.8 W per channel for THD+N = 10 % using 8 Ω load at 9 V supply, while Figure 15b shows that the part delivers 3.3 W per channel at 12 V supply and 16 Ω load, THD+N = 10 %.

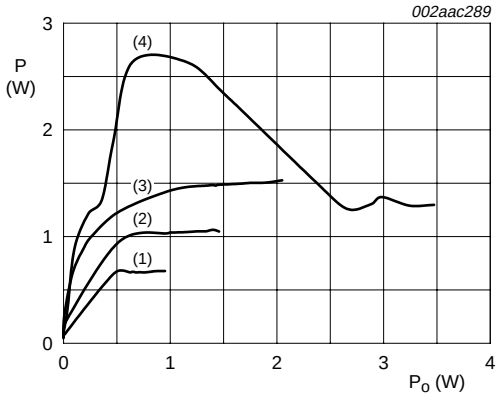


(1) V_{CC} = 6 V.

(2) V_{CC} = 7.5 V.

(3) V_{CC} = 9 V.

a. R_L = 8 Ω; f = 1 kHz; G_v = 20 dB



(1) V_{CC} = 6 V.

(2) V_{CC} = 7.5 V.

(3) V_{CC} = 9 V.

(4) V_{CC} = 12 V.

b. R_L = 16 Ω; f = 1 kHz; G_v = 20 dB

Fig 12. Power dissipation as a function of output power

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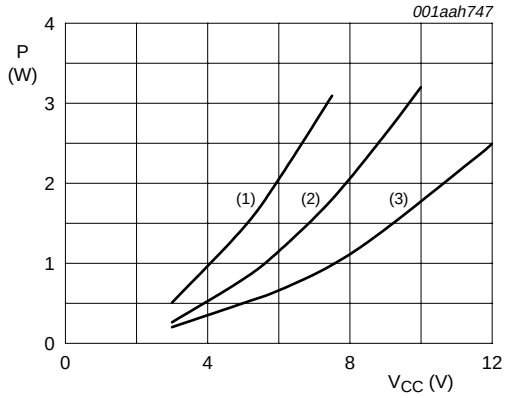
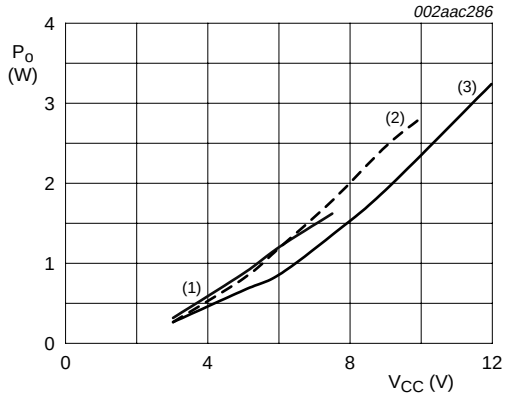


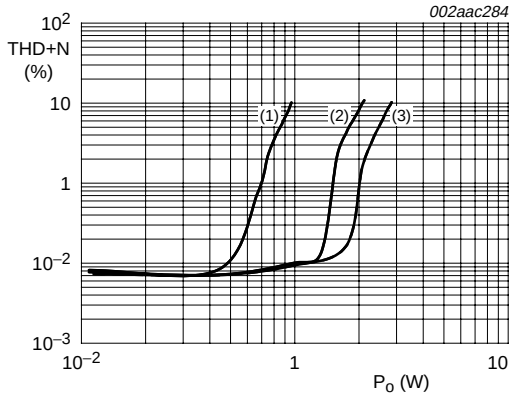
(1) R_L = 4 Ω.
(2) R_L = 8 Ω.
(3) R_L = 16 Ω.

Fig 13. Worst case power dissipation as a function of supply voltage



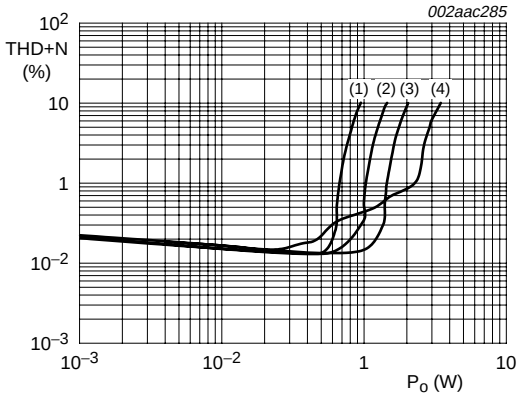
THD+N = 10 %; f = 1 kHz; G_v = 20 dB.
(1) R_L = 4 Ω.
(2) R_L = 8 Ω.
(3) R_L = 16 Ω.

Fig 14. Output power as a function of supply voltage



(1) V_{CC} = 6 V.
(2) V_{CC} = 7.5 V.
(3) V_{CC} = 9 V.

a. R_L = 8 Ω; f = 1 kHz; G_v = 20 dB



(1) V_{CC} = 6 V.
(2) V_{CC} = 7.5 V.
(3) V_{CC} = 9 V.
(4) V_{CC} = 12 V.

b. R_L = 16 Ω; f = 1 kHz; G_v = 20 dB

Fig 15. Total harmonic distortion-plus-noise as a function of output power

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14.4 General remarks

The frequency characteristics can be adapted by connecting a small capacitor across the feedback resistor. To improve the immunity of HF radiation in radio circuit applications, a small capacitor can be connected in parallel with the feedback resistor (56 kΩ); this creates a low-pass filter.

14.5 SA58637BS PCB demo

The application demo board may be used for evaluation single-ended input, BTL differential output configuration as shown in the schematic in Figure 3. The demo PCB (Figure 16) is laid out for a 64.5 mm^2 (10 in^2) heat spreader (total of top and bottom heat spreader area).

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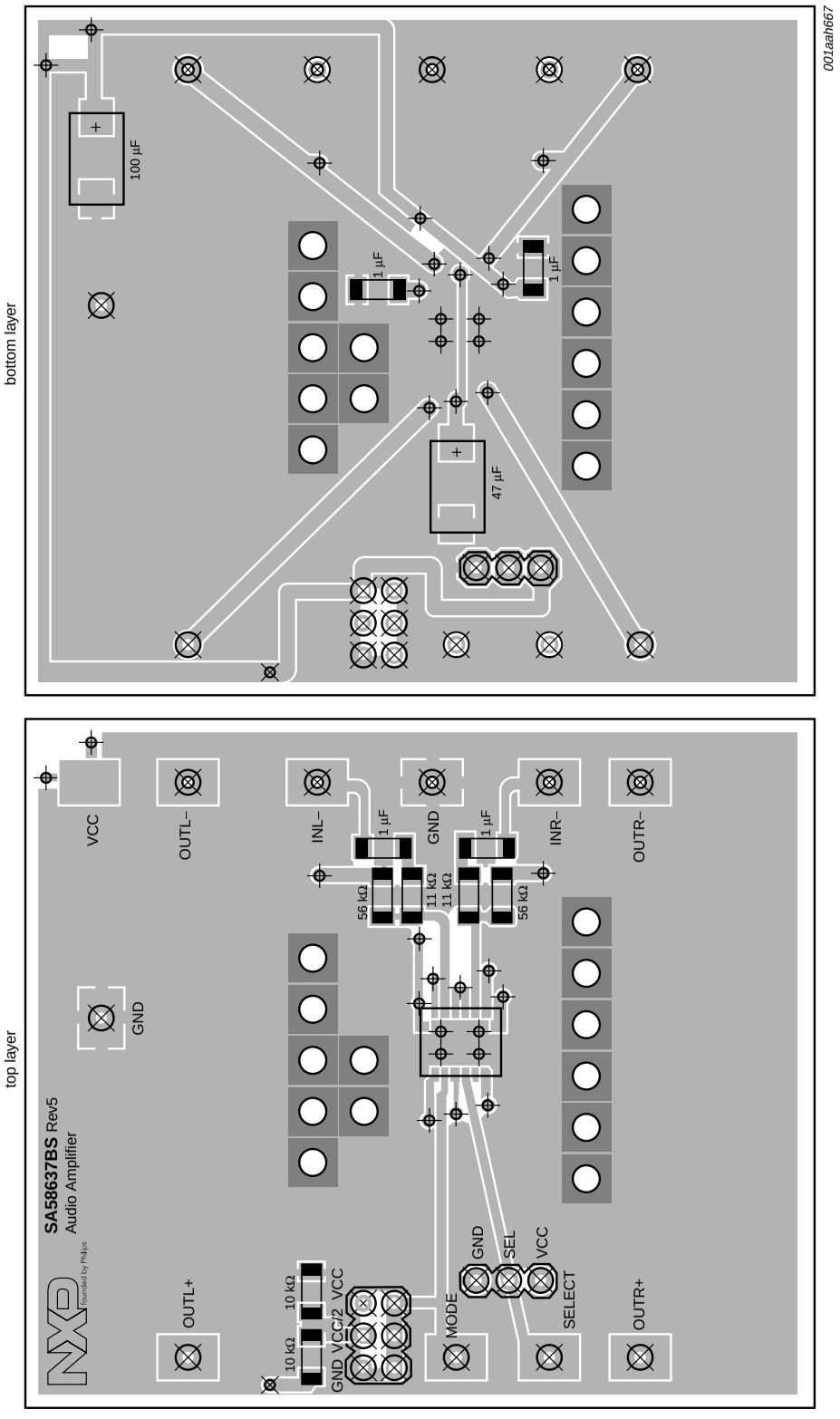

Fig 16. SA58637BS PCB demo

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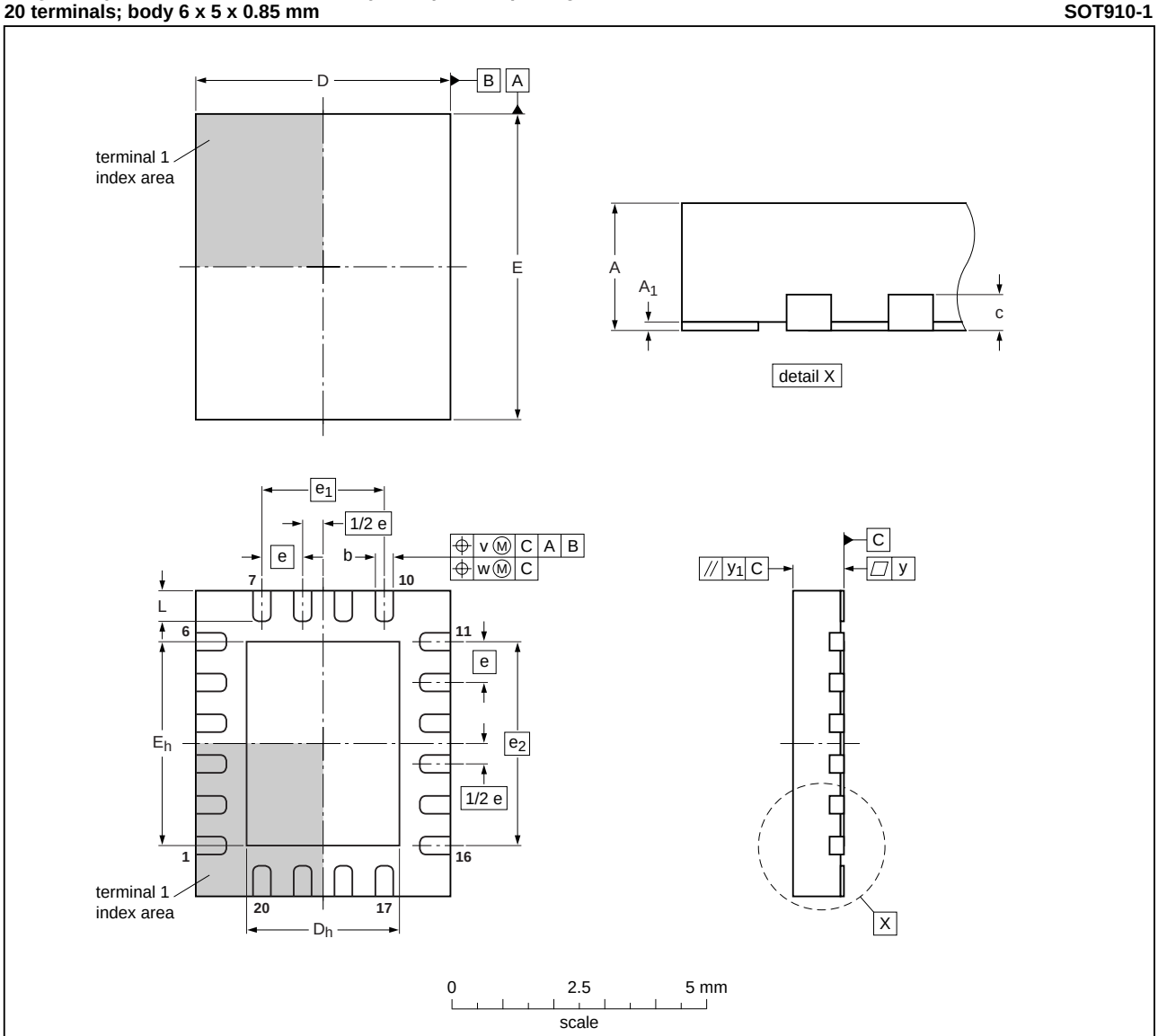
15. Package outline

HVQFN20: plastic thermal enhanced very thin quad flat package; no leads; 20 terminals; body 6 x 5 x 0.85 mm **SOT910-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	b	c	D	D_h	E	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.4 0.3	0.2	5.1 4.9	3.15 2.85	6.1 5.9	4.15 3.85	0.8	2.4	4	0.65 0.40	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT910-1	- - -	MO-220	- - -			05-10-11

Fig 17. Package outline SOT910-1 (HVQFN20)

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16. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

16.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

16.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

16.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

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16.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 18) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 9 and 10

Table 9. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 10. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 18.

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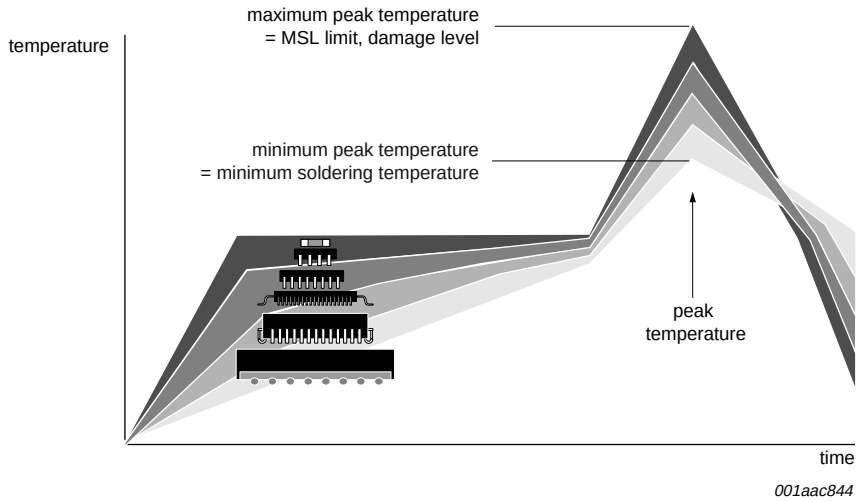

MSL: Moisture Sensitivity Level

Fig 18. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

17. Abbreviations

Table 11. Abbreviations

Acronym	Description
BTL	Bridge-Tied Load
CMOS	Complementary Metal Oxide Semiconductor
DAP	Die Attach Paddle
ESD	ElectroStatic Discharge
HF	High-Frequency
NPN	Negative-Positive-Negative
PCB	Printed-Circuit Board
PNP	Positive-Negative-Positive
RMS	Root Mean Squared
SE	Single-Ended
THD	Total Harmonic Distortion

18. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SA58637_1	20080225	Product data sheet	-	-

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19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 25 February 2008
Document identifier: SA58637_1

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