SA56

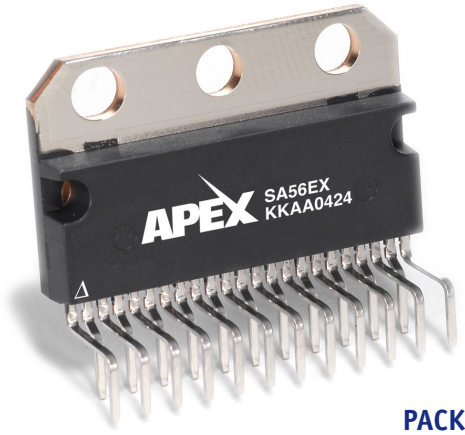
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FEATURES

- DELIVERS UP TO 5A CONTINUOUS OUTPUT
- OPERATES AT SUPPLY VOLTAGES UP TO 60V
- TTL AND CMOS COMPATIBLE INPUTS
- NO "SHOOT-THROUGH" CURRENT
- THERMAL SHUTDOWN (OUTPUTS OFF) AT 160°C
- SHORTED LOAD PROTECTION (to VS or PGND or SHORTED LOAD)
- NO BOOTSTRAP CAPACITORS REQUIRED
- PROGRAMMABLE ONBOARD PWM

APPLICATIONS

- DC MOTOR DRIVES
- POSITION AND VELOCITY SERVOMECHANISMS
- FACTORY AUTOMATION ROBOTS
- NUMERICALLY CONTROLLED MACHINERY
- COMPUTER PRINTERS AND PLOTTERS
- AUDIO AMPLIFICATION

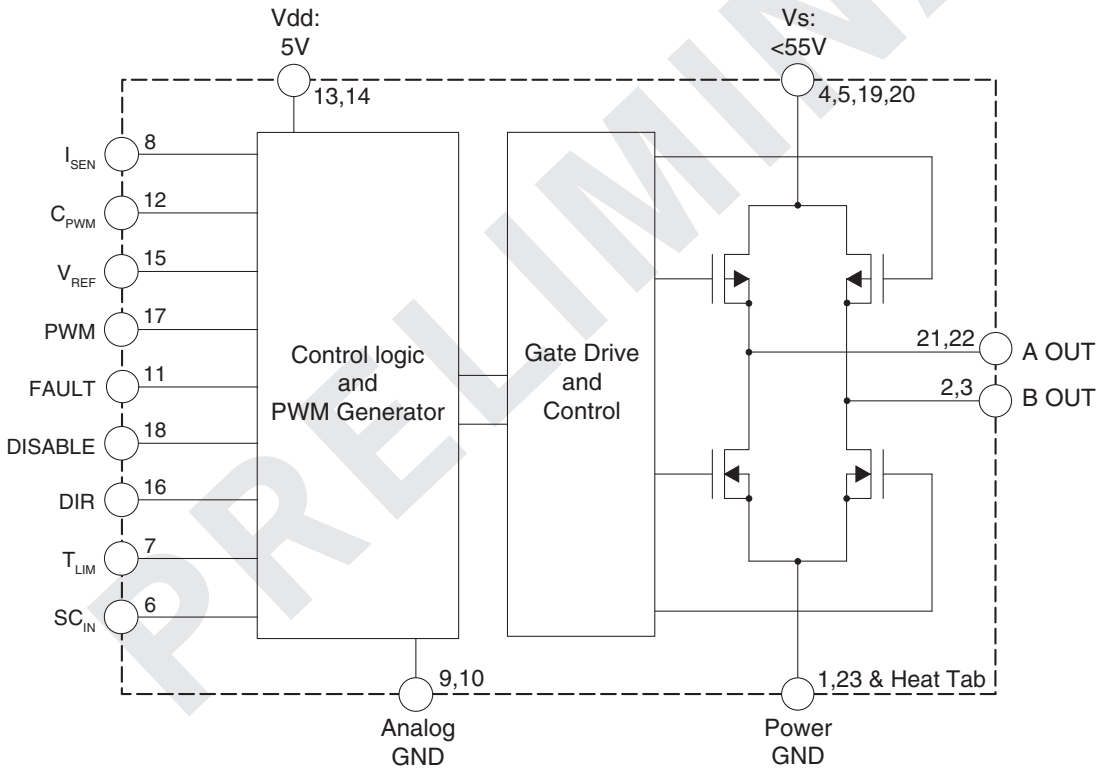


23 PIN SIP
PACKAGE STYLE EX

DESCRIPTION

The SA56 is a 5A PWM Amplifier designed for motion control applications. The device is built using a multi-technology process which combines bipolar and CMOS control circuitry with DMOS power devices in the same monolithic structure. Ideal for driving DC and stepper motors; the SA56 accommodates peak output currents up to 10A. An innovative circuit which facilitates low-loss sensing of the output current has been implemented. On board PWM oscillator and comparator are used to convert an analog signal into PWM direction and magnitude for motor control applications, or to amplify audio signals using class D amplification.

FIGURE 1. BLOCK DIAGRAM



PRELIMINARY

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, V_{DD}	5.5V
SUPPLY VOLTAGE, V_S	60V
PEAK OUTPUT CURRENT (100mS)	10A
CONTINUOUS OUTPUT CURRENT	5A
POWER DISSIPATION	TBD
POWER DISSIPATION (T_A = 25°C, Free Air)	3W
JUNCTION TEMPERATURE, $T_{J(MAX)}$	150°C
ESD SUSCEPTIBILITY (Logic Signals Only)	1500V
STORAGE TEMPERATURE, T_{STG}	–40°C to +150°C
LEAD TEMPERATURE (Soldering, 10 sec.)	300°C
JUNCTION TEMPERATURE, T_J	–40°C to +150°C

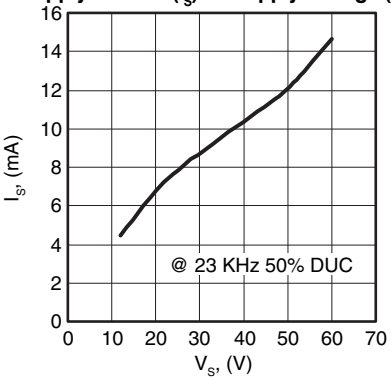
SPECIFICATIONS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_S		12		60	V
VDD		4.5		5.5	V
SWITCH ON RESISTANCE, R_{DS}(ON) N-Channel	Output Current = 5A		0.25	0.6	Ω
SWITCH ON RESISTANCE, R_{DS}(ON) P-Channel	Output Current = 5A		0.3	0.6	Ω
CLAMP DIODE FORWARD DROP, V_{CLAMP}	Clamp Current = 5A		1.43	TBD	V
LOGIC LOW INPUT VOLTAGE, V_{IL}		-0.5		0.8	V
LOGIC LOW INPUT CURRENT, I_{IL}	V_{IN} = –0.1V	-10		+10	µA
LOGIC HIGH INPUT VOLTAGE, V_{IH}		2		V_{DD}	V
LOGIC HIGH INPUT CURRENT, I_{IH}	V_{IN} = 5.5V	-10		10	µA
CURRENT SENSE OUTPUT	I_{OUT} = 1A		300	350	µA
	I_{OUT} = 5A		1.3	1.5	mA
CURRENT SENSE LINEARITY	1A ≤ I_{OUT} ≤ 5A		±1	±5	%
	100 mA ≤ I_{OUT} ≤ 5A			±8	%
	5A ≤ I_{OUT} ≤ 10A (Peak Currents only)			±8	%
SHUTDOWN TEMPERATURE, T_{JSD}	Outputs Turn OFF		160		°C
QUIESCENT SUPPLY CURRENT, I_S	No Load, F_{SW} = 23KHz 50% DUC		12	TBD	mA
QUIESCENT SUPPLY CURRENT, I_{DD}	No Load, F_{SW} = 23KHz 50% DUC		6	15	mA
OUTPUT TURN-ON DELAY TIME, t_{Don}	Sourcing Outputs, I_{OUT} = 1A		61		ns
	Sinking Outputs, I_{OUT} = 1A		66		ns
OUTPUT TURN-ON SWITCHING TIME, t_{on}	Sourcing Outputs, I_{OUT} = 1A		51		ns
	Sinking Outputs, I_{OUT} = 1A		51		ns
OUTPUT TURN-OFF DELAY TIMES, t_{Doff}	Sourcing Outputs, I_{OUT} = 1A		59		ns
	Sinking Outputs, I_{OUT} = 1A		54		ns
OUTPUT TURN-OFF SWITCHING TIME, t_{off}	Sourcing Outputs, I_{OUT} = 1A		70		ns
	Sinking Outputs, I_{OUT} = 1A		70		ns
MINIMUM INPUT PULSE WIDTH, t_p (DIGITAL MODE)			100		ns
PWM FREQUENCY (DIGITAL MODE)				500	KHz
REFERENCE VOLTAGE		2.4	2.5	2.6	V
Vref OUTPUT CURRENT (Vref 2.5V)	Source Only, No current sink capability			1	mA
ANALOG INPUT RANGE FOR FULL MODULATION	Load Current = 400µA	1		4	V
HIGH CURRENT SHUTDOWN RESPONSE	Output shorted (No bypass capacitor at SCin pin)		250	800	ns

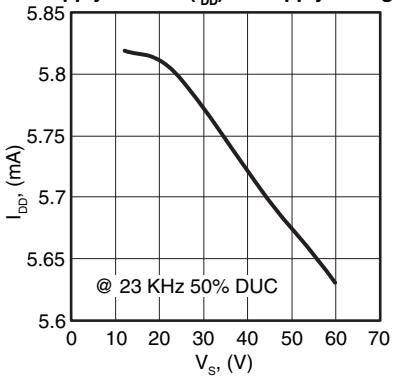
PRELIMINARY

NOTE: These specifications apply for V_S = 50V and V_{DD} = 5V at 25°C, unless otherwise specified.

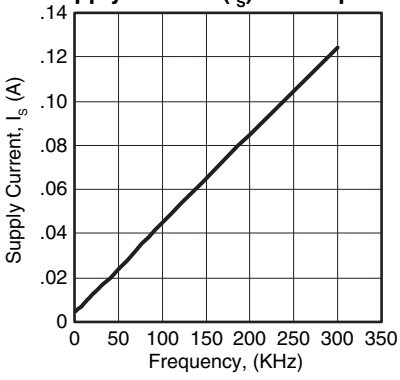
Supply Current (I_S) vs Supply Voltage (V_S)



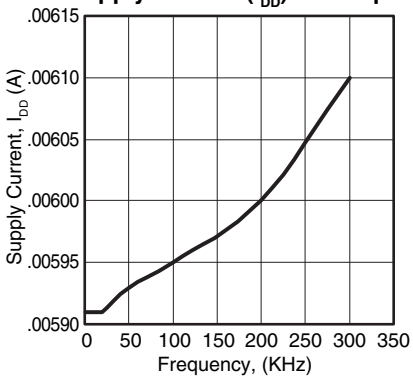
5V Supply Current (I_{DD}) vs Supply Voltage (V_S)



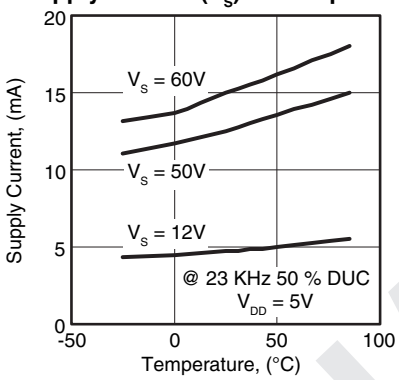
Supply Current (I_S) vs Frequency



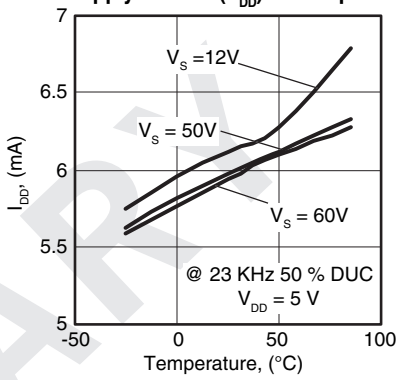
5V Supply Current (I_{DD}) vs Frequency



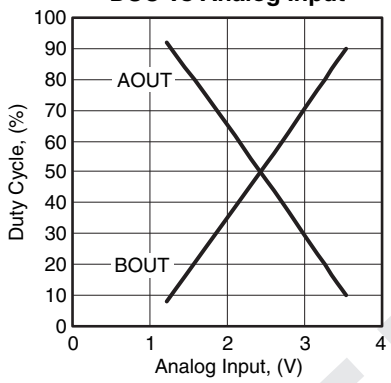
Supply Current (V_S) vs Temperature



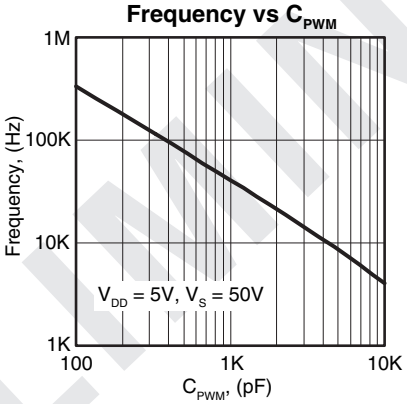
5V Supply Current (V_{DD}) vs Temperature



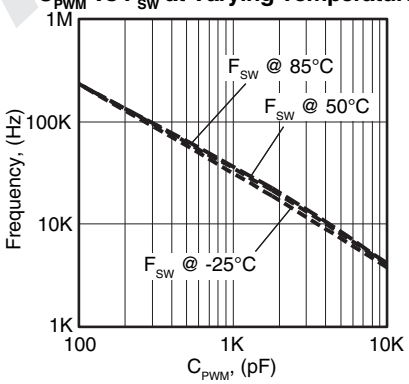
DUC vs Analog Input



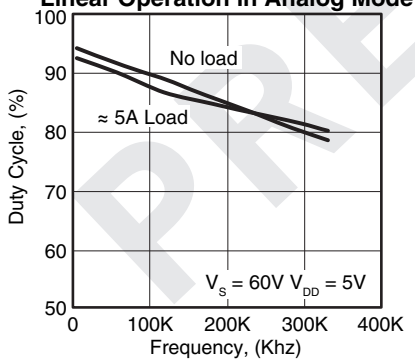
Frequency vs C_{PWM}



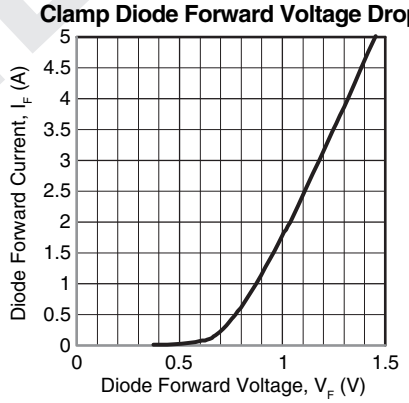
C_{PWM} vs F_{SW} at Varying Temperatures



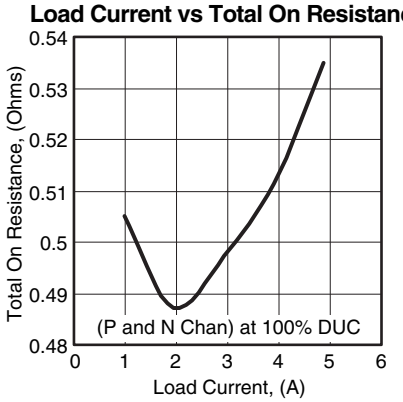
Maximum Duty Cycle for Linear Operation in Analog Mode



Clamp Diode Forward Voltage Drop

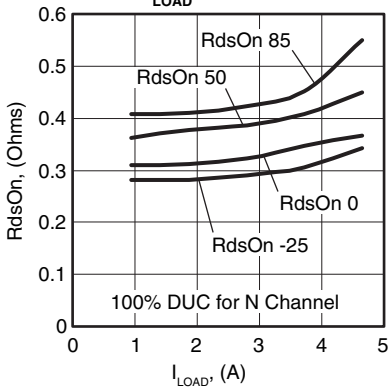


Load Current vs Total On Resistance

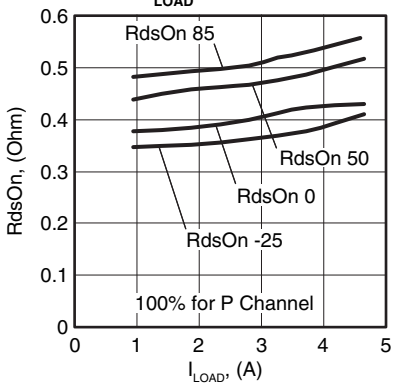


PRELIMINARY

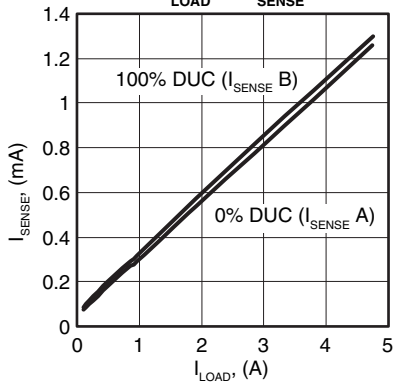
I_{LOAD} vs RdsOn



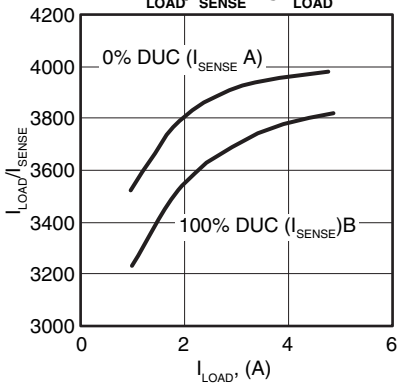
I_{LOAD} vs RdsOn



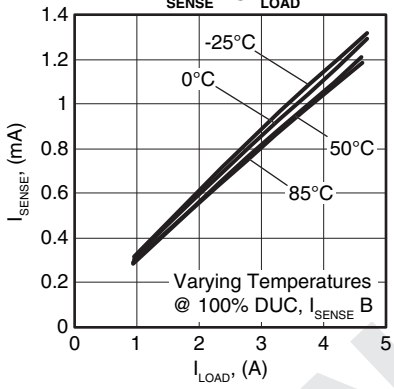
I_{LOAD} vs I_{SENSE}



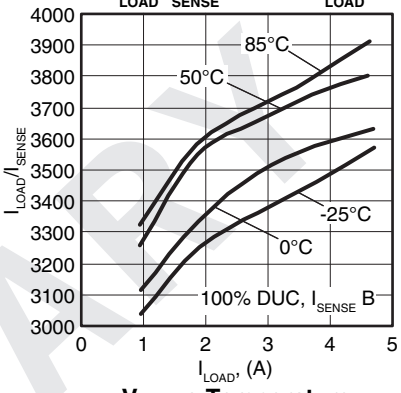
I_{LOAD}/I_{SENSE} vs I_{LOAD}



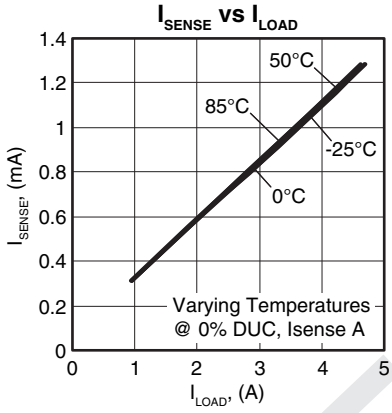
I_{SENSE} vs I_{LOAD}



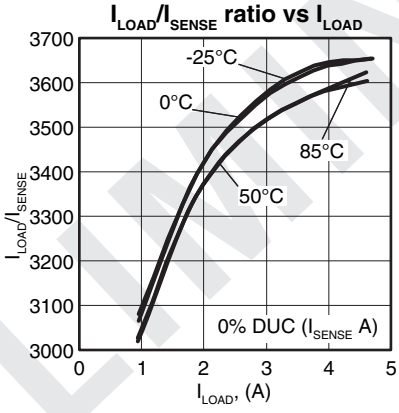
I_{LOAD}/I_{SENSE} ratio vs I_{LOAD}



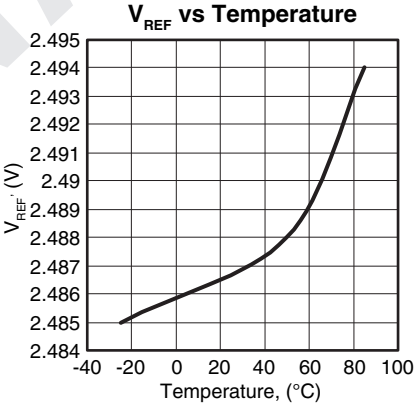
I_{SENSE} vs I_{LOAD}



I_{LOAD}/I_{SENSE} ratio vs I_{LOAD}



V_{REF} vs Temperature



PRELIMINARY

GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, power supplies, heat sinking, mounting, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex's complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

GROUND PINS

There are 4 GND pins. Pins 9 & 10 are for input signal GND and pins 1 and 23 are for power gnd.

POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals Vs and V_{DD} must be connected physically close to the pins to prevent erratic, low efficiency operation and excessive ringing at the outputs. Electrolytic capacitors, at least 10µF per output amp, are required for suppressing Vs to PGND noise. High quality ceramic capacitors (X7R) 1µF or greater should also be used. Only capacitors rated for switching applications should be considered.

The bypass capacitors must be located as close to the power supply pins as possible (due to the very fast switching times of the outputs, the inductance of 1 inch of circuit trace could cause noticeable degradation in performance). The bypassing requirements of V_{DD} are less stringent, but still necessary. A 0.1µF to 0.47µF capacitor connected directly between the V_{DD} and GND (SIG) pins will suffice.

PIN DESCRIPTIONS

Pin #	Name	Description
1,23	PGND	Power ground, high current ground return path of the motor.
2,3	Bout	Half bridge output B
4,5,19,20	VS	High voltage supply
6	SCin	Short circuit detect, CMOS. This pin can be used as a flag for a short circuit condition. Under normal operation this pin will be logic low. When a short circuit is detected, or output current exceeds approximately 10A, this pin will change to logic high and the output will be latched off. Grounding this pin disables short circuit protection. This pin should be left open if short circuit protection is desired but the flag is not used. Short circuit protection functions independently of programmable current limit (ISEN). It is nessesary to bypass the SCin pin with a 14-47pF ceramic capacitor. This capacitor will add a delay to the short circuit response but the device will still be able to protect itself against short circuit and over current.
7	TLIM	Temperature limit, CMOS. This pin can be used as a flag for an over temperature condition. Under normal operation this pin will be logic low. When junction temperature exceeds approximately 160°C this pin will change to logic high and the output will be latched off. Grounding this pin disables over temperature protection. This pin should be left open if over temperature protection is desired but the flag is not used.
8	ISEN/ /ILIM	Current Sense output and programmable current limit. A current proportional to output current is sourced by this pin. Typically this pin is connected to a resistor for programmable current limit or transconductance operation.
9,10	GND(Sig)	Ground connection for all internal digital and low current analog circuitry.
11	FAULT	Protection circuit flag output, CMOS. The fault pin will be logic high when the output MOSFETs have been automatically latched off because of a short circuit or over temperature condition. This pin should be left open if not used.
12	CPWM	An external timing capacitor is connected to this pin to set the frequency of the internal oscillator and ramp generator for analog control mode. The capacitor value (pF) = $4.05 \times 10^7 / F_{SW}$, where F_{SW} = the desired switching frequency. This pin is grounded for digital control mode.
13,14	VDD	5V supply for input logic and low voltage analog circuitry.
15	VREF	Reference voltage. Can be used at low current for biasing analog loop circuits.
16	DIR	Direction logic input, CMOS/TTL. Determines the active output MOSFETs in two quadrant digital control mode. This pin should be grounded for analog control mode.
17	PWM	CMOS/TTL input for digital PWM control, or 1-4V analog input for duty cycle control in analog control mode.
18	DISABLE	Disable logic input, CMOS/TTL. Logic low on this pin allows the SA56 to function normally. When pulled to logic high, all four output MOSFETs are disabled. Pulling this pin high, then low will reset a latched fault condition caused by a short circuit or over temperature fault.
21,22	Aout	Half bridge output A

PRELIMINARY

MODES OF OPERATION

The following chart shows the four modes of operation.

Mode	CPWM	PWM	DIR	Aout	Bout
2 Quad Digital	GND	Modulation In	High	High	$\overline{PWM}$
2 Quad Digital	GND	Modulation In	Low	$\overline{PWM}$	High
4 Quad Digital	GND	High	Modulated In	DIR	$\overline{DIR}$
4 Quad Analog	Add Cap. to set Frequency	Drive with analog signal	Not used but GND	Greater than 50% high for a low input	Greater than 50% high for a high input

ANALOG INPUT OPERATION

The SA56 can operate with analog or digital inputs. In the analog mode, the capacitor from CPWM to GND (SIG) sets the frequency of an internal triangular ramp signal. An analog input at the PWM pin is compared to the ramp to generate the duty cycle of the output. In Analog mode, the digital input on the DIR pin is ignored, though this pin should never be left floating.

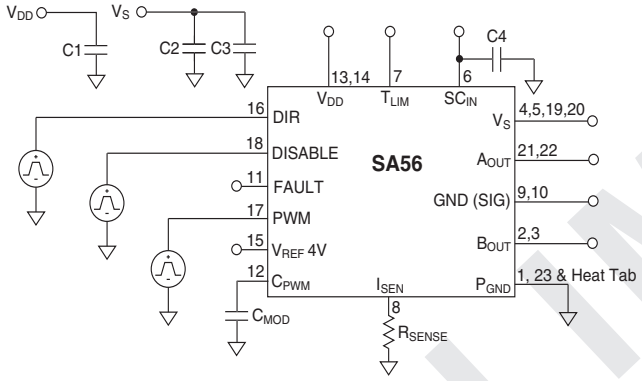


FIGURE 2. ANALOG INPUT OPERATION

OPERATING WITH DIGITAL INPUTS

Two and 4 quadrant operation are possible with the SA56 when driven with a digital PWM signal from a microcontroller or DSP. When using a digital modulation signal, tie the CPWM pin to GND to disable the internal oscillator and ramp generator.

When operating in the digital mode, pulse widths should be no less than 100ns and the switching frequency should remain less than 500KHz. This will allow enough time for the output MOSFETs to reach their full on/off state before receiving a command to reverse state.

2 QUADRANT DIGITAL MODE

For sign/magnitude (2 quadrant) operation, two digital input signals are required. A digital PWM signal to the PWM pin can control the output duty cycle at one output pin with the other output pin held "HIGH". The digital input on the DIR pin will control direction by selecting the outputs that switch according to the PWM input. If DIR is a logic "HIGH", the A output will be held "HIGH" and the B output will be switched as the inverse of the PWM input signal. If DIR is logic "LOW", the B output will be held "HIGH" and the A output will be switched. Operating in 2 quadrant mode reduces switching noise and power dissipation, but limits the control of the motor at very low speed.

A braking function can be achieved by holding the PWM input "LOW", which will turn both of the upper MOSFETs on, rapidly reducing the circulating current of the motor winding.

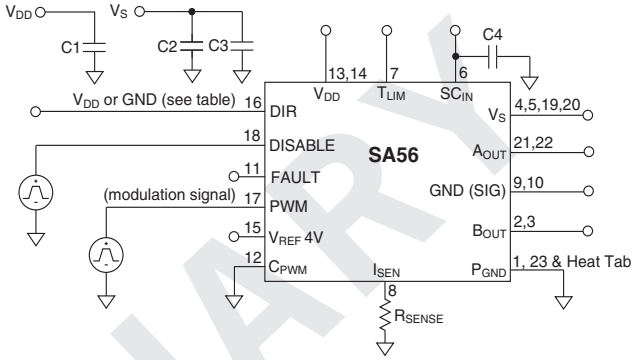


FIGURE 3. 2 QUADRANT DIGITAL MODE

4 QUADRANT DIGITAL MODE

During 4 quadrant operation a single digital PWM input includes magnitude and direction information. The digital PWM input signal is applied to the DIR pin and the PWM/INPUT pin is tied to "HIGH". Both pairs of output MOSFETs will switch in a locked anti-phase fashion from 0-100% duty cycle. With a 50% duty cycle the average voltage of each output will be half of Vs, and the differential voltage applied to the load will be zero. Four quadrant operation allows smooth transitions through zero current for position servos and low speed applications. Power dissipation is slightly higher since all four output MOSFETs switch every cycle.

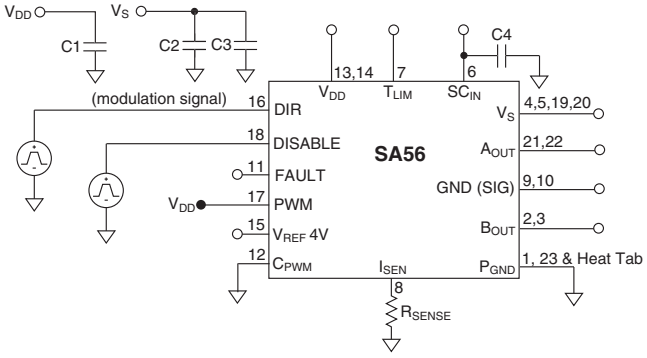


FIGURE 4. 4 QUADRANT DIGITAL MODE

PRELIMINARY

PROTECTION CIRCUITS

Thermal and short circuit protection are included in the SA56 to prevent damage during fault conditions. High current protection circuits will sense a direct short from either output to GND or Vs as well as across the load. The thermal protection will engage when the temperature of the MOSFETs reach approximately 160°C. The FAULT output pin will go "HIGH" if either protection circuits engages and will place all MOSFETs in the "OFF" state (high impedance output). The SC or T_{LIM} output will also go "HIGH", to indicate which of the protection features has been triggered. The fault going high disables the 4 output transistors. To reset the fault condition, cycle the V_{DD} power or bring the DISABLE pin "HIGH" then "LOW".

The most severe condition for any power device is a direct, hard-wired ("screwdriver") short from an output to ground. While the short circuit protection will latch the output MOSFETs within 250ns (typical) the die and package may be required to dissipate up to 600 Watts of power until the protection is engaged. This energy can be destructive, particularly at higher operating voltages, so good thermal design is critical if such fault tolerance is required of the system.

PROGRAMMABLE CURRENT LIMIT

The ISEN pin sources a current proportional to the forward output current of the active P channel output MOSFET. The proportionality is 300µA (nom) per ampere of output current. The ISEN output is blocked during the switching transitions when current spikes can be significant.

To create a programmable current limit, connect a resistor from ISEN out to GND. When the voltage across this resistor exceeds internally generated 2.75V threshold, all 4 output MOSFETs will be turned off for the remainder of the switching cycle. A 2.75KΩ resistor will set the current limit to approximately 5 Amps.

The ISEN output can also be used for maintaining a current control loop in torque motor applications.

CURRENT SENSE LINEARITY CALCULATION

The current sense linearity is calculated using the method described below:

a) Define straight line (y = mx + c) joining the two end data points where, m is the slope and c is the offset or zero crossover. Calculate the slope m and offset c using the extreme data points. Assume Isense in the y axis and Iload in the x axis.
b) Calculate linear Isense (or ideal Isense value, IS_{IDEAL}) using the straight line equation derived in step (a) for the Iload data points.
c) Determine deviation from linear Isense (step (b)) and actual measured Isense value (IS_{ACTUAL}) as shown below:

$$\% \text{ Deviation from Linearity} = \frac{IS_{IDEAL} - IS_{ACTUAL}}{IS_{IDEAL}} \bullet 100$$

IC REV C ERRATA INFORMATION

This document describes the errata information for SA56 rev C full H-Bridge DC motor driver. Rev C parts can be identified by date code 0206 marked on the EX package.

Errata Number and Date	Description	Impact
1 Dated: 3/3/06	TLIM pin: This pin is modified to serve as a flag for any fault occurrence including short-circuit, over current and over temperature.	Impact: Grounding the TLIM pin disables all fault protection mechanisms in the SA56 including SC, over current and over temp. This pin should be left floating at all times unless the user desires to disable all protection mechanisms.

Note: The errata items described in the table above are strictly for beta samples and will be rectified to conform to SA56U specifications for the production parts.

PRELIMINARY