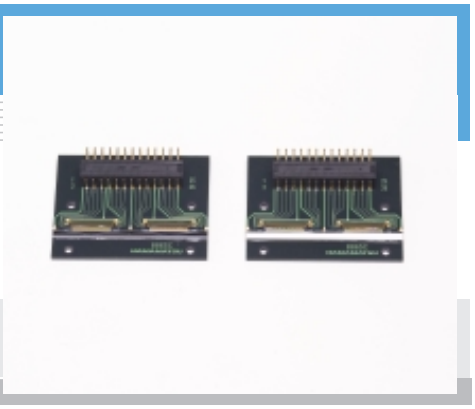
Photodiode array with amplifier
S8865-256, S8865-256G



Photodiode array combined with signal processing circuit chip

S8865-256 and S8865-256G are Si photodiode arrays combined with a signal processing circuit chip. The signal processing circuit chip is formed by CMOS process and incorporates a timing generator, shift register, charge amplifier array, clamp circuit and hold circuit, making the external circuit configuration simple. A long, narrow image sensor can also be configured by arranging multiple arrays in a row. For X-ray detection applications, types with fluorescent paper affixed on the active area are also available.

Features

- Element pitch: 0.2 mm pitch × 256 ch
- 5 V power supply operation
- Simultaneous integration by using a charge amplifier array
- Sequential readout with a shift register (Data rate: 1 MHz Max.)
- Low dark current due to zero-bias photodiode operation
- Integrated clamp circuit allows low noise and wide dynamic range
- Integrated timing generator allows operation at two different input pulse timings (reset, clock)
- Types with phosphor screen affixed on the active area are available for X-ray detection: S8865-256G

Applications

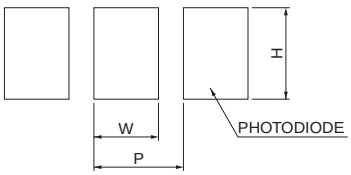
- Long line sensors
- Line sensors for X-ray detection

■ Specifications of active area

Parameter	Symbol *1	Value	Unit
Element pitch	P	0.2	mm
Element width	W	0.1	mm
Element height	H	0.3	mm
Number of elements	-	256	-
Active area length	-	51.2	mm

*1: Refer to following figure.

■ Enlarged view of active area



KMPDC0072EB

SOLID STATE DIVISION

■ Absolute maximum ratings

Parameter	Symbol	Rated value	Unit
Supply voltage	Vdd	-0.3 to +6	V
Reference voltage	Vref	-0.3 to +6	V
Photodiode voltage	Vpd	-0.3 to +6	V
Gain selection terminal voltage	Vgain	-0.3 to +6	V
Master/slave selection voltage	Vms	-0.3 to +6	V
Clock pulse voltage	V (CLK)	-0.3 to +6	V
Reset pulse voltage	V (RESET)	-0.3 to +6	V
External start pulse voltage	V (EXTST)	-0.3 to +6	V
Operating temperature *2	Topr	-5 to +60	°C
Storage temperature	Tstg	-10 to +70	°C

*2: No condensation

■ Recommended terminal voltage

Parameter		Symbol	Min.	Typ.	Max.	Unit
Supply voltage		Vdd	4.75	5	5.25	V
Reference voltage		Vref	4	4.5	4.75	V
Photodiode voltage		Vpd	-	Vref	-	V
Gain selection terminal voltage	High gain	Vgain	Vdd-0.25	Vdd	Vdd+0.25	V
	Low gain		0	-	0.4	V
Master/slave selection voltage	High level *3	Vms	Vdd-0.25	Vdd	Vdd+0.25	V
	Low level *4		0	-	0.4	V
Clock pulse voltage	High level	V (CLK)	Vdd-0.25	Vdd	Vdd+0.25	V
	Low level		0	-	0.4	V
Reset pulse voltage	High level	V (RESET)	Vdd-0.25	Vdd	Vdd+0.25	V
	Low level		0	-	0.4	V
External start pulse voltage	High level	V (EXESP)	Vdd-0.25	Vdd	Vdd+0.25	V
	Low level		0	-	0.4	V

*3: Parallel
*4: Serial at 2nd or later stages

■ Electrical characteristics [Ta=25 °C, Vdd=5 V, V (CLK)=V (RESET)=5 V]

Parameter		Symbol	Min.	Typ.	Max.	Unit
Clock pulse frequency *5		f (CLK)	40	-	4000	kHz
Output impedance		Zo	-	3	-	kΩ
Power consumption		P	-	360	-	mW
Charge amp feedback capacitance	High gain	Cf	-	0.5	-	pF
	Low gain		-	1	-	

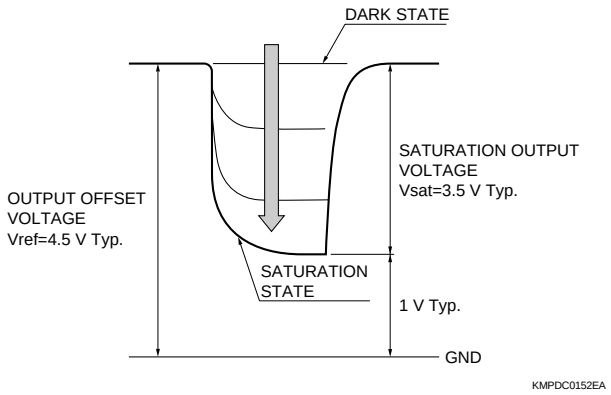
*5: Video data rate is 1/4 of clock pulse frequency f (CLK).

■ Electrical/optical characteristics [Ta=25 °C, Vdd=5 V, V (CLK)=V (RESET)=5 V, Vgain=5 V (High gain), 0 V (Low gain)]

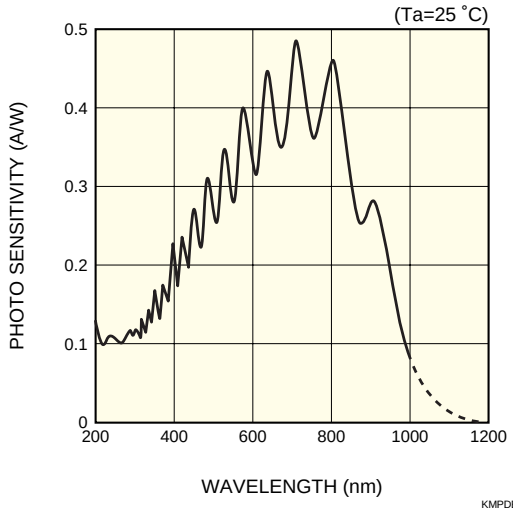
Parameter		Symbol	Min.	Typ.	Max.	Unit
Spectral response range		λ		200 to 1000		nm
Peak sensitivity wavelength		λp	-	720	-	nm
Dark output voltage *6	High gain	Vd	-	0.002	0.02	mV
	Low gain		-	0.001	0.01	
Saturation output voltage		Vsat	3	3.5	-	V
Saturation exposure *7	High gain	Esat	-	15	-	$mlx \cdot s$
	Low gain		-	30	-	
Photo sensitivity	High gain	S	-	250	-	$V/lx \cdot s$
	Low gain		-	125	-	
Photo response non-uniformity *8		PRNU	-	-	±10	%
Noise *9	High gain	N	-	0.6	-	mVrms
	Low gain		-	0.3	-	
Output offset voltage *10		Vos	-	Vref	-	V

*6: Integration time ts=1 ms
*7: Measured with a 2856 K tungsten lamp
*8: When the photodiode array is exposed to uniform light which is 50 % of the saturation exposure, the Photo Response Non-Uniformity (PRNU) is defined as follows:
PRNU = ΔX/X × 100 (%)
where X is the average output of all elements and ΔX is the difference between the maximum and minimum outputs.
*9: Measured with a video data rate of 50 kHz and Ts=1 ms in dark state
*10: Video output is negative-going output with respect to the output offset voltage.

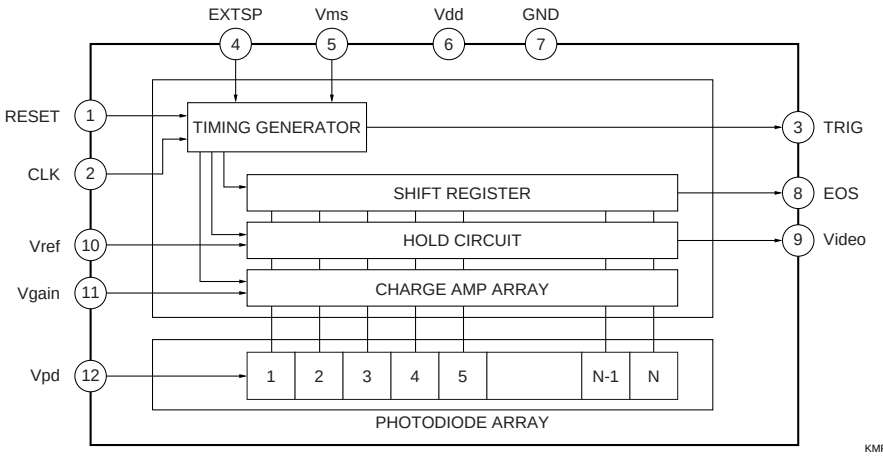
■ Output waveform of one element



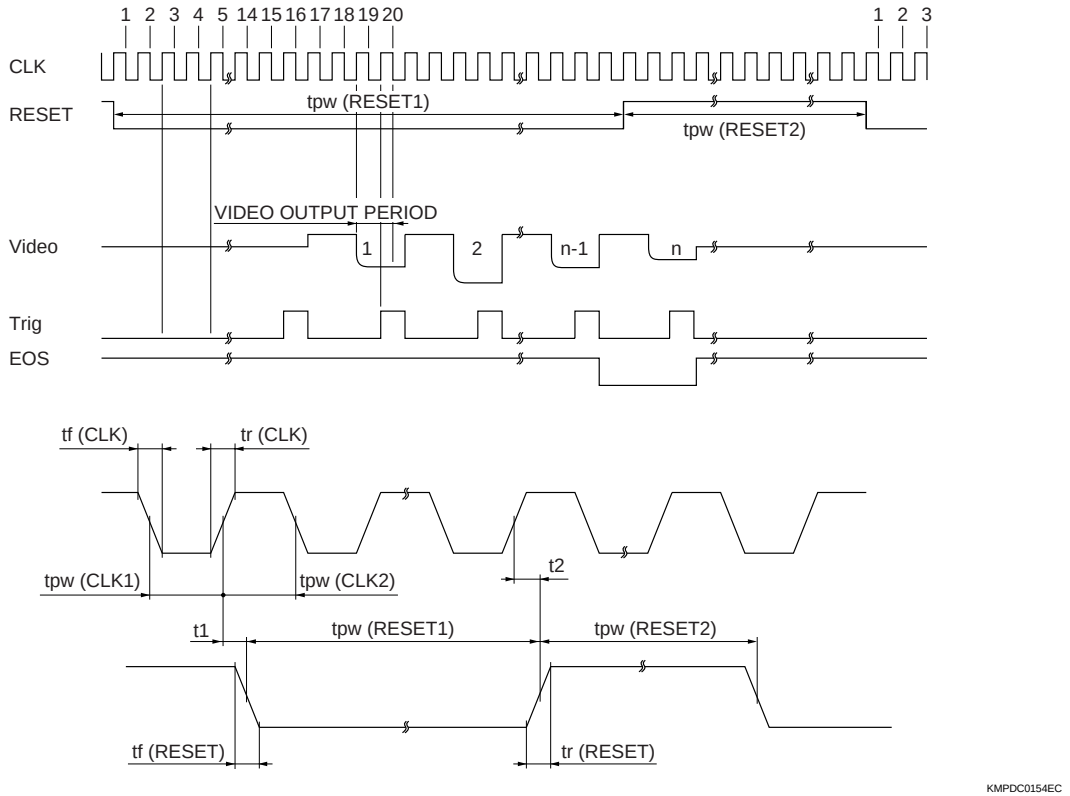
■ Spectral response (measurement example)



■ Block diagram



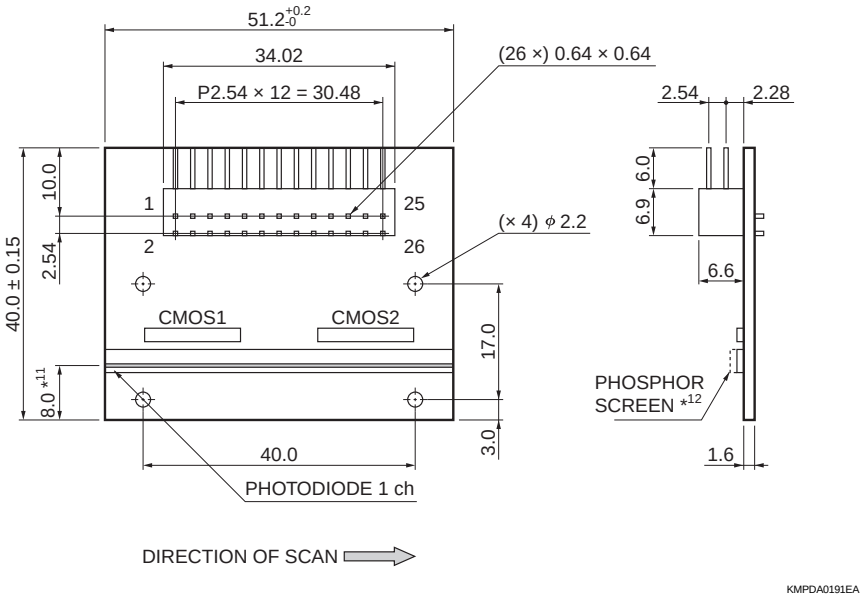
■ Timing chart



Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock pulse width	tpw (CLK1), tpw (CLK2)	125	-	12500	ns
Clock pulse rise/fall times	tr (CLK), tf (CLK)	0	20	30	ns
Reset pulse width 1	tpw (RESET1)	10	-	-	µs
Reset pulse width 2	tpw (RESET2)	20	-	-	µs
Reset pulse rise/fall times	tr (RESET), tf (RESET)	0	20	30	ns
Clock pulse-reset pulse timing 1	t1	-20	0	20	ns
Clock pulse-reset pulse timing 2	t2	-20	0	20	ns

1. The internal timing circuit starts operation at a fall of CLK immediately after a RESET pulse sets to Low.
2. When a fall of CLK is counted as "1 clock", the video signal at the 1st channel appears between "18.5 clocks and 20 clocks". Then a video signal appears every 4 clocks.
3. Signal charge integration time equals the High period of a RESET pulse. However, the charge integration does not start at the rise of a RESET pulse but starts at the 8th clock after the rise of the RESET pulse and ends at the 8th clock after the fall of the RESET pulse. Signals integrated within this period are sequentially read out as time-series signals by the shift register operation when the RESET pulse next changes from High to Low. The rise and fall of a RESET pulse must be synchronized with the fall of a CLK pulse, but the rise of a RESET pulse must be set outside the video output period. One cycle of RESET pulses cannot be set shorter than the time equal to "(video signal readout period 16.5 + 4) × N (number of pixels)" clocks.

■ Dimensional outline (unit: mm)



*11: Distance from the bottom of the board to the center of active area
Board: G10 glass epoxy
Connector: JAE (Japan Aviation Electronics Industry, Limited)
PS-26PE-D4LT1-PN1

*12: Photodiode array with phosphor screen: S8865-256G only
· Material Gd_2O_2S: Tb
· Phosphor thickness 300 µm Typ.
· Detectable energy range 30k to 100 keV

■ Pin connection

Pin No.	CMOS1	Pin No.	CMOS2	Name	Note
1	Vpd	14	Vpd	Photodiode voltage	Voltage input
2	RESET	15	RESET	Reset pulse	Pulse input
3	CLK	16	CLK	Clock pulse	Pulse input
4	Trig	17	Trig	Trigger pulse	Positive-going pulse output
5	EXTSP	18	EXTSP	External start pulse	Pulse input
6	Vms	19	Vms	Master/slave selection supply voltage	Voltage input
7	Vdd	20	Vdd	Supply voltage	Voltage input
8	GND	21	GND	Ground	
9	EOS	22	EOS	End of scan	Negative-going pulse output
10	Video	23	Video	Video output	Negative-going output with respect to Vref
11	Vref	24	Vref	Reference voltage	Voltage input
12	Vg	25	Vg	Gain-selection terminal voltage	Voltage input
13	Vpd	26	Vpd	Photodiode voltage	Voltage input

■ Gain selection terminal voltage setting

Vdd: High gain (Cf: 0.5 pF) GND: Low gain (Cf: 1 pF)

■ Readout methods and settings

Signals of channels 1 through 126 are output from CMOS1, while signals of channels 129 through 256 are output from CMOS2. The following two readout methods are available.

(1) Serial readout method

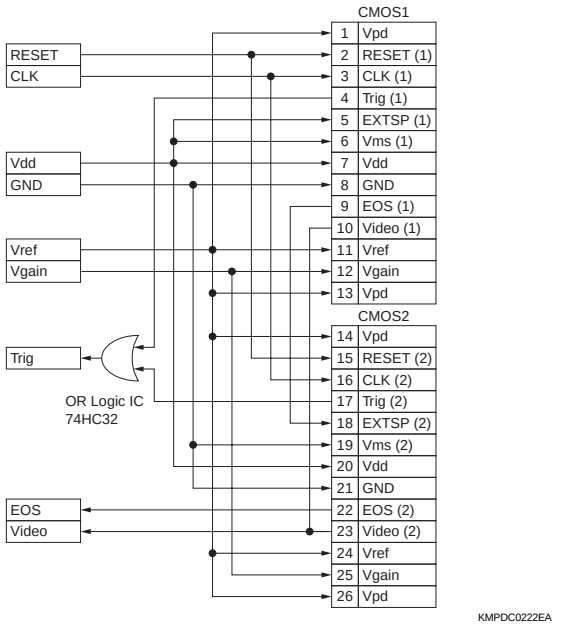
CMOS1 and CMOS2 are connected in serial and the signals of channels 1 through 256 are sequentially read out from one output line. Set CMOS1 as in “A” in the table below, and set CMOS2 as in “B”. CMOS1 and CMOS2 should be connected to the same CLK and RESET lines, and their video output terminals to one line.

(2) Parallel readout method

128 channel signals are output in parallel respectively from the output lines of CMOS1 and CMOS2. Set both CMOS1 and CMOS2 as in “A” in the table below.

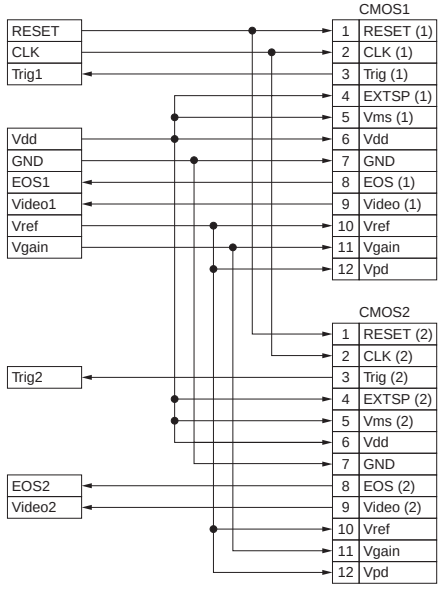
■ Connection example

Serial readout method



KMPDC0222EA

Parallel readout method



KMPDC0223EA

Type	Vms	EXTSP
A	Vdd	Vdd
B	GND	Preceding sensor EOS should be input

■ Readout circuit

Check that pulse signals meet the required pulse conditions before supplying them to the input terminals.
Video output should be amplified by an operational amplifier that is connected close to the sensor.

■ Cautions during use

(1) The signal processing circuit chips of S8865 series are protected against static electricity. However, in order to prevent possible damage to the chip, implement electrostatic countermeasures such as grounding of the operator, work table and tools. Furthermore, the devices must be protected against surge voltages from external equipment.

(2) Since the photodiode array chip is not protected, handle it carefully so it will not become contaminated or scratched. Photodiode array performance may deteriorate if operated at high temperatures and humidity, so the housing should be designed to be airtight. The signal processing circuit chip and its wire bonding are covered with a resin coating for protection, but never touch these portions. In addition, take care when installing the board so that it does not warp.

(3) S8865-256G

Signal processing IC chip performance will drop if subjected to X-rays. Protect the IC chip from X-rays by installing a lead shield.

HAMAMATSU
Information furnished by HAMAMATSU is believed to be reliable. However, no responsibility is assumed for possible inaccuracies or omissions.
Specifications are subject to change without notice. No patent rights are granted to any of the circuits described herein. ©2006 Hamamatsu Photonics K.K.

HAMAMATSU PHOTONICS K.K., Solid State Division
1126-1 Ichino-cho, Higashi-ku, Hamamatsu City, 435-8558 Japan, Telephone: (81) 53-434-3311, Fax: (81) 53-434-5184, www.hamamatsu.com
U.S.A.: Hamamatsu Corporation: 360 Foothill Road, P.O.Box 6910, Bridgewater, N.J. 08807-0910, U.S.A., Telephone: (1) 908-231-0960, Fax: (1) 908-231-1218
Germany: Hamamatsu Photonics Deutschland GmbH: Arzbergerstr. 10, D-82211 Herrsching am Ammersee, Germany, Telephone: (49) 08152-3750, Fax: (49) 08152-2658
France: Hamamatsu Photonics France S.A.R.L.: 19, Rue du Saule Trapu, Parc du Moulin de Massy, 91882 Massy Cedex, France, Telephone: 33-(1) 69 53 71 00, Fax: 33-(1) 69 53 71 10
United Kingdom: Hamamatsu Photonics UK Limited: 2 Howard Court, 10 Tewin Road, Welwyn Garden City, Hertfordshire AL7 1BW, United Kingdom, Telephone: (44) 1707-294888, Fax: (44) 1707-325777
North Europe: Hamamatsu Photonics Norden AB: Smidesvägen 12, SE-171 41 Solna, Sweden, Telephone: (46) 8-509-031-00, Fax: (46) 8-509-031-01
Italy: Hamamatsu Photonics Italia S.R.L.: Strada della Moia, 1/E, 20020 Arese, (Milano), Italy, Telephone: (39) 02-935-81-733, Fax: (39) 02-935-81-741

Cat. No. KMPD1087E01
Jul. 2006 DN