S71GL-N Based MCPs

Stacked Multi-Chip Product (MCP)
Flash Memory and RAM
64/32 Megabit (4/2 M x 16-bit) CMOS 3.0 Volt-only Page Mode Flash Memory and 32/16/8/4 Megabit (2M/1M/512k/256k x 16-bit) Pseudo Static RAM

Data Sheet *(Advance Information)*

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Publication Number S71GL-N_00 **Revision** 03 **Issue Date** March 25, 2008

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Distinctive Characteristics

MCP Features

- **Power supply voltage of 2.7 to 3.1 volt**
- **High performance**
  - 90 ns access time (90 ns Flash, 70 ns pSRAM/SRAM)
  - 25 ns page read times
- **Packages**
  - 7 x 9 x 1.2 mm 56 ball FBGA (TLC056)
- **Operating Temperature**
  - –25°C to +85°C

General Description

The S71GL-N product series consists of S29GL-N Flash memory with pSRAM combinations defined as:

		Flash Memory Density	
		32 Mb	**64 Mb**
pSRAM Density	4 Mb	S71GL032N40	
	8 Mb	S71GL032N80	
	16 Mb	S71GL032NA0	S71GL064NA0
	32 Mb		S71GL064NB0

For detailed specifications, please refer to the individual data sheets.

Document	Publication Identification Number (PID)
S29GL-N	S29GL-N_00
4 Mb pSRAM Type 9	pSRAM_33
8 Mb pSRAM Type 9	pSRAM_34
16 Mb pSRAM Type 7	pSRAM_13
32 Mb pSRAM Type 8	pSRAM_31

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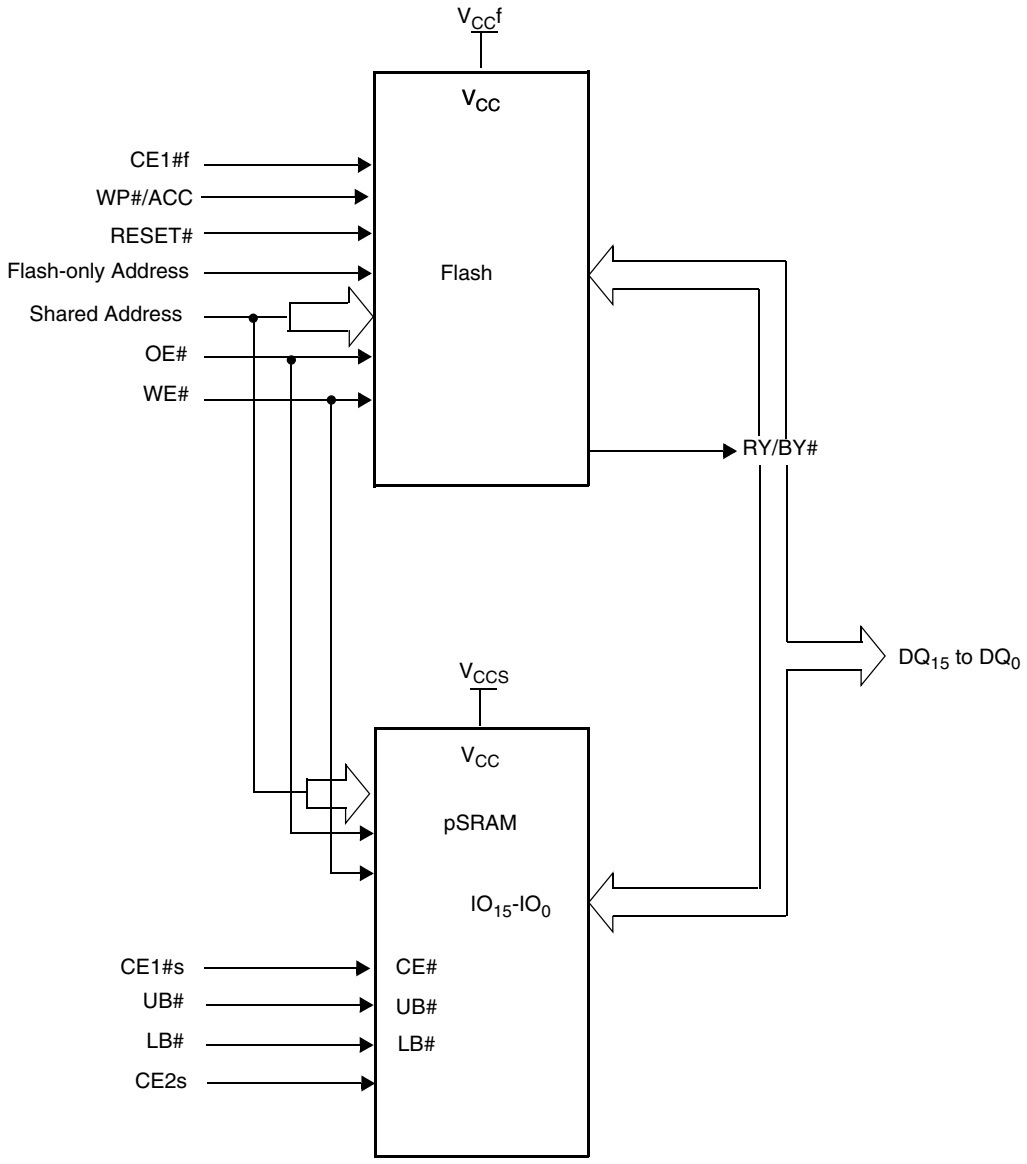
1. Product Selector Guide

1.1 64 Mb Flash Memory

Device-Model# (Note)	Flash Access time (ns)	(p)SRAM density	(p)SRAM Access time (ns)	(p)SRAM type	Package
S71GL032N40-0K	90	4 Mb	70	pSRAM 9	TLC056
S71GL032N40-0P					
S71GL032N80-0K		8 Mb			
S71GL032N80-0P					
S71GL032NA0-0U		16 Mb		pSRAM7	
S71GL032NA0-0Z					
S71GL064NA0-0U					
S71GL064NA0-0Z					
S71GL064NB0-0U		32 Mb		pSRAM 8	
S71GL064NB0-0Z					

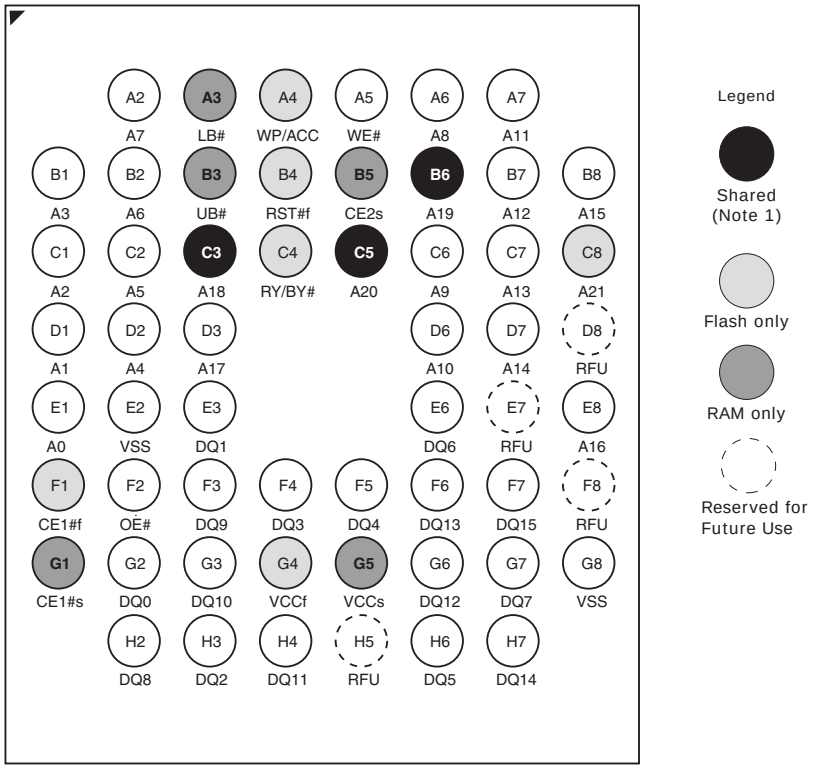
Note
Please see the valid combinations table for the model# description.

2. MCP Block Diagram



3. Connection Diagram

56-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)



Note
May be shared depending on density.

MCP	Flash-only Addresses	Shared Addresses
S71GL032NA0	A20	A19-A0
S71GL032N80	A20-A19	A18-A0
S71GL032N40	A20-A18	A17-A0
S71GL064NB0	A21	A20-A0
S71GL064NA0	A21-A20	A19-A0

3.1 Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

4. Pin Description

Pin	Description
A21–A0	22 Address Inputs (Common and Flash only) (A20-A0 for the S71GL032N)
DQ15–DQ0	16 Data Inputs/Outputs (Common)
CE1#f	Chip Enable (Flash)
CE1#s	Chip Enable 1 (pSRAM/SRAM)
CE2s	Chip Enable 2 (pSRAM/SRAM)
OE#	Output Enable (Common)
WE#	Write Enable (Common)
RY/BY#	Ready/Busy Output (Flash 1)
UB#	Upper Byte Control (pSRAM/SRAM)
LB#	Lower Byte Control (pSRAM/SRAM)
RESET#	Hardware Reset Pin, Active Low (Flash)
WP#/ACC	Hardware Write Protect/Acceleration Pin (Flash)
$V_{CC}f$	Flash 3.0 volt-only single power supply (see *Product Selector Guide* for speed options and voltage supply tolerances)
V_{CCS}	pSRAM/SRAM Power Supply
V_{SS}	Device Ground (Common)
NC	Pin Not Connected Internally

5. Ordering Information

The order number is formed by a valid combinations of the following:

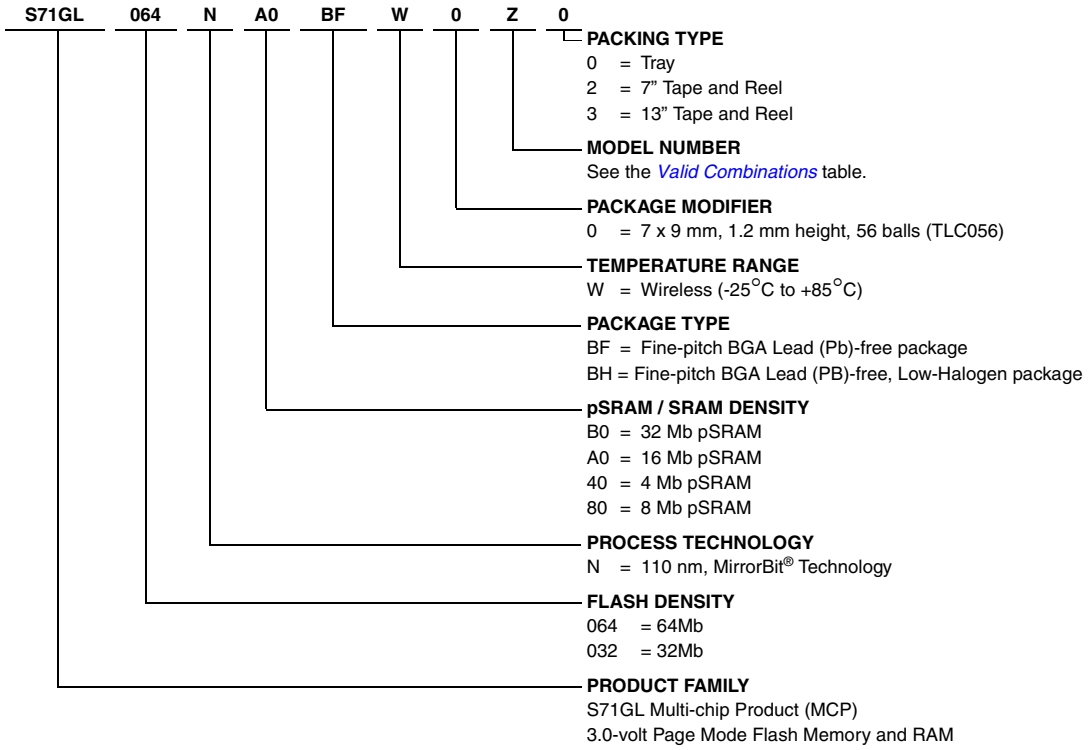


Table 5.1 Valid Combinations

S71GL064N Valid Combinations				Speed Options (ns)/Boot Sector Option	(p)SRAM Type/ Access Time (ns)	Package Marking
Base Ordering Part Number	Package & Temperature	Package Modifier/Model Number	Packing Type			
S71GL032N40	BFW, BHW	0K	0, 2, 3 (1)	90 / Bottom Boot Sector	pSRAM9 / 70	TLC056
		0P		90 / Top Boot Sector		
S71GL032N80		0K		90 / Bottom Boot Sector	pSRAM9 / 70	
		0P		90 / Top Boot Sector		
S71GL032NA0		0U		90 / Bottom Boot Sector	pSRAM7 / 70	
		0Z		90 / Top Boot Sector		
S71GL064NA0		0U		90 / Bottom Boot Sector	pSRAM7 / 70	
S71GL064NA0		0Z		90 / Top Boot Sector		
S71GL064NB0		0U		90 / Bottom Boot Sector	pSRAM8 / 70	
S71GL064NB0		0Z		90 / Top Boot Sector		

Note

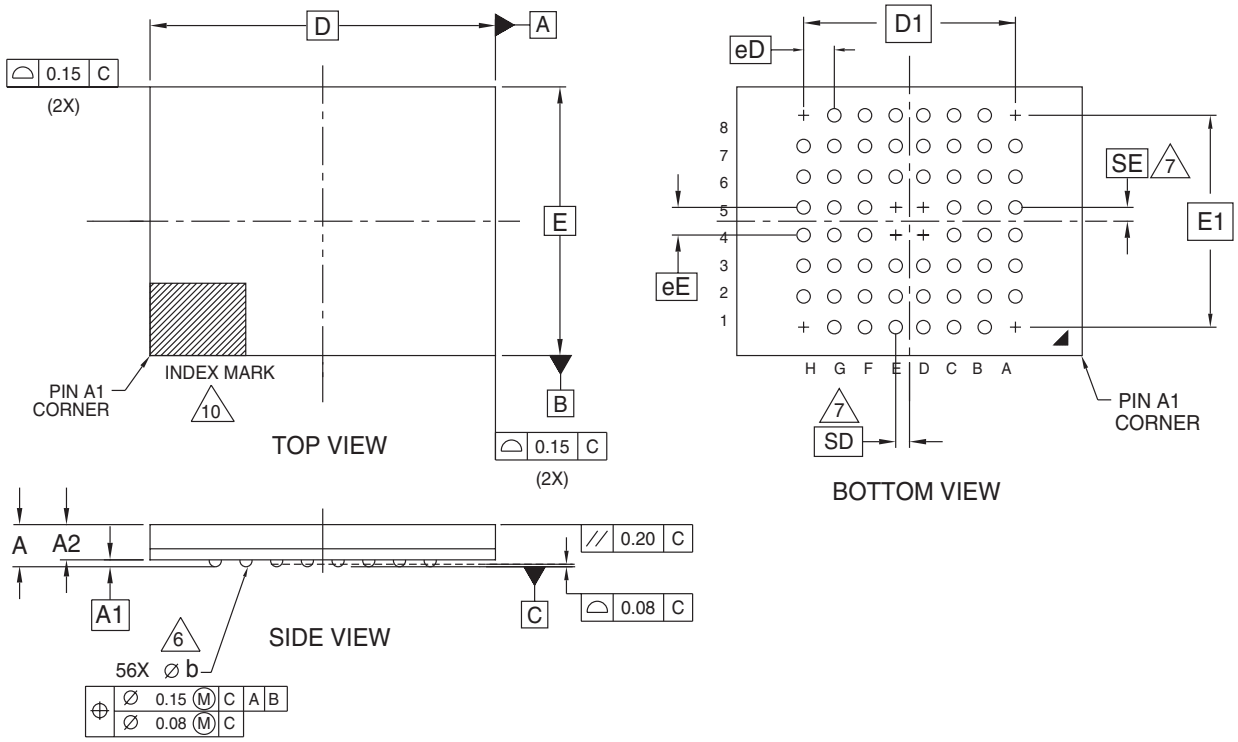
1. Type 0 is standard. Specify other options as required.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

6. Physical Dimensions

6.1 TLC056—56-ball Fine-Pitch Ball Grid Array (FBGA) 9 x 7 mm Package



PACKAGE	TLC 056			
JEDEC	N/A			
D x E	9.00 mm x 7.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		9.00 BSC.		BODY SIZE
E		7.00 BSC.		BODY SIZE
D1		5.60 BSC.		MATRIX FOOTPRINT
E1		5.60 BSC.		MATRIX FOOTPRINT
MD		8		MATRIX SIZE D DIRECTION
ME		8		MATRIX SIZE E DIRECTION
n		56		BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
		A1,A8,D4,D5,E4,E5,H1,H8		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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7. Revision History

Section	Description
Revision 01 (May 14, 2007)	
	Initial release.
Revision 02 (June 19, 2007)	
Global	Editorial changes to valid combinations table
Revision 03 (March 25, 2008)	
Ordering Information	Added Low-Halogen option to package type.

Colophon

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