S6B0728

132 SEG / 128 COM DRIVER & CONTROLLER FOR STN LCD

Jan. 2000.

Ver. 0.1

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Version	Content	Date
0.0	Original	Sep.1999
0.1	Change the supply voltage(VDD) range (2.4 to 5.5 -> 2.4 to 3.6)	Jan.2000

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INTRODUCTION

The S6B0728 is a driver and controller LSI for graphic dot-matrix liquid crystal display systems. It contains 128 common and 132 segment driver circuits. It is connected directly to a microprocessor, accepts serial or 8-bit parallel display data and stores in an on-chip display data RAM of 128 x 132 bits. It provides a highly flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. And it performs display data RAM read/write operation with no external-operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

FEATURES

Driver Output Circuits

– 128 common outputs / 132 segment outputs

Applicable Duty-ratios

Programmable duty ratio	Applicable LCD bias	Maximum display area
1/16 to 1/128	1/5 to 1/12	128 × 132

– Various partial display
– Partial window moving & data scrolling

On-chip Display Data RAM

– Capacity: 128 x 132 = 16,896 bits
– Bit data "1": a dot of display is illuminated
– Bit data "0": a dot of display is not illuminated

Microprocessor Interface

– 8-bit parallel bi-directional interface with 6800-series or 8080-series
– Serial interface(only write operation) with 4-pin or 3-pin SPI(Serial Peripheral Interface)

On-chip Low Power Analog Circuit

– On-chip oscillator circuit
– Voltage converter (x3, x4, x5, x6 or x7)
– Voltage regulator (temperature coefficient: -0.05%/°C or external input)
– On-chip electronic contrast control function (64 steps)
– Voltage follower (LCD bias: 1/5 to 1/12)

Operating Voltage Range

– Supply voltage (V_{DD}): 2.4 to 3.6 [V]
– LCD driving voltage (V_{LCD} = V0 - V_{SS}): 4.0 to 17.0 [V]

Low Power Consumption

– TBD μA Typ. (V_{DD} = 3V, x6 boosting, V0 = 15V, Internal power supply ON and display OFF)
– TBD μA Max. (during power save [standby] mode)

Package Type

– Gold bumped chip or TCP

BLOCK DIAGRAM

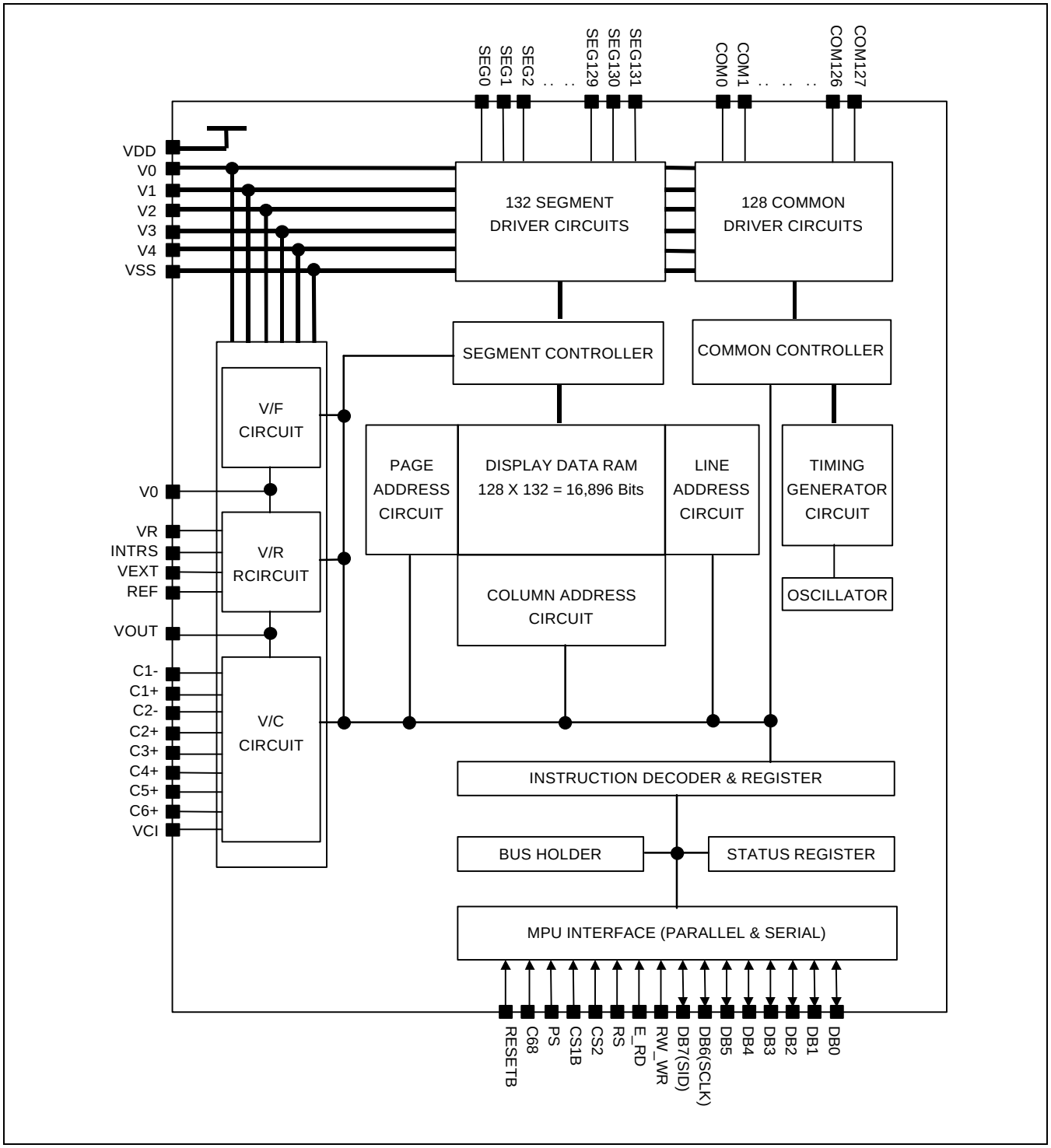


Figure 1. Block Diagram

PAD CONFIGURATION

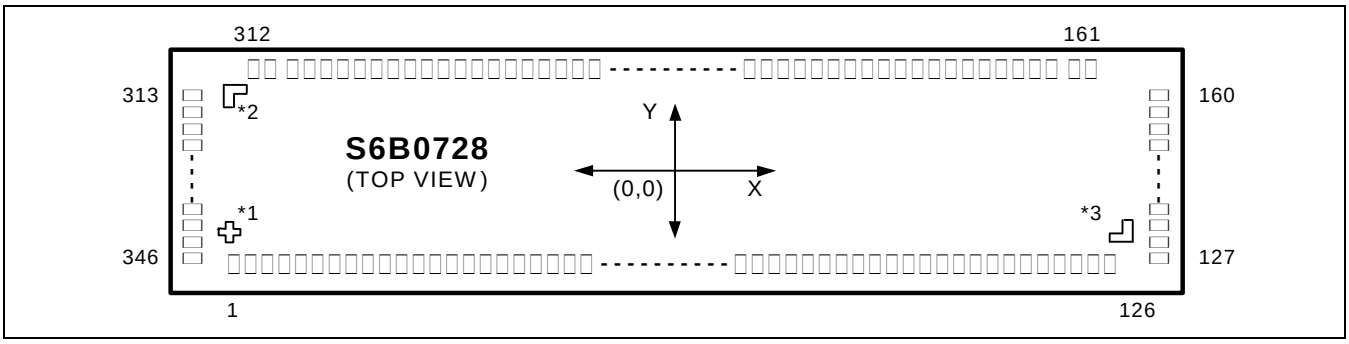
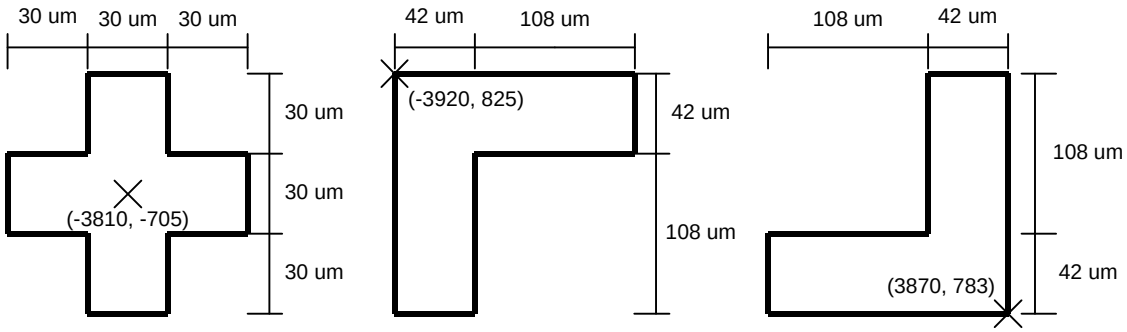


Figure 2. S6B0728 Chip Configuration

Table 1. S6B0728 Pad Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	8740	2470	mm
Pad pitch	27 to 100	70 (Min.)		
	1 to 26, 101 to 346	54 (Min.)		
Bumped pad size	27 to 100	60	78	
	128 to 159, 314 to 345	78	44	
	3 to 26, 101 to 124 163 to 310	44	78	
	1, 2, 125, 126, 160, 161, 313, 346	70	78	
	127, 162, 311, 312	78	70	
Bumped pad height	1 to 346	14 (Typ.)		



*1 : Bump Align Key

*2 : ILB Align Key 1

*3 : ILB Align Key 2

PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: μm]

NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y	NO	NAME	X	Y
1	DUMMY	-4161	-1110	51	DB6	-875	-1110	101	COM63	2759	-1110	151	COM16	4245	405
2	DUMMY	-4081	-1110	52	DB7	-805	-1110	102	COM62	2813	-1110	152	COM15	4245	459
3	COM104	-4001	-1110	53	VDD	-735	-1110	103	COM61	2867	-1110	153	COM14	4245	513
4	COM105	-3947	-1110	54	VDD	-665	-1110	104	COM60	2921	-1110	154	COM13	4245	567
5	COM106	-3893	-1110	55	VDD	-595	-1110	105	COM59	2975	-1110	155	COM12	4245	621
6	COM107	-3839	-1110	56	VDD	-525	-1110	106	COM58	3029	-1110	156	COM11	4245	675
7	COM108	-3785	-1110	57	VCI	-455	-1110	107	COM57	3083	-1110	157	COM10	4245	729
8	COM109	-3731	-1110	58	VCI	-385	-1110	108	COM56	3137	-1110	158	COM9	4245	783
9	COM110	-3677	-1110	59	VSS	-315	-1110	109	COM55	3191	-1110	159	COM8	4245	837
10	COM111	-3623	-1110	60	VSS	-245	-1110	110	COM54	3245	-1110	160	DUMMY	4245	917
11	COM112	-3569	-1110	61	VSS	-175	-1110	111	COM53	3299	-1110	161	DUMMY	4129	1110
12	COM113	-3515	-1110	62	VSS	-105	-1110	112	COM52	3353	-1110	162	DUMMY	4049	1110
13	COM114	-3461	-1110	63	VOUT	-35	-1110	113	COM51	3407	-1110	163	COM7	3969	1110
14	COM115	-3407	-1110	64	VOUT	35	-1110	114	COM50	3461	-1110	164	COM6	3915	1110
15	COM116	-3353	-1110	65	C5+	105	-1110	115	COM49	3515	-1110	165	COM5	3861	1110
16	COM117	-3299	-1110	66	C5+	175	-1110	116	COM48	3569	-1110	166	COM4	3807	1110
17	COM118	-3245	-1110	67	C3+	245	-1110	117	COM47	3623	-1110	167	COM3	3753	1110
18	COM119	-3191	-1110	68	C3+	315	-1110	118	COM46	3677	-1110	168	COM2	3699	1110
19	COM120	-3137	-1110	69	C1-	385	-1110	119	COM45	3731	-1110	169	COM1	3645	1110
20	COM121	-3083	-1110	70	C1-	455	-1110	120	COM44	3785	-1110	170	COM0	3591	1110
21	COM122	-3029	-1110	71	C1+	525	-1110	121	COM43	3839	-1110	171	SEG0	3537	1110
22	COM123	-2975	-1110	72	C1+	595	-1110	122	COM42	3893	-1110	172	SEG1	3483	1110
23	COM124	-2921	-1110	73	C2+	665	-1110	123	COM41	3947	-1110	173	SEG2	3429	1110
24	COM125	-2867	-1110	74	C2+	735	-1110	124	COM40	4001	-1110	174	SEG3	3375	1110
25	COM126	-2813	-1110	75	C2-	805	-1110	125	DUMMY	4081	-1110	175	SEG4	3321	1110
26	COM127	-2759	-1110	76	C2-	875	-1110	126	DUMMY	4161	-1110	176	SEG5	3267	1110
27	TEST1	-2555	-1110	77	C4+	945	-1110	127	DUMMY	4245	-917	177	SEG6	3213	1110
28	TEST2	-2485	-1110	78	C4+	1015	-1110	128	COM39	4245	-837	178	SEG7	3159	1110
29	TEST3	-2415	-1110	79	C6+	1085	-1110	129	COM38	4245	-783	179	SEG8	3105	1110
30	CL	-2345	-1110	80	C6+	1155	-1110	130	COM37	4245	-729	180	SEG9	3051	1110
31	M	-2275	-1110	81	VSS	1225	-1110	131	COM36	4245	-675	181	SEG10	2997	1110
32	VDD	-2205	-1110	82	VSS	1295	-1110	132	COM35	4245	-621	182	SEG11	2943	1110
33	PS	-2135	-1110	83	V4	1365	-1110	133	COM34	4245	-567	183	SEG12	2889	1110
34	C68	-2065	-1110	84	V4	1435	-1110	134	COM33	4245	-513	184	SEG13	2835	1110
35	VSS	-1995	-1110	85	V3	1505	-1110	135	COM32	4245	-459	185	SEG14	2781	1110
36	CS1B	-1925	-1110	86	V3	1575	-1110	136	COM31	4245	-405	186	SEG15	2727	1110
37	CS2	-1855	-1110	87	V2	1645	-1110	137	COM30	4245	-351	187	SEG16	2673	1110
38	VDD	-1785	-1110	88	V2	1715	-1110	138	COM29	4245	-297	188	SEG17	2619	1110
39	RESETB	-1715	-1110	89	V1	1785	-1110	139	COM28	4245	-243	189	SEG18	2565	1110
40	RS	-1645	-1110	90	V1	1855	-1110	140	COM27	4245	-189	190	SEG19	2511	1110
41	VSS	-1575	-1110	91	V0	1925	-1110	141	COM26	4245	-135	191	SEG20	2457	1110
42	RW_WR	-1505	-1110	92	V0	1995	-1110	142	COM25	4245	-81	192	SEG21	2403	1110
43	E_RD	-1435	-1110	93	VR	2065	-1110	143	COM24	4245	-27	193	SEG22	2349	1110
44	VDD	-1365	-1110	94	VR	2135	-1110	144	COM23	4245	27	194	SEG23	2295	1110
45	DB0	-1295	-1110	95	VSS	2205	-1110	145	COM22	4245	81	195	SEG24	2241	1110
46	DB1	-1225	-1110	96	REF	2275	-1110	146	COM21	4245	135	196	SEG25	2187	1110
47	DB2	-1155	-1110	97	VEXT	2345	-1110	147	COM20	4245	189	197	SEG26	2133	1110
48	DB3	-1085	-1110	98	VDD	2415	-1110	148	COM19	4245	243	198	SEG27	2079	1110
49	DB4	-1015	-1110	99	INTRS	2485	-1110	149	COM18	4245	297	199	SEG28	2025	1110
50	DB5	-945	-1110	100	VSS	2555	-1110	150	COM17	4245	351	200	SEG29	1971	1110

SAMSUNG ELECTRONICS

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

NO	NAME	X	Y
201	SEG30	1917	1110
202	SEG31	1863	1110
203	SEG32	1809	1110
204	SEG33	1755	1110
205	SEG34	1701	1110
206	SEG35	1647	1110
207	SEG36	1593	1110
208	SEG37	1539	1110
209	SEG38	1485	1110
210	SEG39	1431	1110
211	SEG40	1377	1110
212	SEG41	1323	1110
213	SEG42	1269	1110
214	SEG43	1215	1110
215	SEG44	1161	1110
216	SEG45	1107	1110
217	SEG46	1053	1110
218	SEG47	999	1110
219	SEG48	945	1110
220	SEG49	891	1110
221	SEG50	837	1110
222	SEG51	783	1110
223	SEG52	729	1110
224	SEG53	675	1110
225	SEG54	621	1110
226	SEG55	567	1110
227	SEG56	513	1110
228	SEG57	459	1110
229	SEG58	405	1110
230	SEG59	351	1110
231	SEG60	297	1110
232	SEG61	243	1110
233	SEG62	189	1110
234	SEG63	135	1110
235	SEG64	81	1110
236	SEG65	27	1110
237	SEG66	-27	1110
238	SEG67	-81	1110
239	SEG68	-135	1110
240	SEG69	-189	1110
241	SEG70	-243	1110
242	SEG71	-297	1110
243	SEG72	-351	1110
244	SEG73	-405	1110
245	SEG74	-459	1110
246	SEG75	-513	1110
247	SEG76	-567	1110
248	SEG77	-621	1110
249	SEG78	-675	1110
250	SEG79	-729	1110
251	SEG80	-783	1110
252	SEG81	-837	1110
253	SEG82	-891	1110
254	SEG83	-945	1110
255	SEG84	-999	1110
256	SEG85	-1053	1110
257	SEG86	-1107	1110
258	SEG87	-1161	1110
259	SEG88	-1215	1110
260	SEG89	-1269	1110
261	SEG90	-1323	1110
262	SEG91	-1377	1110
263	SEG92	-1431	1110
264	SEG93	-1485	1110
265	SEG94	-1539	1110
266	SEG95	-1593	1110
267	SEG96	-1647	1110
268	SEG97	-1701	1110
269	SEG98	-1755	1110
270	SEG99	-1809	1110
271	SEG100	-1863	1110
272	SEG101	-1917	1110
273	SEG102	-1971	1110
274	SEG103	-2025	1110
275	SEG104	-2079	1110
276	SEG105	-2133	1110
277	SEG106	-2187	1110
278	SEG107	-2241	1110
279	SEG108	-2295	1110
280	SEG109	-2349	1110
281	SEG110	-2403	1110
282	SEG111	-2457	1110
283	SEG112	-2511	1110
284	SEG113	-2565	1110
285	SEG114	-2619	1110
286	SEG115	-2673	1110
287	SEG116	-2727	1110
288	SEG117	-2781	1110
289	SEG118	-2835	1110
290	SEG119	-2889	1110
291	SEG120	-2943	1110
292	SEG121	-2997	1110
293	SEG122	-3051	1110
294	SEG123	-3105	1110
295	SEG124	-3159	1110
296	SEG125	-3213	1110
297	SEG126	-3267	1110
298	SEG127	-3321	1110
299	SEG128	-3375	1110
300	SEG129	-3429	1110
301	SEG130	-3483	1110
302	SEG131	-3537	1110
303	COM64	-3591	1110
304	COM65	-3645	1110
305	COM66	-3699	1110
306	COM67	-3753	1110
307	COM68	-3807	1110
308	COM69	-3861	1110
309	COM70	-3915	1110
310	COM71	-3969	1110
311	DUMMY	-4049	1110
312	DUMMY	-4129	1110
313	DUMMY	-4245	917
314	COM72	-4245	837
315	COM73	-4245	783
316	COM74	-4245	729
317	COM75	-4245	675
318	COM76	-4245	621
319	COM77	-4245	567
320	COM78	-4245	513
321	COM79	-4245	459
322	COM80	-4245	405
323	COM81	-4245	351
324	COM82	-4245	297
325	COM83	-4245	243
326	COM84	-4245	189
327	COM85	-4245	135
328	COM86	-4245	81
329	COM87	-4245	27
330	COM88	-4245	-27
331	COM89	-4245	-81
332	COM90	-4245	-135
333	COM91	-4245	-189
334	COM92	-4245	-243
335	COM93	-4245	-297
336	COM94	-4245	-351
337	COM95	-4245	-405
338	COM96	-4245	-459
339	COM97	-4245	-513
340	COM98	-4245	-567
341	COM99	-4245	-621
342	COM100	-4245	-675
343	COM101	-4245	-729
344	COM102	-4245	-783
345	COM103	-4245	-837
346	DUMMY	-4245	-917

PIN DESCRIPTION

Table 3. Power Supply Pins

<table>
<tr><th>Name</th><th>I/O</th><th colspan="5">Description</th></tr>
<tr><td>VDD</td><td>Supply</td><td colspan="5">Power supply</td></tr>
<tr><td>Vss</td><td>Supply</td><td colspan="5">Ground</td></tr>
<tr><td rowspan="4">V0
V1
V2
V3
V4</td><td rowspan="4">I/O</td><td colspan="5">LCD drivers supply voltages
The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application.
Voltages should have the following relationship: V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ Vss
When the internal power circuit is active, these voltages are generated as following table according to the state of LCD bias.</td></tr>
<tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/N bias</td><td>(N-1)/N x V0</td><td>(N-2)/N x V0</td><td>2/N x V0</td><td>1/N x V0</td></tr>
<tr><td colspan="5">NOTE : *N = 5 to 12</td></tr>
</table>

Table 4. LCD Driver Supply Pins

Name	I/O	Description
C1-, C2-	I/O	Capacitor negative connection pins used for voltage converter
C1+, C2+ C3+, C4+ C5+, C6+	I/O	Capacitor positive connection pins used for voltage converter
VOUT	I/O	Voltage converter input/output pin. VOUT = Boost level × VCI, for internal booster
VCI	I	Voltage converter input voltage pin for internal booster.
VR	I	V0 voltage adjustment pin used to adjust V0 by means of external resistors(INTRS = “L”)
REF	I	Selects the external VREF voltage via VEXT pin – REF = "L": using the external VREF – REF = "H": using the internal VREF
VEXT	I	Externally-input reference voltage(VREF) for the internal voltage regulator. It is valid only when REF is “L”.
INTRS	I	Internal resistors select pin used to select resistors for adjusting V0 voltage level. – INTRS = "H”: use the internal resistors. – INTRS = "L”: use the external resistors. VR pin and external resistive divider control V0 voltage.

Table 5. Microprocessor Interface Pins

<table>
<tr><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESETB</td><td>I</td><td>Reset input pin.
When RESETB is “L”, initialization is executed.</td></tr>
<tr><td rowspan="4">PS</td><td rowspan="4">I</td><td>Parallel / Serial data input select input
<table>
<tr><td>PS</td><td>Interface mode</td><td>Data / instruction</td><td>Data</td><td>Read / Write</td><td>Serial clock</td></tr>
<tr><td>H</td><td>Parallel</td><td>RS</td><td>DB0 to DB7</td><td>E_RD
RW_WR</td><td>-</td></tr>
<tr><td>L</td><td>Serial</td><td>RS</td><td>SID (DB7)</td><td>Write only</td><td>SCLK (DB6)</td></tr>
</table></td></tr>
<tr><td>*NOTE: When PS is “L”, DB0 to DB5 are high impedance and E_RD and RW_WR must be fixed to either “H” or “L”.</td></tr>
<tr><td rowspan="3">C68</td><td rowspan="3">I</td><td>Microprocessor interface(PS = “H”) / Register Select(PS = “L”)input pin
<table>
<tr><td colspan="2">PS</td><td>C68</td><td>Interface mode</td></tr>
<tr><td colspan="2" rowspan="2">H</td><td>H</td><td>6800-series MPU mode</td></tr>
<tr><td>L</td><td>8080-series MPU mode</td></tr>
<tr><td colspan="2" rowspan="2">L</td><td>H</td><td>4-Pin SPI MPU mode</td></tr>
<tr><td>L</td><td>3-Pin SPI MPU mode</td></tr>
</table></td></tr>
<tr><td></td></tr>
<tr><td>CS1B
CS2</td><td>I</td><td>Chip select input pins
Data / instruction I/O is enabled only when CS1B is “L” and CS2 is “H”. When chip select is non-active, DB0 to DB7 may be high impedance.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select input pin
– RS = "H": DB0 to DB7 are display data
– RS = "L": DB0 to DB7 are control data</td></tr>
<tr><td rowspan="3">RW_WR</td><td rowspan="3">I</td><td>Read / Write execution control pin
<table>
<tr><td>C68</td><td>MPU Type</td><td>RW_WR</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>RW</td><td>Read/Write control input pin
– RW = “H”: read
– RW = “L”: write</td></tr>
<tr><td>L</td><td>8080-series</td><td>/WR</td><td>Write enable clock input pin
The data on DB0 to DB7 are latched at the rising edge of the /WR signal.</td></tr>
</table></td></tr>
<tr><td></td></tr>
</table>

Table 5. Microprocessor Interface Pins (Continued)

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="4">E_RD</td><td rowspan="4">I</td><td colspan="4">Read / Write execution control pin</td></tr>
<tr><td>C68</td><td>MPU type</td><td>E_RD</td><td>Description</td></tr>
<tr><td>H</td><td>6800-series</td><td>E</td><td>Read / Write control input pin
– RW = “H”: When E is “H”, DB0 to DB7 are in an output status.
– RW = “L”: The data on DB0 to DB7 are latched at the falling edge of the E signal.</td></tr>
<tr><td>L</td><td>8080-series</td><td>/RD</td><td>Read enable clock input pin
When /RD is “L”, DB0 to DB7 are in an output status.</td></tr>
<tr><td>DB0
to
DB7</td><td>I/O</td><td colspan="4">8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus.
When the serial interface selected (PS = "L");
– DB0 to DB5: high impedance
– DB6: serial input clock (SCLK)
– DB7: serial input data (SID).
When chip select is not active, DB0 to DB7 may be high impedance.</td></tr>
</table>

Table 6. Test Pins

Name	I/O	Description
TEST1 to TEST3	I	Test pins Don’t use these pins.

Table 7. LCD driver output pins

<table>
<tr><th>Name</th><th>I/O</th><th colspan="4">Description</th></tr>
<tr><td rowspan="9">SEG0
to
SEG131</td><td rowspan="9">O</td><td colspan="4">LCD segment driver outputs
The display data and the M signal control the output voltage of segment driver.</td></tr>
<tr><td rowspan="2">Display data</td><td rowspan="2">M</td><td colspan="2">Segment driver output voltage</td></tr>
<tr><td>Normal display</td><td>Reverse display</td></tr>
<tr><td>H</td><td>H</td><td>V0</td><td>V2</td></tr>
<tr><td>H</td><td>L</td><td>Vss</td><td>V3</td></tr>
<tr><td>L</td><td>H</td><td>V2</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V3</td><td>Vss</td></tr>
<tr><td colspan="2">Power save mode</td><td>Vss</td><td>Vss</td></tr>
<tr><td colspan="4"></td></tr>
<tr><td rowspan="8">COM0
to
COM127</td><td rowspan="8">O</td><td colspan="4">LCD common driver outputs
The internal scanning data and M signal control the output voltage of common driver.</td></tr>
<tr><td>Scan data</td><td>M</td><td colspan="2">Common driver output voltage</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">Vss</td></tr>
<tr><td>H</td><td>L</td><td colspan="2">V0</td></tr>
<tr><td>L</td><td>H</td><td colspan="2">V1</td></tr>
<tr><td>L</td><td>L</td><td colspan="2">V4</td></tr>
<tr><td colspan="2">Power save mode</td><td colspan="2">Vss</td></tr>
<tr><td colspan="4"></td></tr>
</table>

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There are CS1B and CS2 pins for chip selection. The S6B0728 can interface with an MPU only when CS1B is "L" and CS2 is "H". When these pins are set to any other combination, RS, E_RD, and RW_WR inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

The S6B0728 has four types of interface with an MPU, which are two serial and two parallel interfaces. This parallel or serial interface is determined by PS pin as shown in **Table 8**.

Table 8. Parallel / Serial Interface Mode.

PS	Type	CS1B	CS2	C68	Interface mode
H	Parallel	CS1B	CS2	H	6800-series MPU mode
				L	8080-series MPU mode
L	Serial	CS1B	CS2	H	4-Pin SPI MPU mode
				L	3-Pin SPI MPU mode

Parallel Interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by C68 as shown in **Table 9**. The type of data transfer is determined by signals at RS, E_RD and RW_WR as shown in **Table 10**.

Table 9. Microprocessor Selection for Parallel Interface

C68	CS1B	CS2	RS	E_RD	RW_WR	DB0 to DB7	MPU bus
H	CS1B	CS2	RS	E	RW	DB0 to DB7	6800-series
L	CS1B	CS2	RS	/RD	/WR	DB0 to DB7	8080-series

Table 10. Parallel Data Transfer

Common	6800-series		8080-series		Description
RS	E_RD (E)	RW_WR (RW)	E_RD (/RD)	RW_WR (/WR)	
H	H	H	L	H	Read display data
H	H	L	H	L	Write display data
L	H	H	L	H	Read out internal status register
L	H	L	H	L	Write instruction data

Serial Interface (PS = "L")

Communication with the microprocessor occurs via a clock-synchronized serial peripheral interface when PS is low. When using the serial interface, read operations are not allowed. **.** When the chip select inputs are valid(CS1B = "L" & CS2 = "H"), the serial data is sent most significant bit first on the rising edge of a serial clock going into DB6 and processed as 8-bit parallel data on the eighth clock. Since the clock signal is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended. And not valid, the internal 8-bit shift register and the 3-bit counter are reset.
The serial interface type is selected by setting C68 as shown in **Table 11**.

Table 11. Microprocessor Selection for Serial Interface

C68	Serial interface mode	Chip Select	Register Select	Serial Data / Clock input
H	4-Pin SPI	CS1B, CS2	by RS pin	DB7 / DB6
L	3-Pin SPI	CS1B, CS2	by software	DB7 / DB6

4-Pin SPI Interface (PS = "L", C68 = "H")

In 4-pin SPI interface mode, RS pin is used for indicating whether serial data input is display or instruction data. Data is display data when RS is high and instruction data when RS is low.

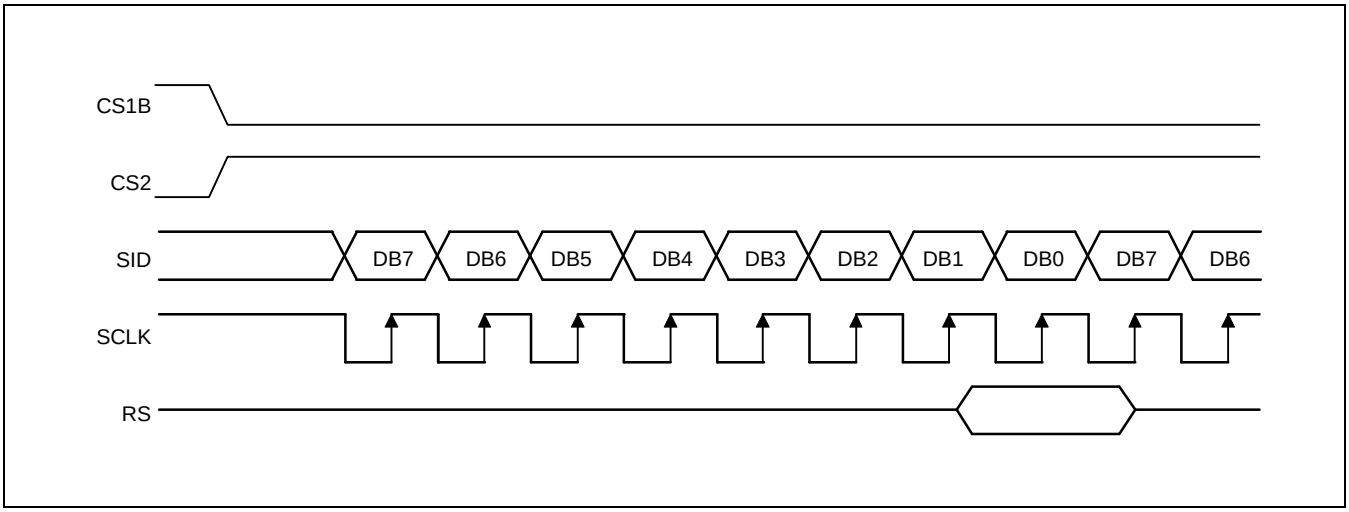


Figure 3. 4-Pin SPI Timing (RS is used)

3-Pin SPI Interface (PS = "L" , C68 = "L")

In 3-Pin SPI Interface mode, the pre-defined instruction called Display Data Length, is used to indicate whether serial data input is display or instruction data instead of RS pin. The data is handled as instruction data until the Display Data Length instruction is issued. This Display Data Length instruction consists two bytes instruction. The first byte instruction enables the next instruction to be valid, and the data of the second byte indicates that a specified number of display data bytes(1 to 256) are to be transmitted. The next byte after the display data string is handled as instruction data. For details, refers the Figure 4.

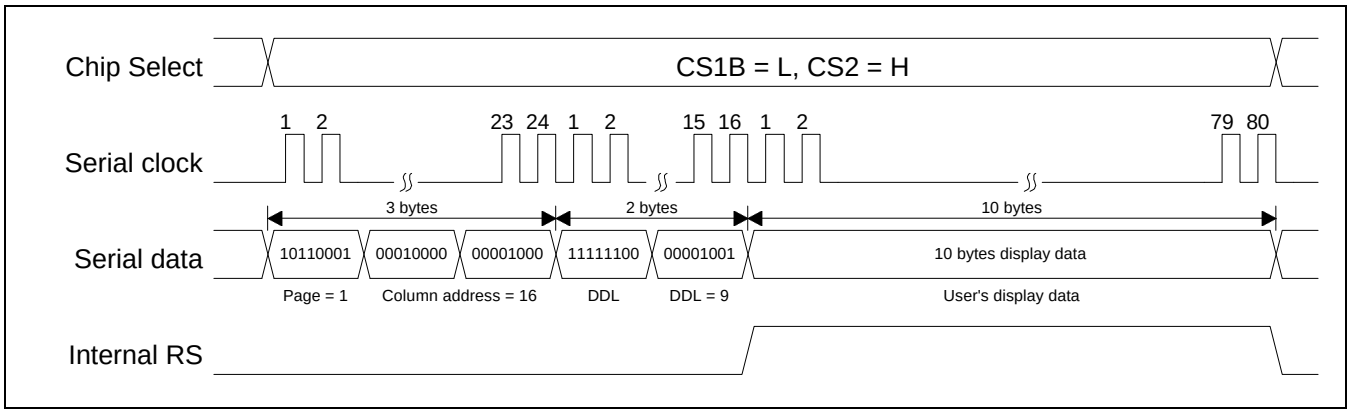


Figure 4. 3 Pin SPI Timing (RS is not used)

*NOTES:

- In spite of transmission of data, if CS1B will be disable, state terminates abnormally. Next state is initialized.
- The number of writing display data = DDL register value + 1

Busy Flag

The Busy Flag indicates whether the S6B0728 is operating or not. When DB7 is “H” in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The S6B0728 uses bus holder and internal data bus for data transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 4. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 5. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

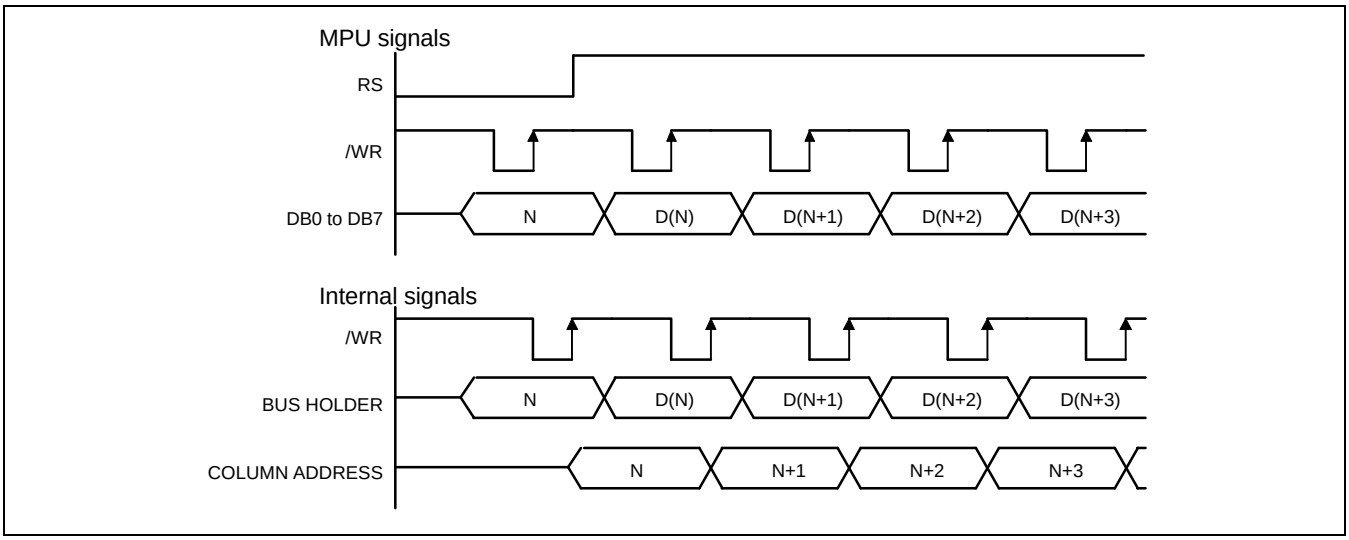


Figure 5. Write Timing

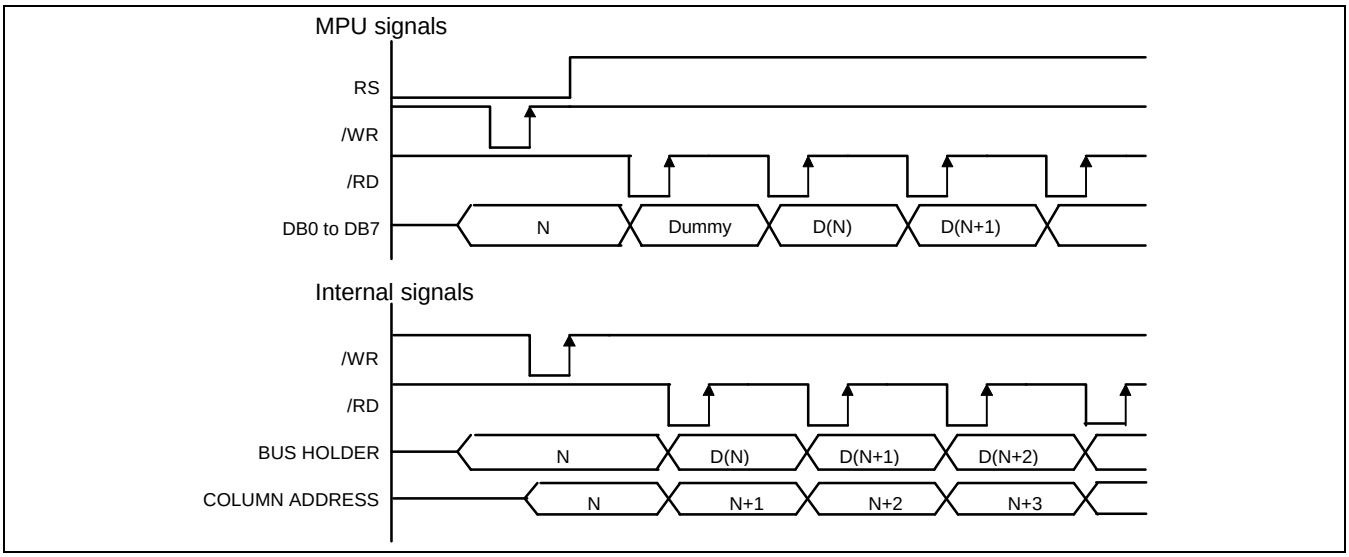


Figure 6. Read Timing

DISPLAY DATA RAM (DDRAM)

The Display Data RAM stores pixel data for the LCD. It is 128-row by 132-column addressable array. Each pixel can be selected when the page and column addresses are specified. The 128 rows are divided into 16 pages of 8 lines. Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The display data of DB0 to DB7 from the microprocessor correspond to the LCD common lines as shown in figure 6. The microprocessor can read from and write to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written into RAM at the same time as data is being displayed without causing the LCD flicker.

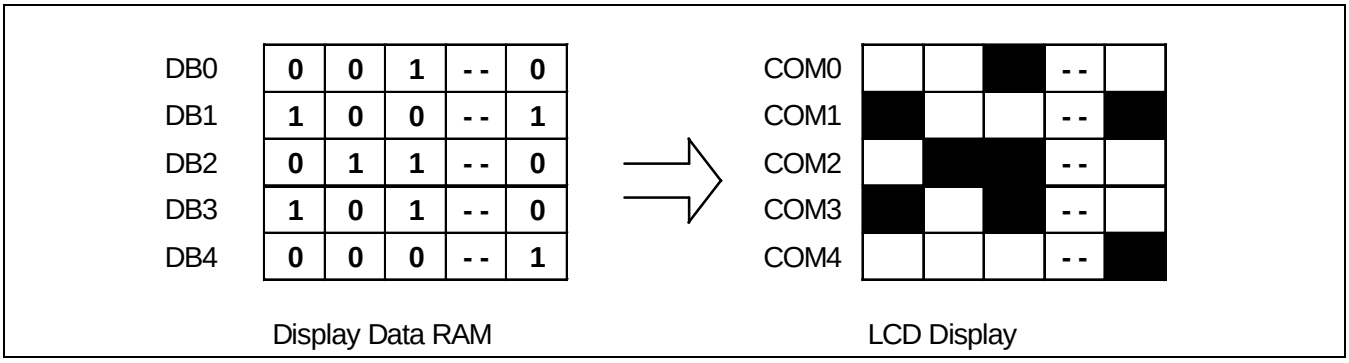


Figure 7. RAM-to-LCD Data Transfer

Page Address Circuit

This circuit is for providing a page address to Display Data RAM shown in figure 8. It incorporates 4-bit page address register changed by only the “Set Page” instruction.

Line Address Circuit

This circuit assigns DDRAM a line address corresponding to the first line (COM0) of the display. Therefore, by setting line address repeatedly, it is possible to realize the screen scrolling and page switching without changing the contents of on-chip RAM as shown in figure 7. It incorporates 7-bit line address register changed by only the initial display line instruction and 7-bit counter circuit. At the beginning of each LCD frame, the contents of register are copied to the line counter which is increased by internal latch signal and generates the Line Address for transferring the 132-bit RAM data to the display data latch circuit. However, display data of icons are not scrolled because the MPU can not access Line Address of icons.

Column Address Circuit

Column Address circuit has an 8-bit preset counter that provides Column Address to the Display Data RAM as shown in figure 8. When set Column Address MSB / LSB instruction is issued, 8-bit [Y7:Y0] is updated. And, since this address is increased by 1 each a read or write data instruction, microprocessor can access the display data continuously. However, the counter is not incremented and locked if a non-existing address above 83H. It is unlocked if a column address is set again by set Column Address MSB / LSB instruction. And the Column Address counter is independent of page address register.

ADC select instruction makes it possible to invert the relationship between the Column Address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC select instruction. Refer to the following figure 7.

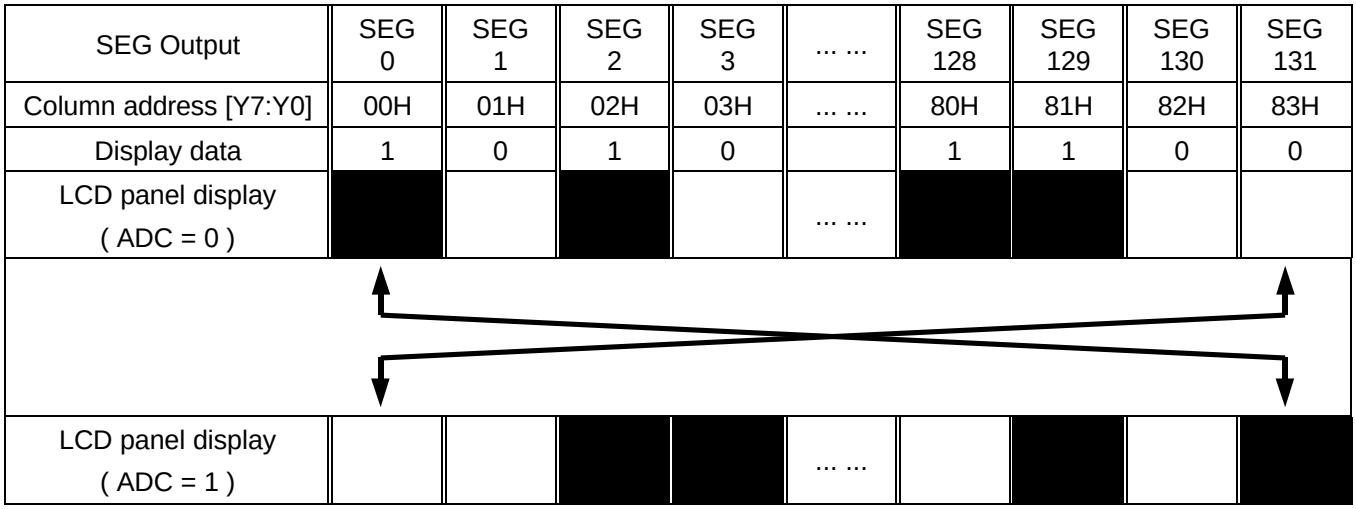


Figure 8. The Relationship between the Column Address and The Segment Outputs

Segment Control Circuit

This circuit controls the display data by the display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

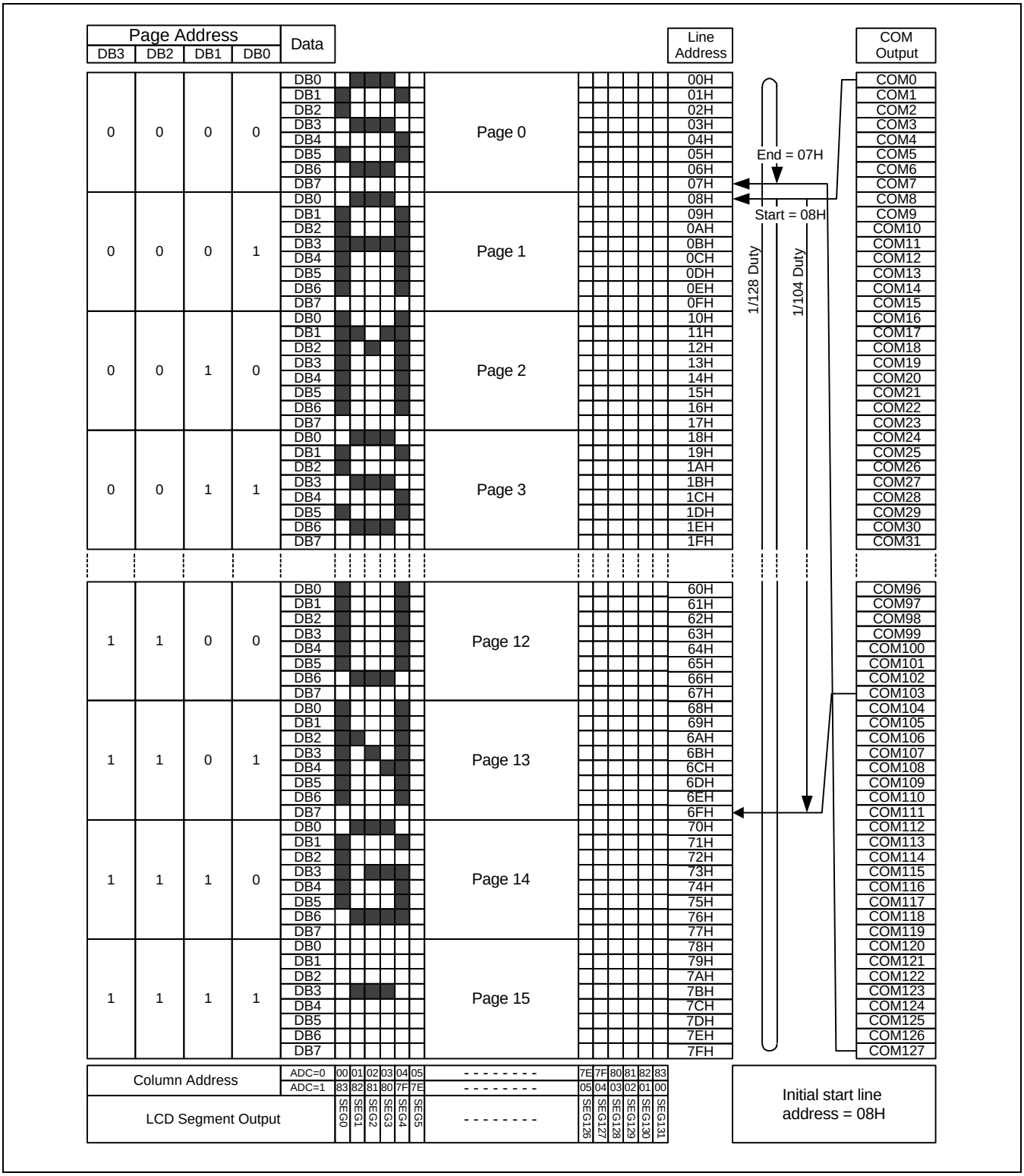


Figure 9. Display Data RAM Map

SAMSUNG ELECTRONICS

LCD DISPLAY CIRCUITS

Oscillator

This is completely on-chip Oscillator and its frequency is nearly independent of V_{DD}. This oscillator signal is used in the voltage converter and display timing generation circuit.

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The internal display clock, CL, generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock (CL) and the display data latch circuit in synchronization latches the 132-bit display data with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. The frame or the line changes the phase of M by setting internal instruction. Driving waveform and internal timing signal are shown in figure 10.

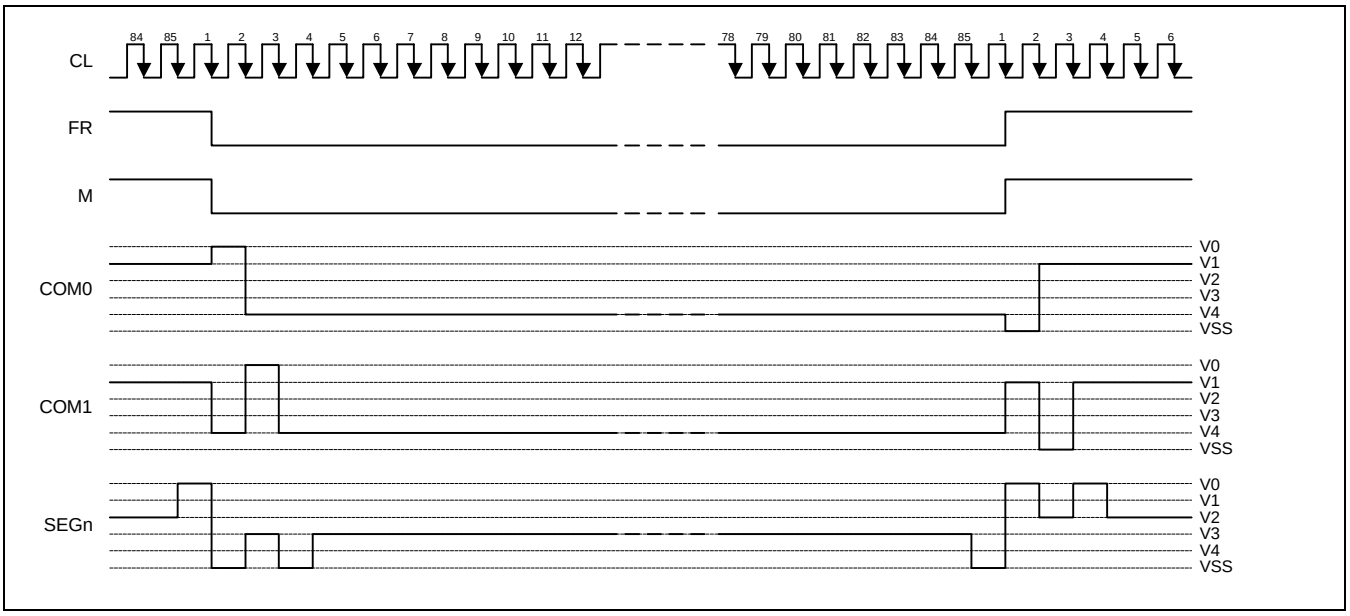


Figure 10. 2-frame AC Driving Waveform (Duty Ratio = 1/85)

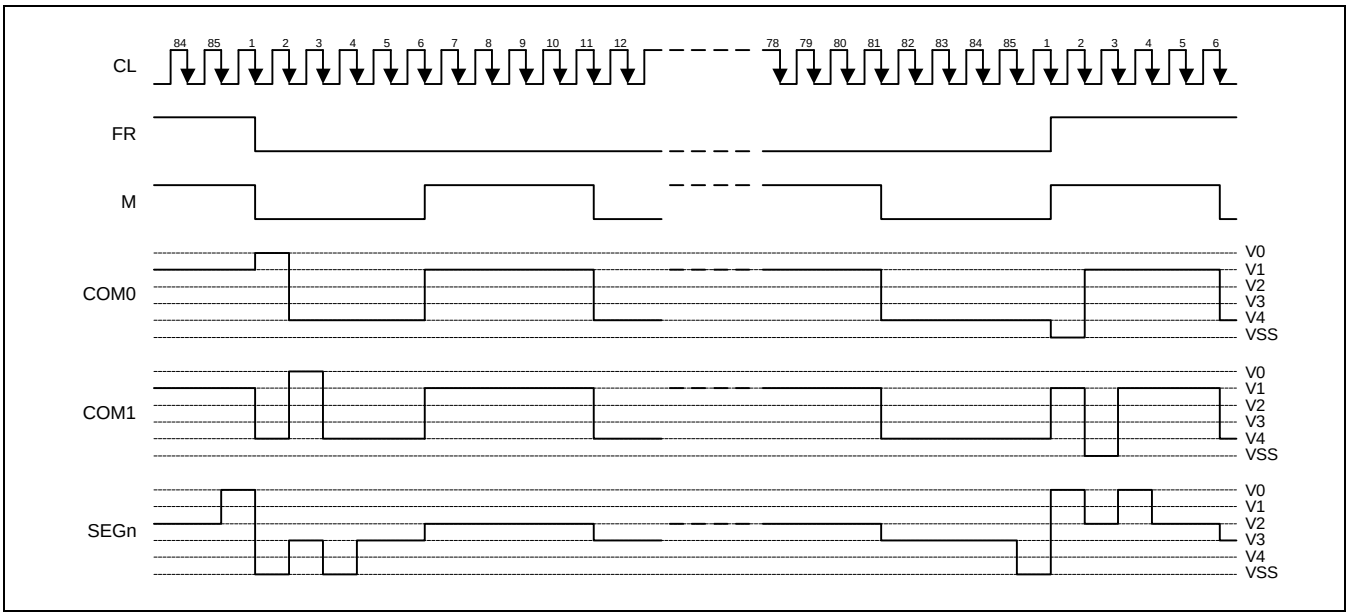


Figure 11. N-line Inversion Driving Waveform (N = 5, Duty Ratio = 1/85)

SAMSUNG ELECTRONICS

LCD DRIVER CIRCUIT

128-channel common driver and 132-channel segment driver configure this driver circuit. This LCD panel driver voltage depends on the combination of display data and M signal.

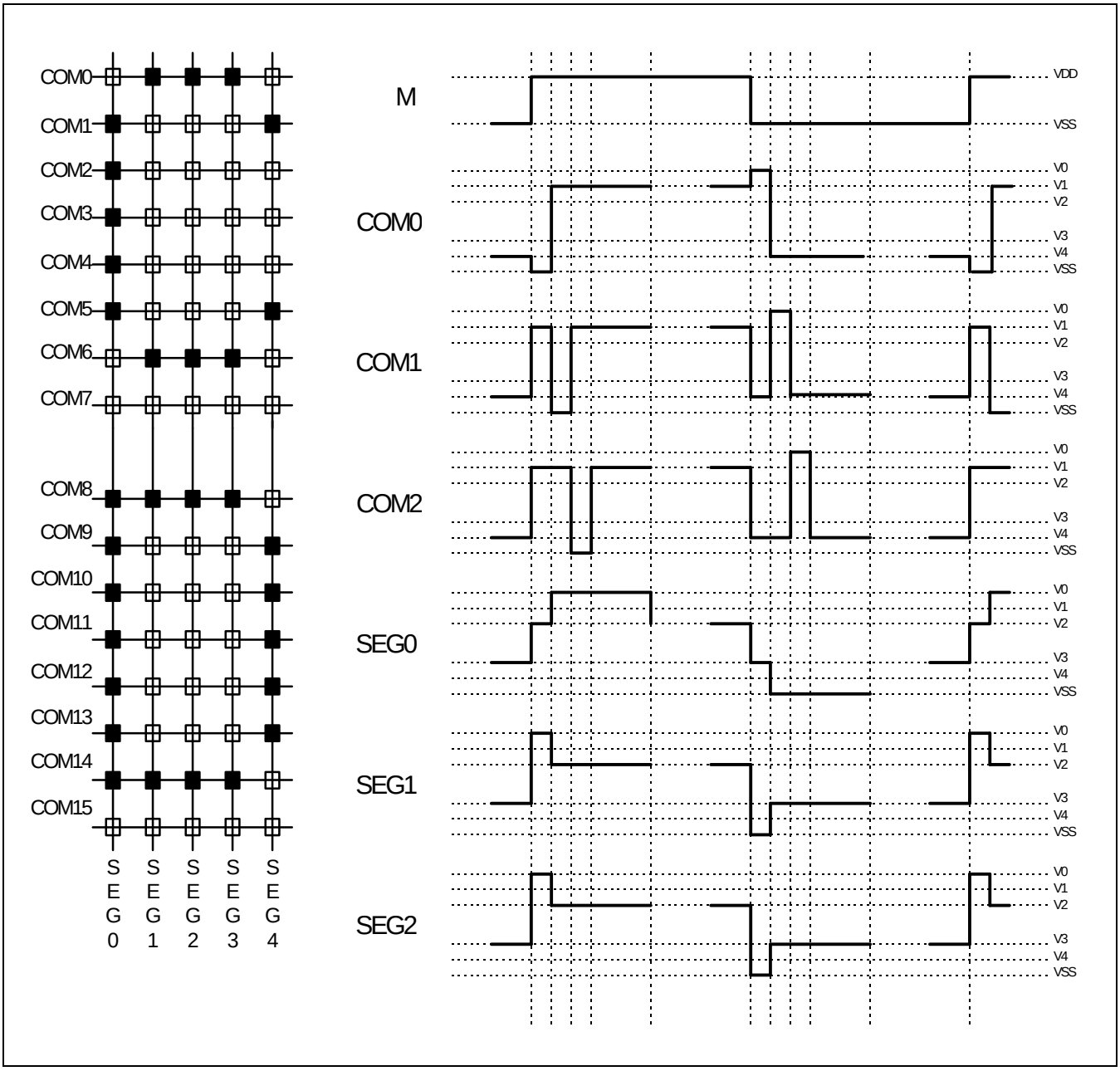


Figure 12. Segment and Common Timing

Partial Display on LCD

The S6B0728 realizes the partial display function on LCD with low-duty driving for saving power consumption and showing the various display duties. To show the various display duties on LCD, LCD driving duty and bias are programmable via the instruction. And, built-in power supply circuits are controlled by the instruction for adjusting the LCD driving voltages

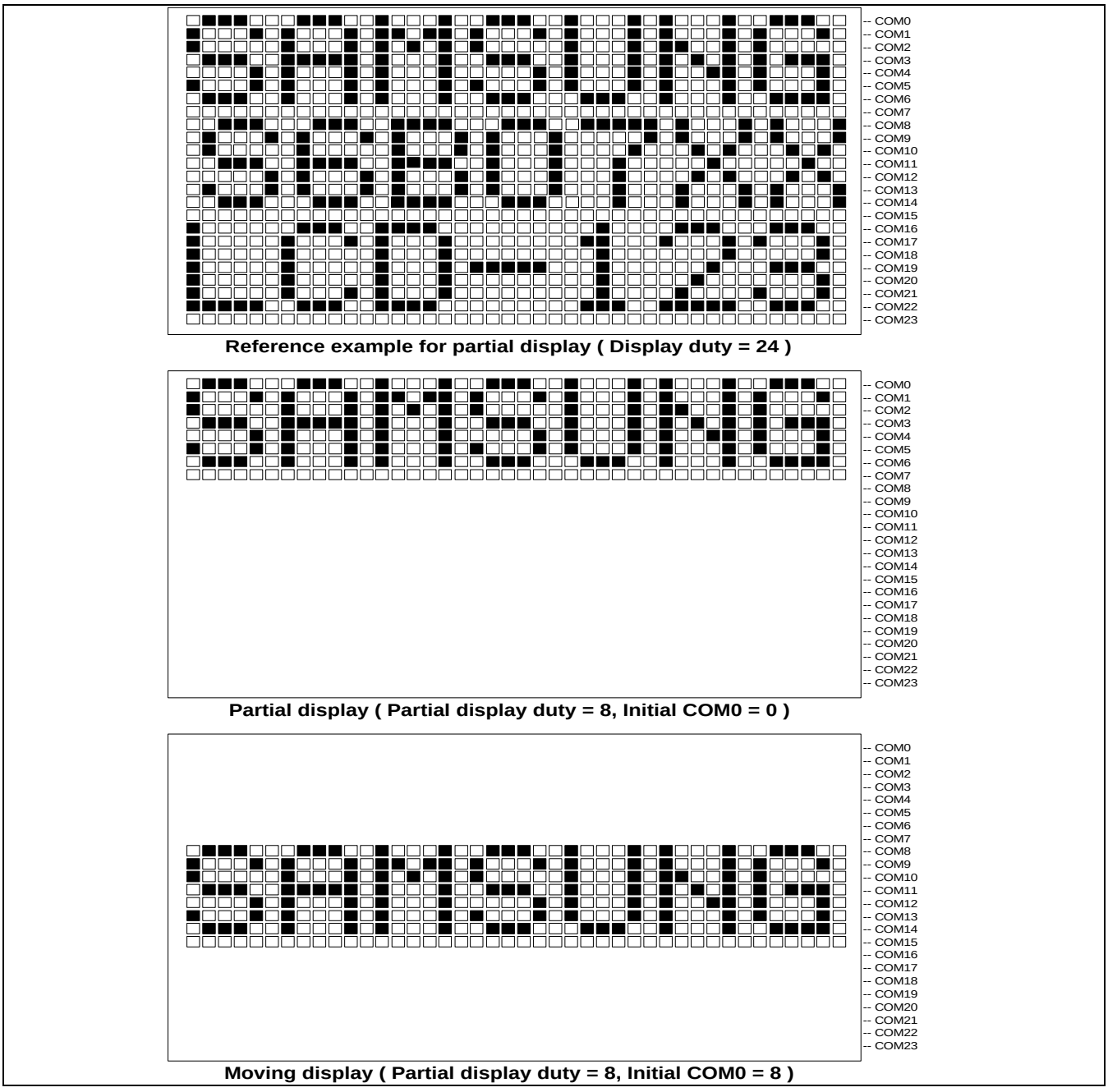


Figure 13. Reference Example for Partial Display

POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low-power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by power control instruction. For details, refers to "Instruction Description". Table 12 shows the referenced combinations in using Power Supply circuits.

Table 12. Recommended Power Supply Combinations

User setup	Power control (VC VR VF)	V/C circuits	V/R circuits	V/F circuits	VOUT	V0	V1 to V4
Only the internal power supply circuits are used	1 1 1	ON	ON	ON	Open	Open	Open
Only the voltage regulator circuits and voltage follower circuits are used	0 1 1	OFF	ON	ON	External input	Open	Open
Only the voltage follower circuits are used	0 0 1	OFF	OFF	ON	External input	Open	Open
Only the external power supply circuits are used	0 0 0	OFF	OFF	OFF	Open	External input	External input

Voltage Converter Circuits

These circuits boost up the electric potential between VCI and Vss to 3, 4, 5, 6 or 7 times toward positive side and boosted voltage is outputted from VOUT pin. It is possible to select the lower boosting level in any boosting circuit by "Set DC-DC Step-up" instruction. When the higher level is selected by instruction, VOUT voltage is not valid.

[C1 = 1.0 to 4.7 ㎌]

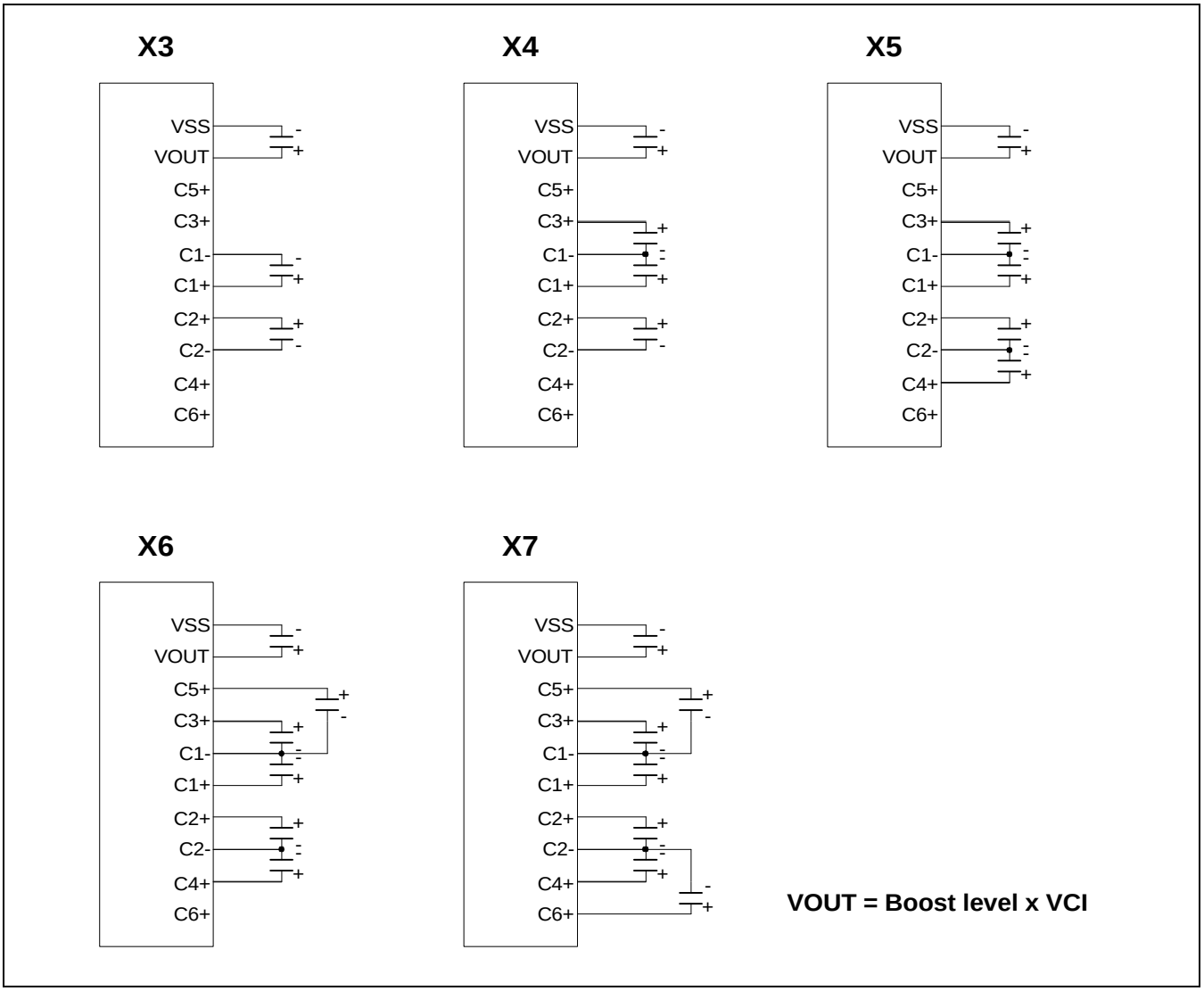


Figure 14. Boosting Circuits

Voltage Regulator Circuits

The function of the internal voltage regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in figure 19, it is necessary to be applied internally or externally.

For the Eq. 6-1, we determine V0 by Ra, Rb and V_{EV}. The Ra and Rb are connected internally or externally by INTRS pin. And V_{EV} called the voltage of electronic volume is determined by Eq. 6-2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 63. V_{REF} voltage at Ta = 25°C is shown in Table 13.

$$V0 = (1 + (Rb / Ra)) \times V_{EV} \quad [V] \text{ ------ (Eq. 6-1)}$$

$$V_{EV} = (1 - ((63 - \alpha) / 200)) \times V_{REF} \quad [V] \text{ ------ (Eq. 6-2)}$$

Table 13. V_{REF} Voltage at Ta = 25°C

REF	Temp. coefficient	V_{REF} [V]
1	-0.05% / °C	2.0
0	External input	VEXT

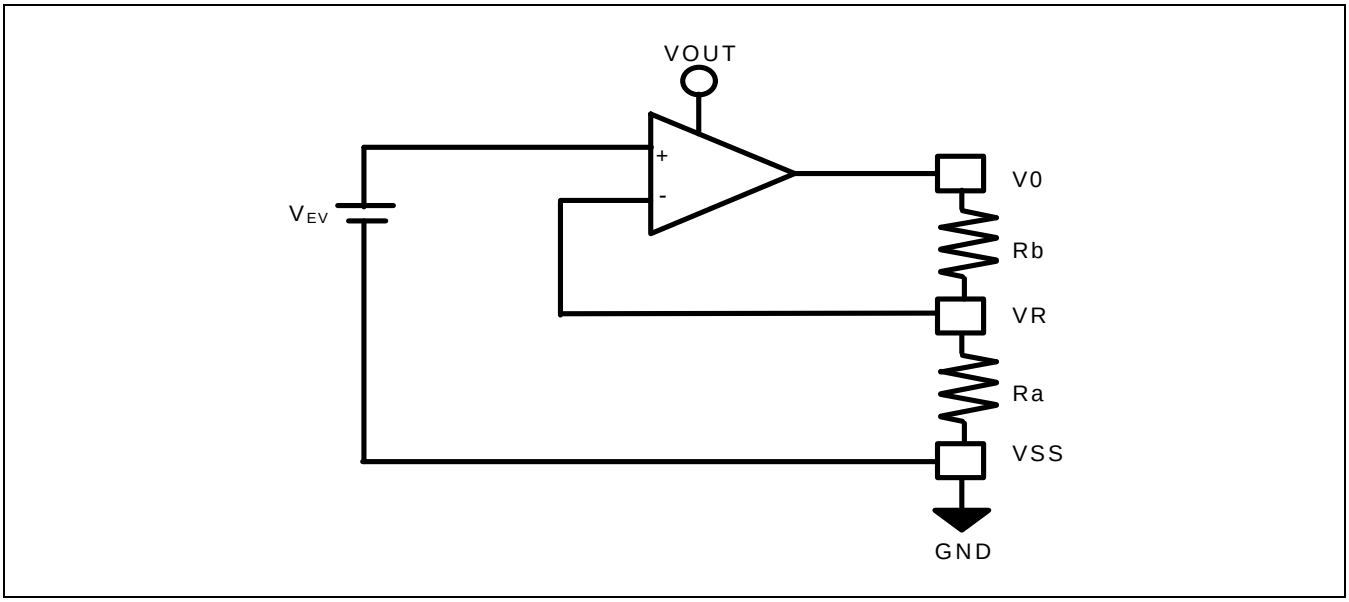


Figure 15. Internal Voltage Regulator Circuit

In Case of Using Internal Resistors, Ra and Rb (INTRS = "H")

When INTRS pin is "H", resistor Ra is connected internally between VR pin and Vss, and Rb is connected between V0 and VR. We determine V0 by two instructions, "Regulator Resistor Select" and "Set Reference Voltage".

	3-bit data settings (R2 R1 R0)							
	0 0 0	**0 0 1**	**0 1 0**	**0 1 1**	**1 0 0**	**1 0 1**	**1 1 0**	**1 1 1**
1 + (Rb / Ra)	2.6	3.4	4.2	5.0	5.8	6.6	7.4	8.3

Table 14. Internal Rb / Ra ratio Depending on 3-bit Data (R2 R1 R0)

Figure 16 shows V0 voltage measured by adjusting internal regulator register ratio (Rb / Ra) and 6-bit electronic volume registers for each temperature coefficient at Ta = 25 °C.

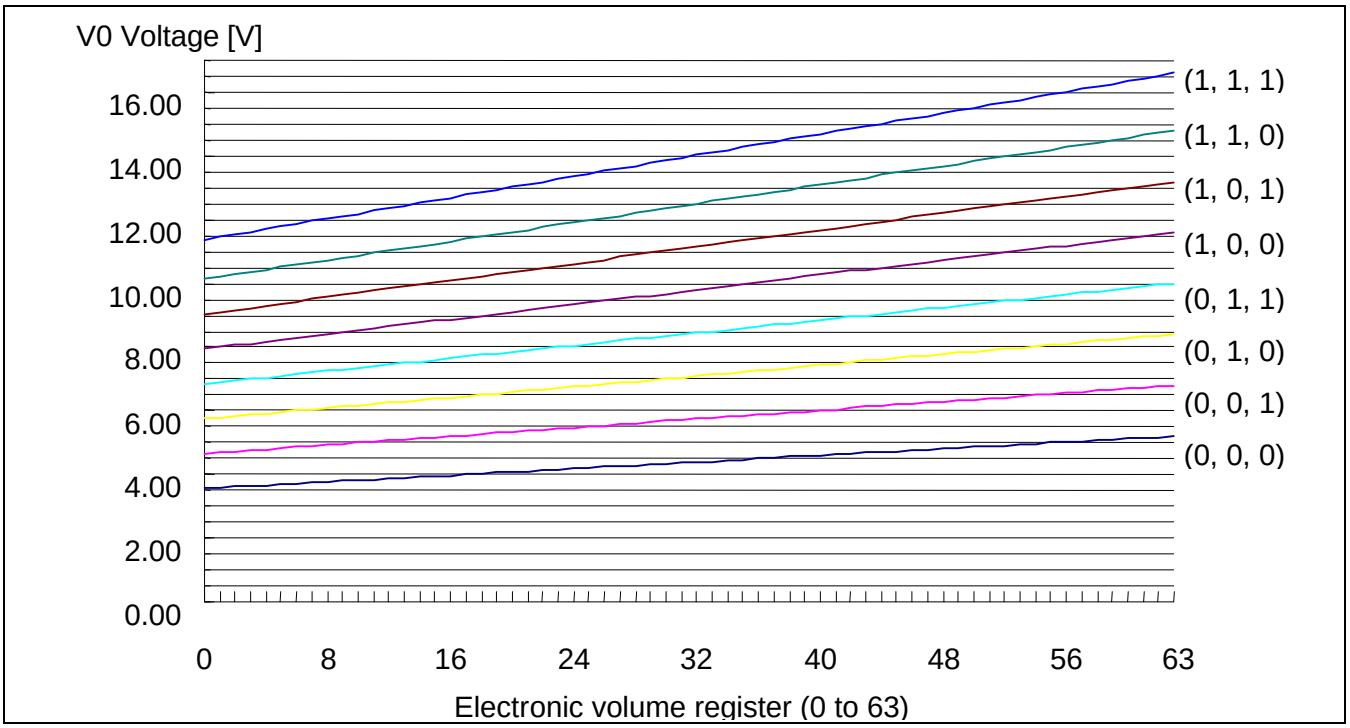


Figure 16. V0 Voltage by 1 + (Rb / Ra) and Electronic Volume Levels

In Case of Using External Resistors, Ra and Rb (INTRS = "L")

When INTRS pin is “L”, it is necessary to connect external regulator resistor Ra between VR and VSS, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 10V
2. 6-bit reference voltage register = (1, 0, 0, 0, 0, 0)
3. Maximum current flowing Ra, Rb = 1 *u*A

From Eq. 6.1

$10 = (1 + (Rb / Ra)) \times V_{EV}$ [V] ------ (Eq. 6.3)

From Eq. 6.2

$V_{EV} = (1 – ((63 - 32) / 200)) \times 2.0 = 1.69$ [V] ------ (Eq. 6.4)

From requirement 3.

$10 / (Ra + Rb) = 1$ [uA] ------ (Eq. 6.5)

From equations Eq. 6.3, 6.4 and 6.5

Ra = 1.69 [MΩ], Rb = 8.31 [MΩ]

Table 15 shows the range of V0 depending on the above requirements.

Table 15. The Range of V0

	Electronic volume level				
	0	**.....**	**32**	**.....**	**63**
V0	8.10	.....	10.00	.....	11.83

Voltage Follower Circuits

VLCD voltage (V0) is resistively divided into four voltage levels (V1, V2, V3 and V4), and these output impedance are converted by the Voltage Follower for increasing drive capability. Table 16 shows the relationship between V1 to V4 level and each duty ratio.

Table 16. V1 to V4 Level

LCD bias	V1	V2	V3	V4	Remarks
1/N	(N-1)/N x V0	(N-1)/N x V0	2/N x V0	1/N x V0	N = 5 to 12

REFERENCE CIRCUIT EXAMPLES

[C1 = 1.0 to 4.7 [㎌], C2 = 0.1 to 0.47 [㎌]]

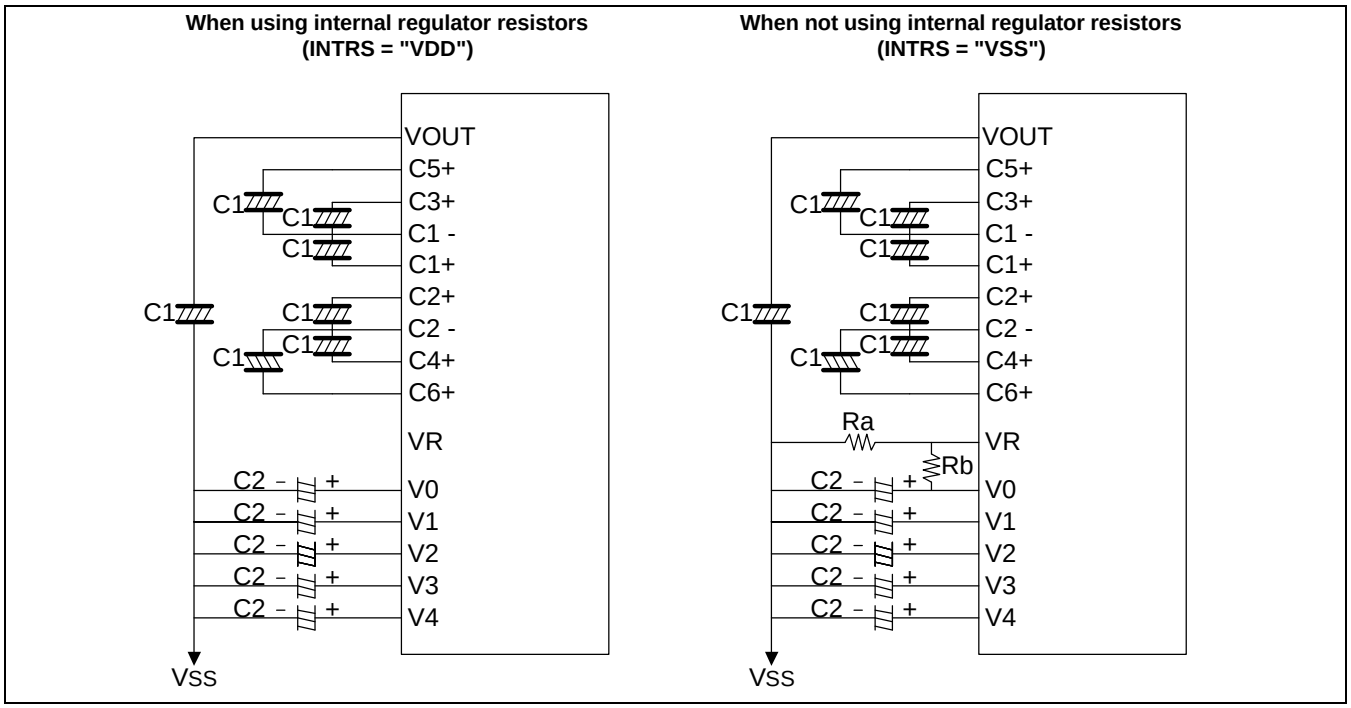


Figure 17. When Using all LCD Power Circuits (7-times V/C: ON, V/R: ON, V/F: ON)

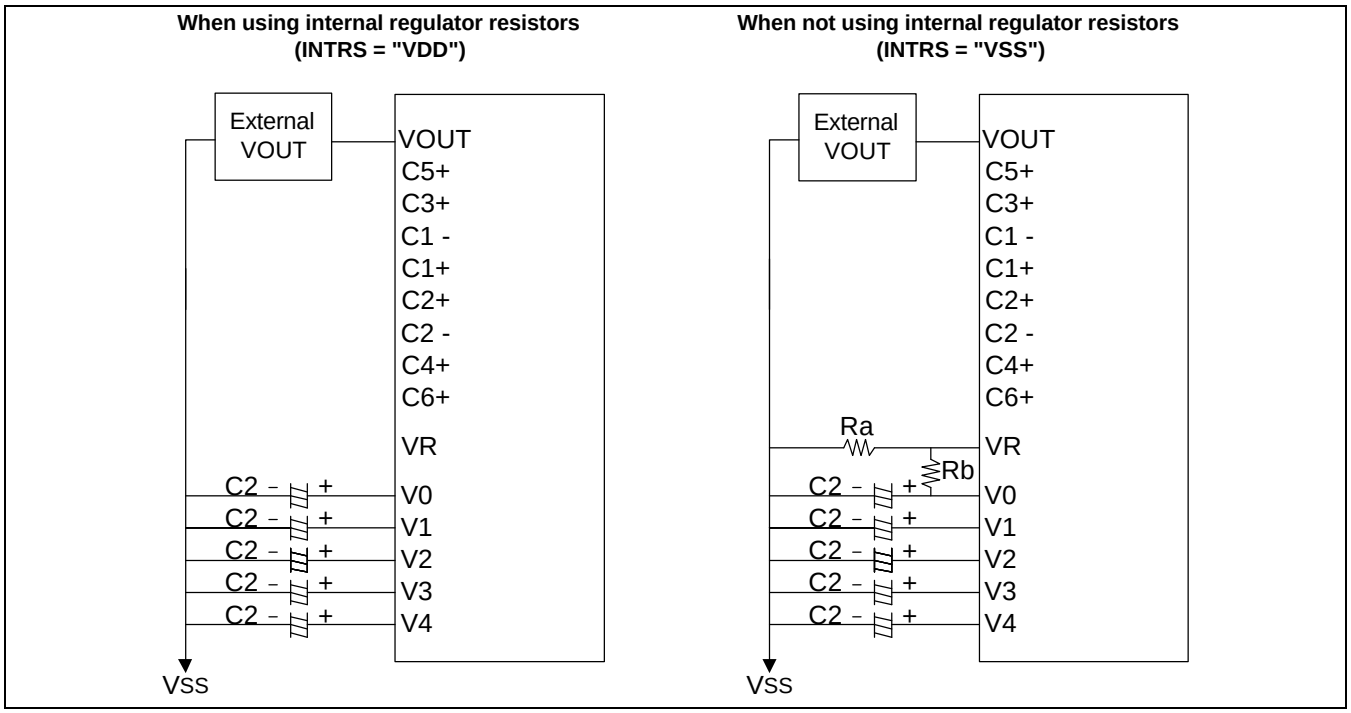


Figure 18. When Using some LCD Power Circuits (V/C: OFF, V/R: ON, V/F: ON)

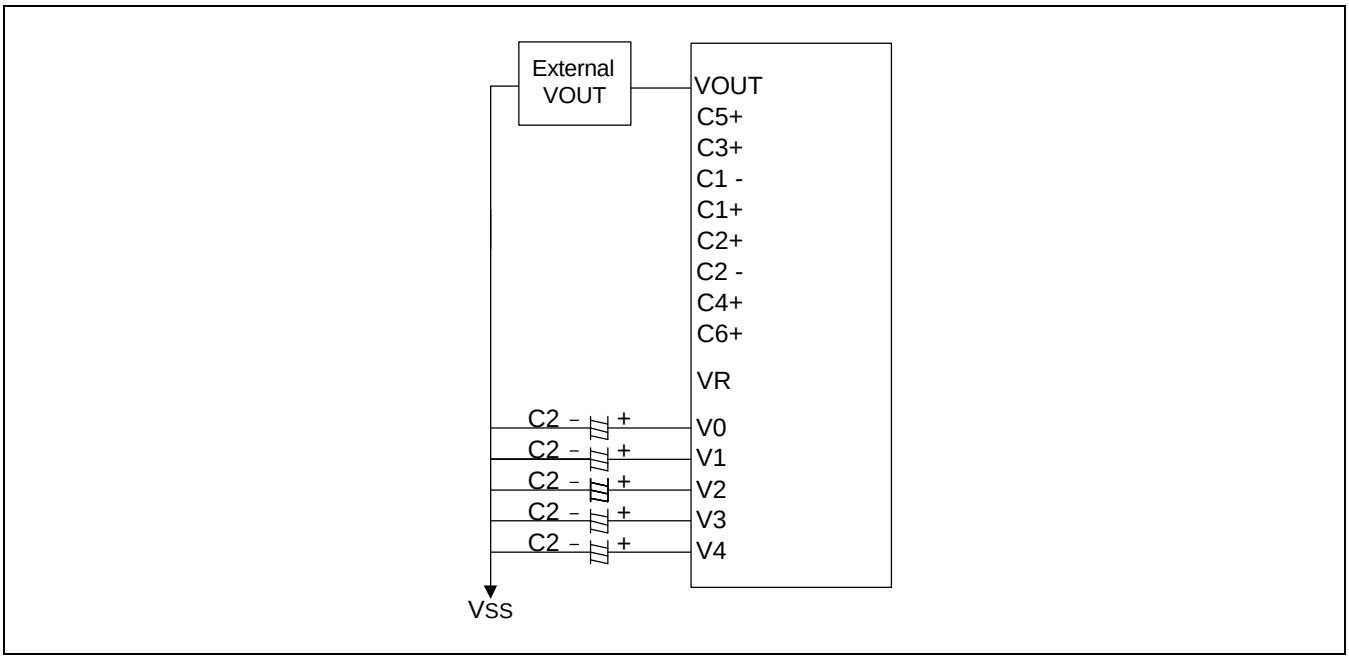


Figure 19. When Using only Voltage Follower Circuit (V/C: OFF, V/R: OFF, V/F: ON)

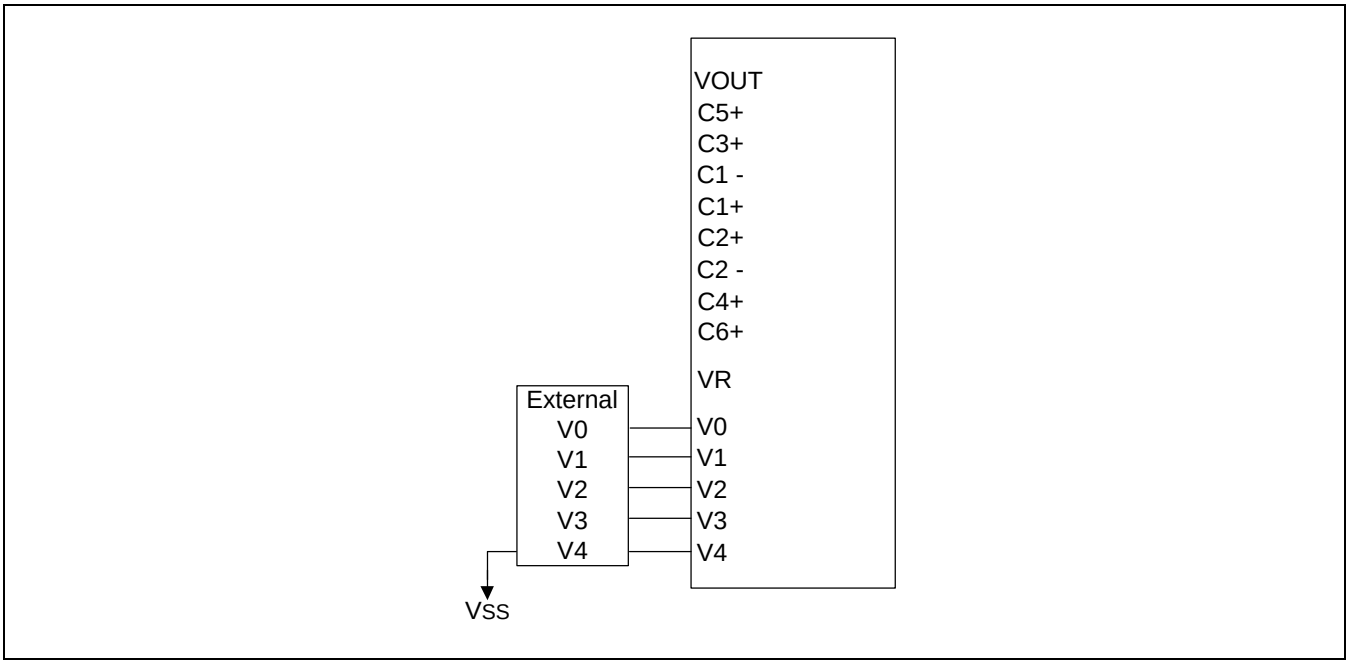


Figure 20. When Not Using all LCD Power Circuits (V/C: OFF, V/R: OFF, V/F: OFF)

RESET CIRCUIT

Setting RESETB to “L” or Reset instruction can initialize internal function.
When RESETB becomes “L”, following procedure is occurred.

Page address: 0
Column address: 0
Modify-read: Off
Display On / Off: Off
Initial display line: 0 (first)
Initial COM0 register: 0 (COM0)
Partial display duty ratio: 1/128
Reverse display On / Off: Off (normal)
n-line inversion register: 0 (disable)
Entire display On / Off: Off (normal)
Power control register (VC, VR, VF) = (0, 0, 0)
DC-DC step up: 3 times converter circuit = (0, 0, 0)
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Reference voltage control register: (EV5, EV4, EV3, EV2, EV1, EV0) = (1, 0, 0, 0, 0, 0)
LCD bias ratio: 1/12
SHL select: Off (normal)
ADC select: Off (normal)
Oscillator status: Off
Power save mode: release

When RESET instruction is issued, following procedure is occurred.

Page address: 0
Column address: 0
Modify-read: Off
Initial display line: 0 (first)
Regulator resistor select register: (R2, R1, R0) = (0, 0, 0)
Reference voltage control register (EV5, EV4, EV3, EV2, EV1, EV0) = (1, 0, 0, 0, 0, 0)

While RESETB is “L” or reset instruction is executed, no instruction except read status could be accepted. Reset status appears at DB4. After DB4 becomes ”L”, any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

INSTRUCTION DESCRIPTION

Table 17. Instruction Table

× : Don't care

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description
Read display data	1	1	Read data								Read data from DDRAM
Write display data	1	0	Write data								Write data into DDRAM
Read status	0	1	BUSY	ADC	ON	RES	0	0	0	0	Read the internal status
Set page address	0	0	1	0	1	1	P3	P2	P1	P0	Set page address
Set column address MSB	0	0	0	0	0	1	Y7	Y6	Y5	Y4	Set column address MSB
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0	Set column address LSB
Set modify-read	0	0	1	1	1	0	0	0	0	0	Set modify-read mode
Reset modify-read	0	0	1	1	1	0	1	1	1	0	release modify-read mode
Display ON / OFF	0	0	1	0	1	0	1	1	1	D	D = 0: display OFF D = 1: display ON
Set initial display line register	0	0	0	1	0	0	0	0	×	×	2-byte instruction to specify the initial display line to realize vertical scrolling
	0	0	×	S6	S5	S4	S3	S2	S1	S0	
Set initial COM0 register	0	0	0	1	0	0	0	1	×	×	2-byte instruction to specify the initial COM0 to realize window scrolling
	0	0	×	C6	C5	C4	C3	C2	C1	C0	
Set partial display duty ratio	0	0	0	1	0	0	1	0	×	×	2-byte instruction to set partial display duty ratio
	0	0	D7	D6	D5	D4	D3	D2	D1	D0	
Set N-line inversion	0	0	0	1	0	0	1	1	×	×	2-byte instruction to set n-line inversion register
	0	0	×	×	×	N4	N3	N2	N1	N0	
Release N-line inversion	0	0	1	1	1	0	0	1	0	0	Release N-line Inversion mode
Reverse display ON / OFF	0	0	1	0	1	0	0	1	1	REV	REV = 0: normal display REV = 1: reverse display
Entire display ON / OFF	0	0	1	0	1	0	0	1	0	EON	EON = 0: normal display EON = 1: entire display ON
Power control	0	0	0	0	1	0	1	VC	VR	VF	Control power circuit operation
Select DC-DC step-up	0	0	0	1	1	0	0	DC2	DC1	DC0	Select the step-up of the internal voltage converter
Select regulator resistor	0	0	0	0	1	0	0	R2	R1	R0	Select internal resistance ratio of the regulator resistor
Set electronic volume register	0	0	1	0	0	0	0	0	0	1	2-byte instruction to specify the electronic volume register
	0	0	×	×	EV5	EV4	EV3	EV2	EV1	EV0	
Select LCD bias	0	0	0	1	0	1	0	B2	B1	B0	Select LCD bias
SHL select	0	0	1	1	0	0	SHL	×	×	×	COM bi-directional selection SHL = 0: normal direction SHL = 1: reverse direction
ADC select	0	0	1	0	1	0	0	0	0	ADC	SEG bi-directional selection ADC = 0: normal direction ADC = 1: reverse direction
Oscillator ON start	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator
Set power save mode	0	0	1	0	1	0	1	0	0	1	Power save mode
Release power save mode	0	0	1	1	1	0	0	0	0	1	Release power save mode
Set DDL register	0	0	0	1	1	1	0	0	0	0	Set DDL register in 3-pin serial mode
Reset	0	0	1	1	1	0	0	0	1	0	Initialize the internal functions
NOP	0	0	1	1	1	0	0	0	1	1	***No operation***
Test instruction	0	0	1	1	1	1	×	×	×	×	***Don't use this instruction.***

Read Display Data

8-bit data from Display Data RAM specified by the column address and page address can be read by this instruction. As the column address is incremented by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display data cannot be read through the serial interface.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read data							

Write Display Data

8-bit data of display data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is incremented by 1 automatically so that the microprocessor can continuously write data to the addressed page.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write data							

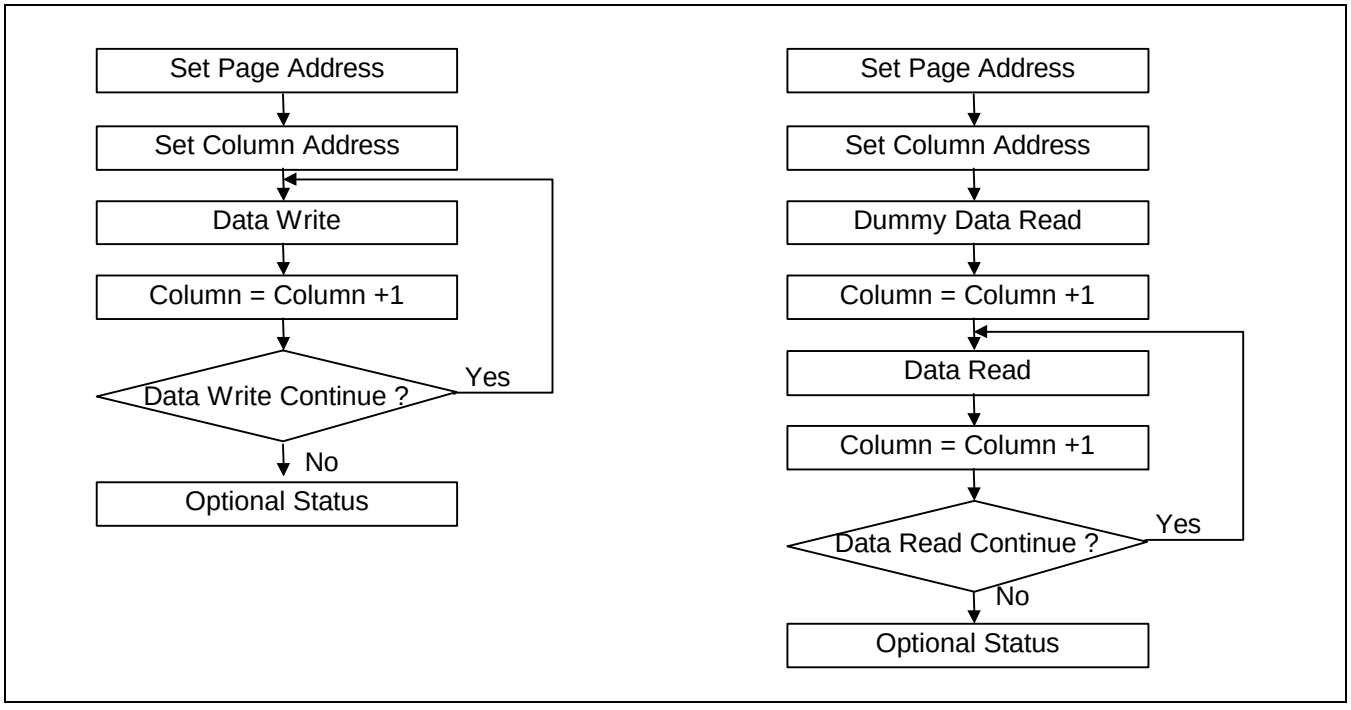


Figure 21. Sequence for Writing Display Data

Figure 22. Sequence for Reading Display Data

Read Status

Indicates the internal status of the S6B0728

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BUSY	ADC	ON	RES	0	0	0	0

Flag	Description
BUSY	The device is busy when internal operation or reset Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy.
ADC	Indicates the relationship between RAM column address and segment driver. 0: reverse direction (SEG131 → SEG0), 1: normal direction (SEG0 → SEG131)
ON	Indicates display ON / OFF status 0: display ON, 1: display OFF
RES	Indicates the initialization is in progress by RESETB signal 0: chip is active, 1: chip is being reset.

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the Page Address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't effect to the display status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	P3	P2	P1	P0

P3	P2	P1	P0	Specified page address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
:	:	:	:	:
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Set Column Address

Sets the Column Address of display RAM from the microprocessor into the Column Address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically incremented.

Set Column Address MSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	Y7	Y6	Y5	Y4

Set Column Address LSB

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	Y3	Y2	Y1	Y0

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	Selected column address
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	1	129
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131
1	0	0	0	0	1	0	0	Not accessible column
1	0	0	0	0	1	0	1	
:	:	:	:	:	:	:	:	
1	1	1	1	1	1	1	0	
1	1	1	1	1	1	1	1	

Set Modify-Read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-read instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	0

Reset Modify-Read

This instruction cancels the Modify-read mode, and makes the column address return to its initial value just before the set Modify-read instruction is started.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	1	1	1	0

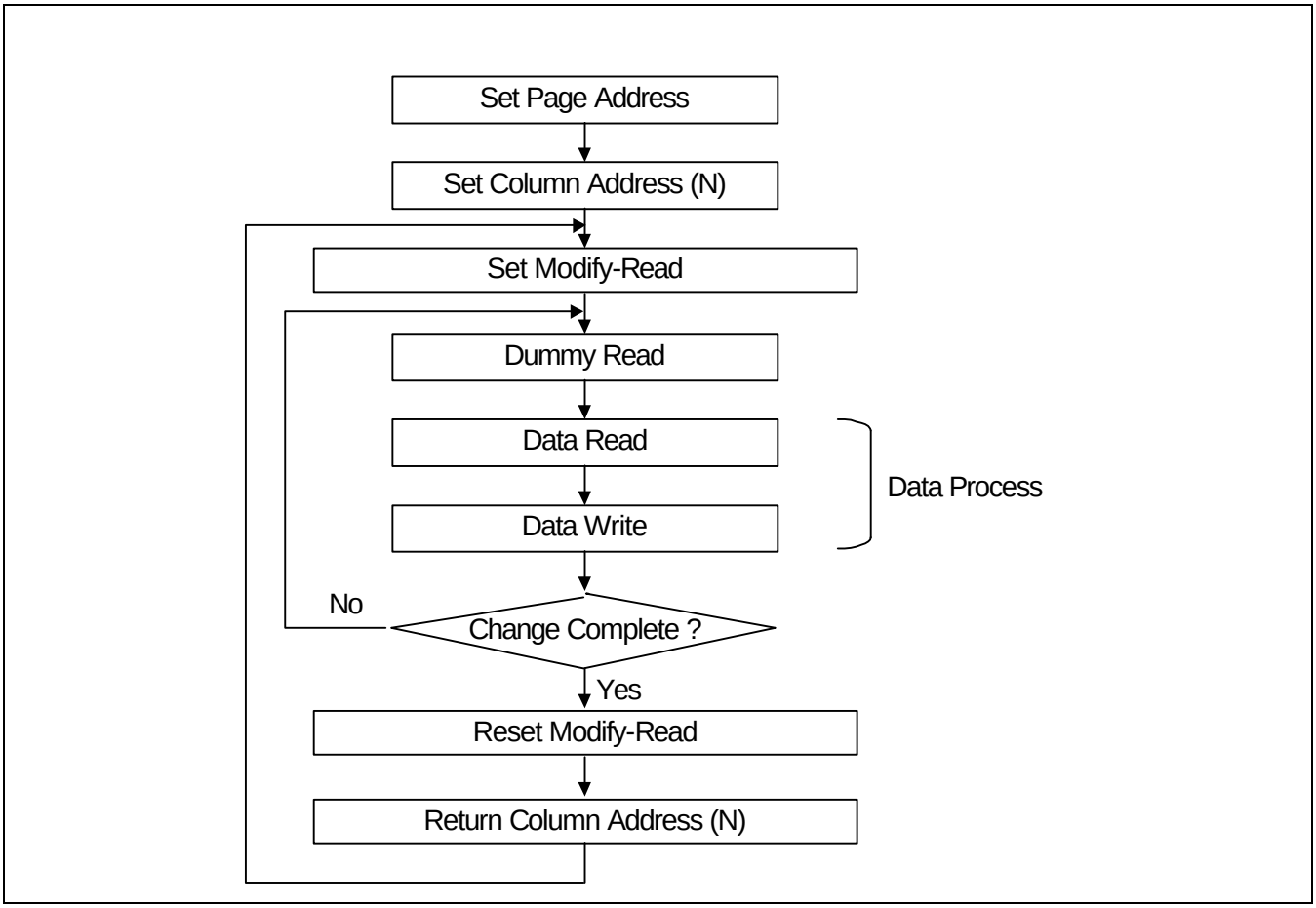


Figure 23. Sequence for Cursor Display

Display ON / OFF

Turns the Display ON or OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	1	1	D

D = 1: display ON
D = 0: display OFF

Set Initial Display Line Register

Sets the line address of display RAM to determine the initial display line using 2-byte instruction. The RAM display data is displayed at the top row (COM0) of LCD panel.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	S6	S5	S4	S3	S2	S1	S0

S6	S5	S4	S3	S2	S1	S0	Selected line address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	126
1	1	1	1	1	1	1	127

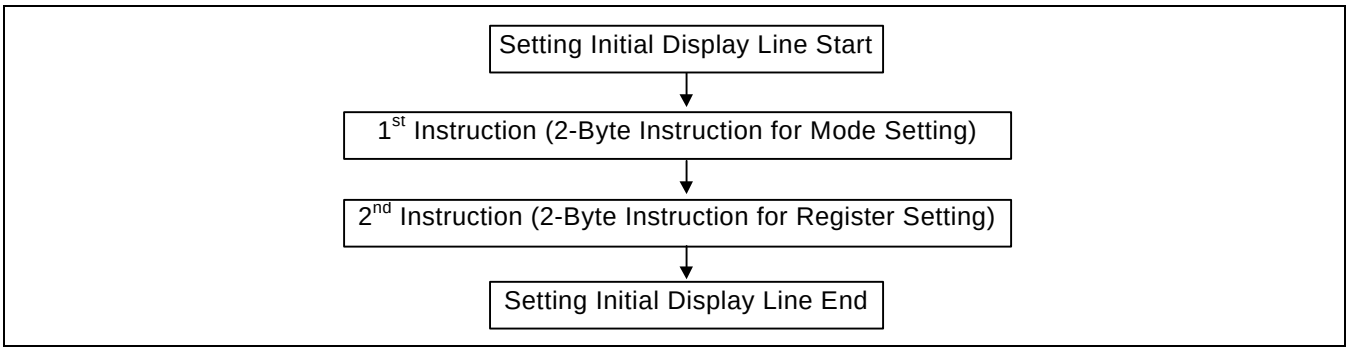


Figure 24. The Sequence for Setting the Initial Display Line

Set Initial COM0 Register

Sets the initial row (COM) of the LCD panel using the 2-byte instruction. By using this instruction, it is possible to realize the window moving without the change of display data.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	1	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	C6	C5	C4	C3	C2	C1	C0

C6	C5	C4	C3	C2	C1	C0	Initial COM0
0	0	0	0	0	0	0	COM0
0	0	0	0	0	0	1	COM1
0	0	0	0	0	1	0	COM2
:	:	:	:	:	:	:	:
1	1	1	1	1	0	1	COM125
1	1	1	1	1	1	0	COM126
1	1	1	1	1	1	1	COM127

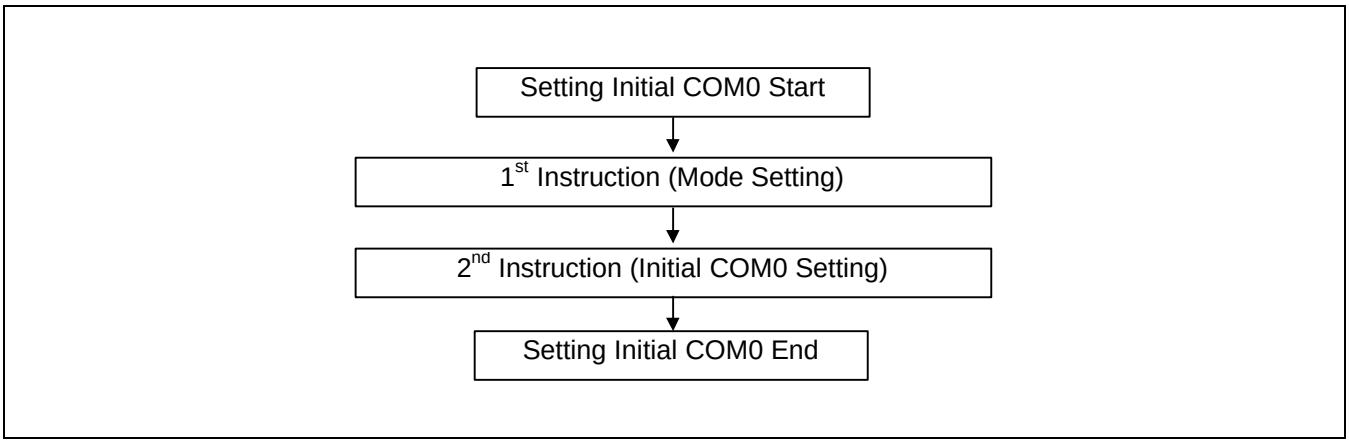


Figure 25. Sequence for Setting the Initial COM0

Set Partial Display Duty Ratio

Sets the duty ratio within range of 16 to 128 to realize Partial Display by using the 2-byte instruction.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	0	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	D7	D6	D5	D4	D3	D2	D1	D0

D7	D6	D5	D4	D3	D2	D1	D0	partial duty ratio
0	0	0	1	0	0	0	0	1/16
0	0	0	1	0	0	0	1	1/17
:	:	:	:	:	:	:	:	:
0	1	1	1	1	1	1	1	1/127
1	0	0	0	0	0	0	0	1/128
Other combinations								No operation

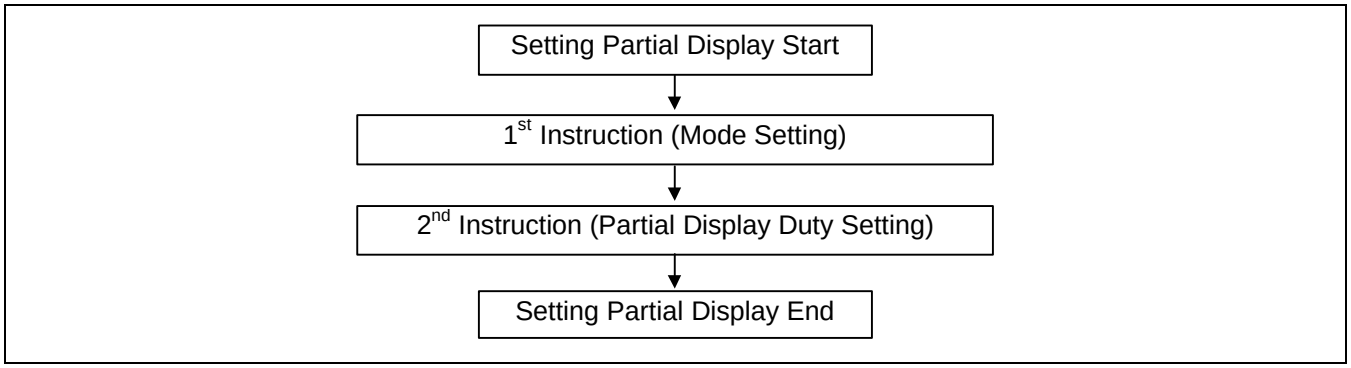


Figure 26. Sequence for Setting Partial Display

Set N-line Inversion Register

Sets the inverted line number within range of 2 to 32 to improve the display quality by controlling the phase of the internal LCD AC signal (M) by using the 2-byte instruction.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	1	1	×	×

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	**0**	´	´	´	**N4**	**N3**	**N2**	**N1**	**N0**

N4	N3	N2	N1	N0	Selected n-line inversion
0	0	0	0	0	0-line inversion (frame inversion)
0	0	0	0	1	2-line inversion
0	0	0	1	0	3-line inversion
0	0	0	1	1	4-line inversion
:	:	:	:	:	:
1	1	1	0	1	30-line inversion
1	1	1	1	0	31-line inversion
1	1	1	1	1	32-line inversion

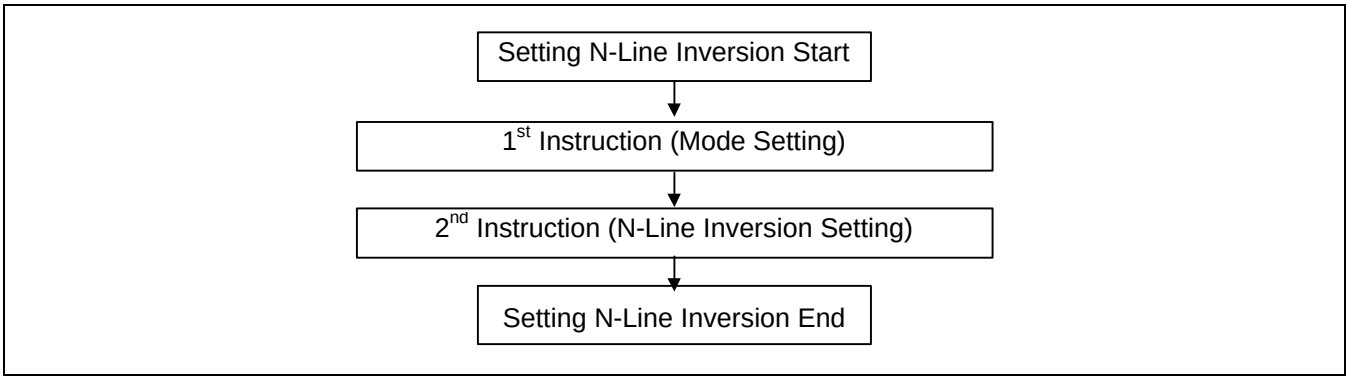


Figure 27. Sequence for Setting Partial Display

Release N-line Inversion

Returns to the frame inversion condition from the n-line inversion condition.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	1	0	0

Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	1	REV

REV	RAM bit data = “1”	RAM bit data = “0”
0 (normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (reverse)	LCD pixel is not illuminated	LCD pixel is illuminated

Entire Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the reverse Display ON / OFF instruction.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	1	0	EON

EON	RAM bit data = “1”	RAM bit data = “0”
0 (Normal)	LCD pixel is illuminated	LCD pixel is not illuminated
1 (Entire)	LCD pixel is illuminated	LCD pixel is illuminated

Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	1	VC	VR	VF

VC	VR	VF	Status of internal power supply circuits
0			Internal voltage converter circuit is OFF
1			Internal voltage converter circuit is ON
	0		Internal voltage regulator circuit is OFF
	1		Internal voltage regulator circuit is ON
		0	Internal voltage follower circuit is OFF
		1	Internal voltage follower circuit is ON

Select DC/DC Step-up

Selects one of 5 DC/DC step-up to reduce the power consumption by this instruction. It is very useful to realize the partial display function.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	0	DC2	DC1	DC0

DC1	DC0	DC0	Selected DC-DC converter circuit
0	0	0	3 times boosting circuit
0	0	1	4 times boosting circuit
0	1	0	5 times boosting circuit
0	1	1	6 times boosting circuit
1	0	0	7 times boosting circuit

Regulator Resistor Select

Selects resistance ratio of the internal resistor used in the internal voltage regulator. See voltage regulator section in power supply circuit. Refer to the table 15.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	0	0	R2	R1	R0

R2	R1	R0	[Rb / Ra] ratio
0	0	0	Small
0	0	1	:
:	:	:	:
1	1	0	:
1	1	1	Large

Set Electronic Volume Register

Consists of 2-byte instruction. The 1st instruction sets Electronic Volume mode, the 2nd one updates the contents of Electronic Volume register. After second instruction, Electronic Volume mode is released.

The 1st Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	0	0	0	1

The 2nd Instruction

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	×	×	EV5	EV4	EV3	EV2	EV1	EV0

EV5	EV4	EV3	EV2	EV1	EV0	Reference voltage (a)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

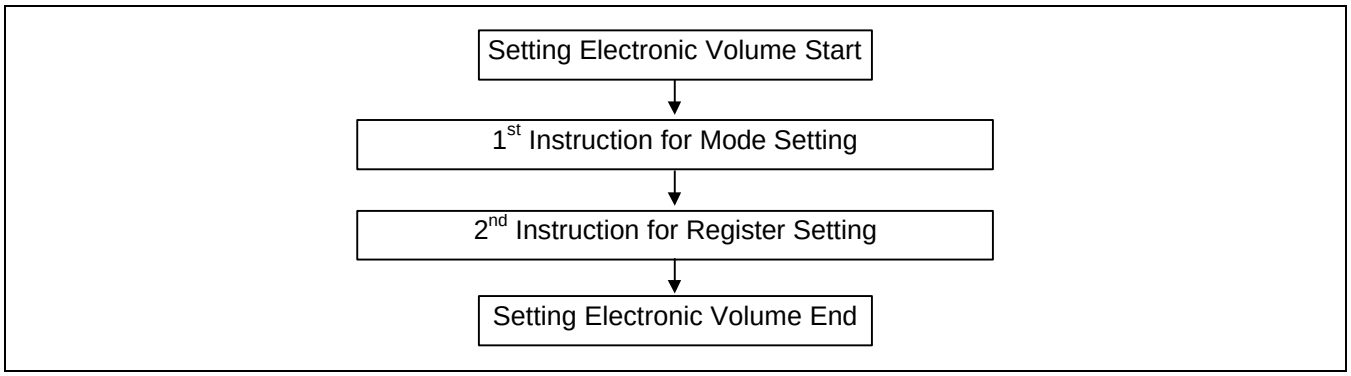


Figure 28. Sequence for Setting the Electronic Volume

Select LCD Bias

Selects LCD Bias ratio of the voltage required for driving the LCD.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	1	0	B2	B1	B0

B2	B1	B0	Selected LCD bias
0	0	0	1/5
0	0	1	1/6
0	1	0	1/7
0	1	1	1/8
1	0	0	1/9
1	0	1	1/10
1	1	0	1/11
1	1	1	1/12

SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	0	0	SHL	×	×	×

SHL = 0: normal direction (COM0 → COM127)
SHL = 1: reverse direction (COM127 → COM0)

ADC Select

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins can be reversed by software. This makes IC layout flexible in LCD module assembly.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	0	0	0	ADC

ADC = 0: normal direction (SEG0 → SEG131)
ADC = 1: reverse direction (SEG131 → SEG0)

Oscillator ON Start

This instruction enables the built-in oscillator circuit.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	1	1

Reset

This instruction resets initial display line, column address, page address, and common output status select to their initial status, but dose not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply that is initialized by the RESETB pin.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	0

Power Save

The S6B0728 enters the Power Save status to reduce the power consumption to the static power consumption value and returns to the normal operation status by the following instructions.

Set Power Save Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	0	1	0	0	1

Release Power Save Mode

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	0	1

The internal status during power save mode are as follows :

- Oscillator circuit : off
- LCD power supply circuit : off
- All COM / SEG output level : VSS
- Consumption Current < 2μA

NOP

Non-operation

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	0	0	0	1	1

Test Instruction

This instruction is for testing IC. Please do not use it.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	1	1	×	×	×	×

Referential Instruction Setup Flow: Initializing with the Built-in Power Supply Circuits

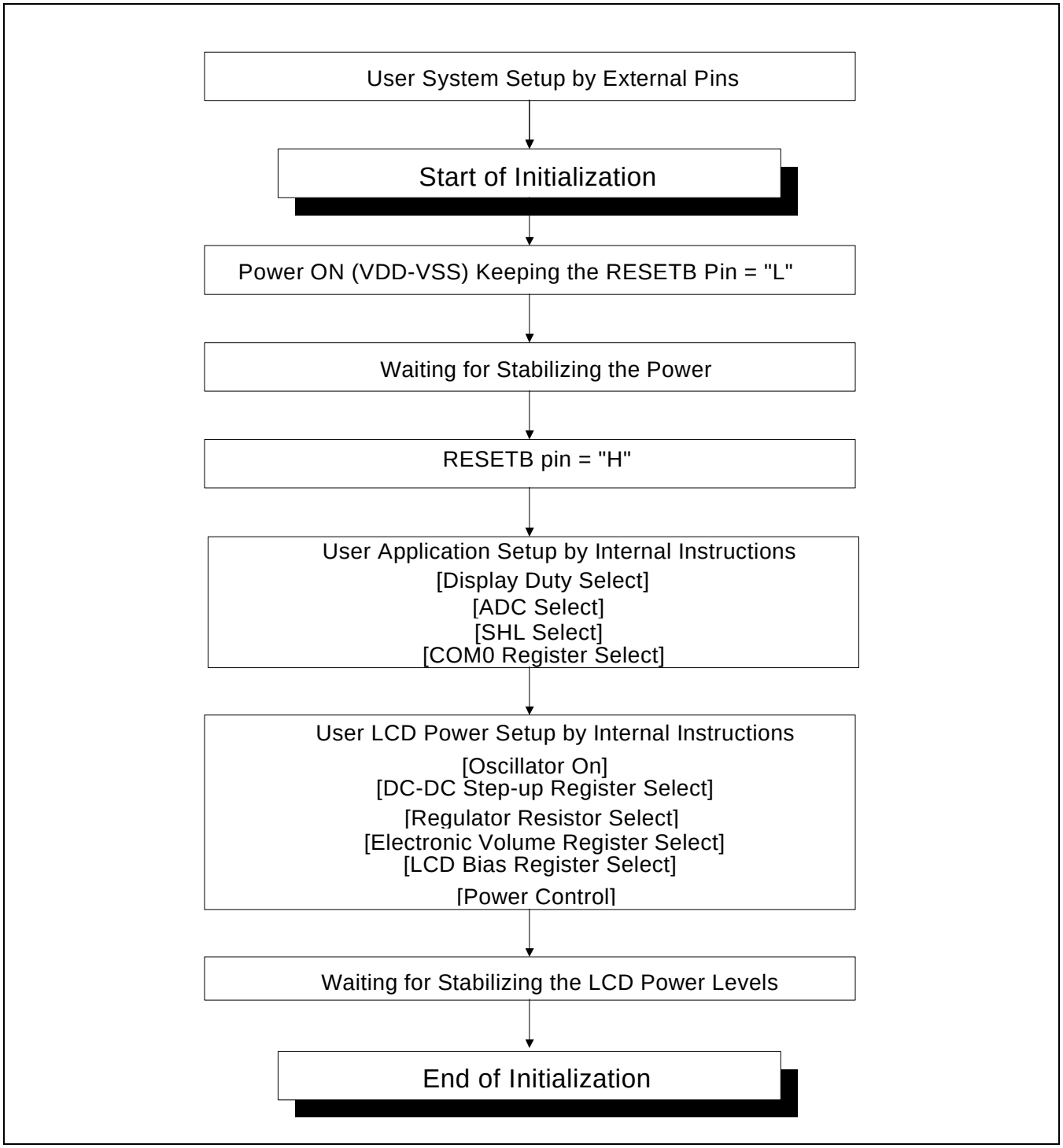


Figure 29. Initializing with the Built-in Power Supply Circuits

Referential Instruction Setup Flow: Initializing without the Built-in Power Supply Circuits

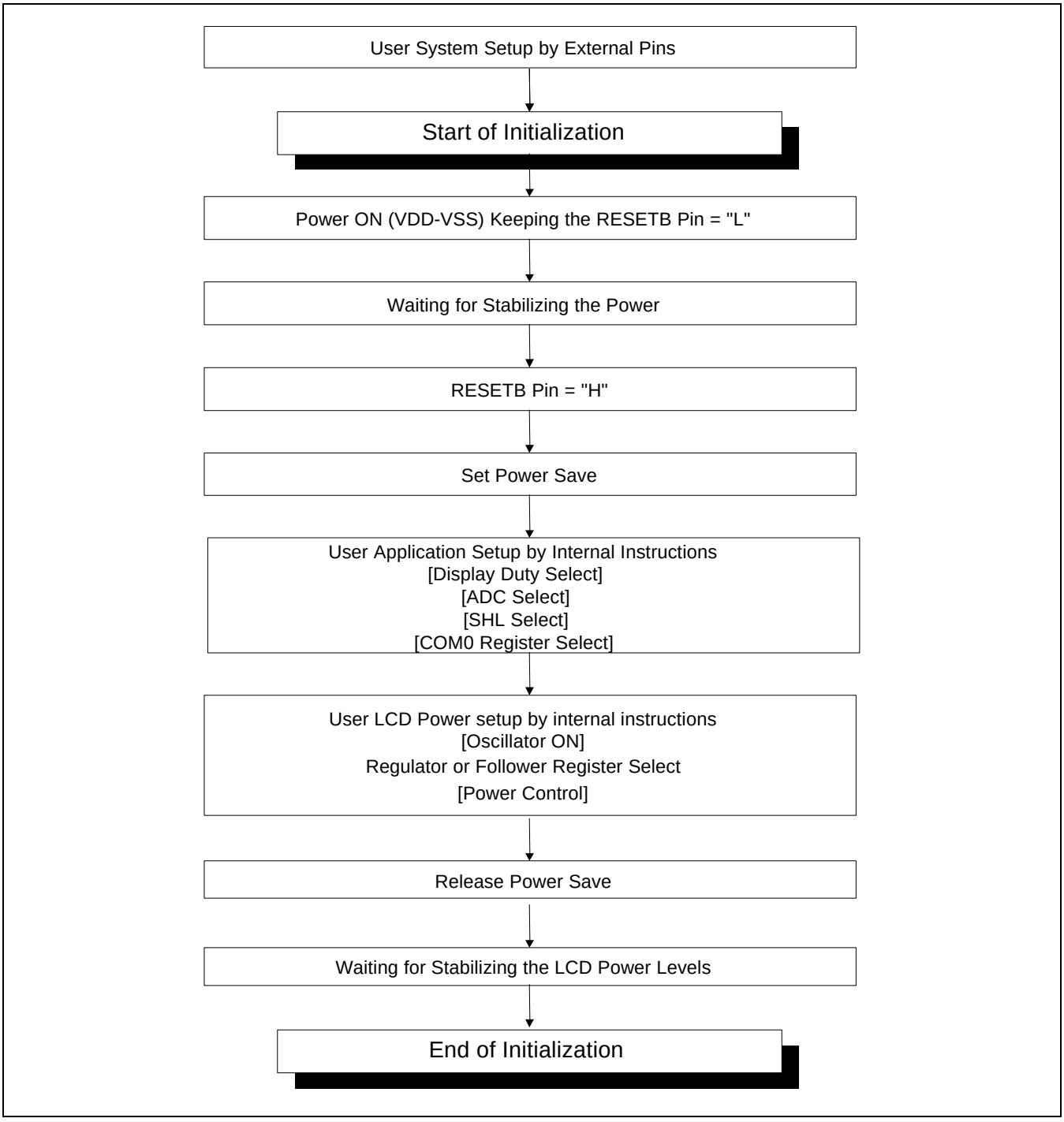


Figure 30. Initializing without the Built-in Power Supply Circuits

Referential Instruction Setup Flow: Data Displaying

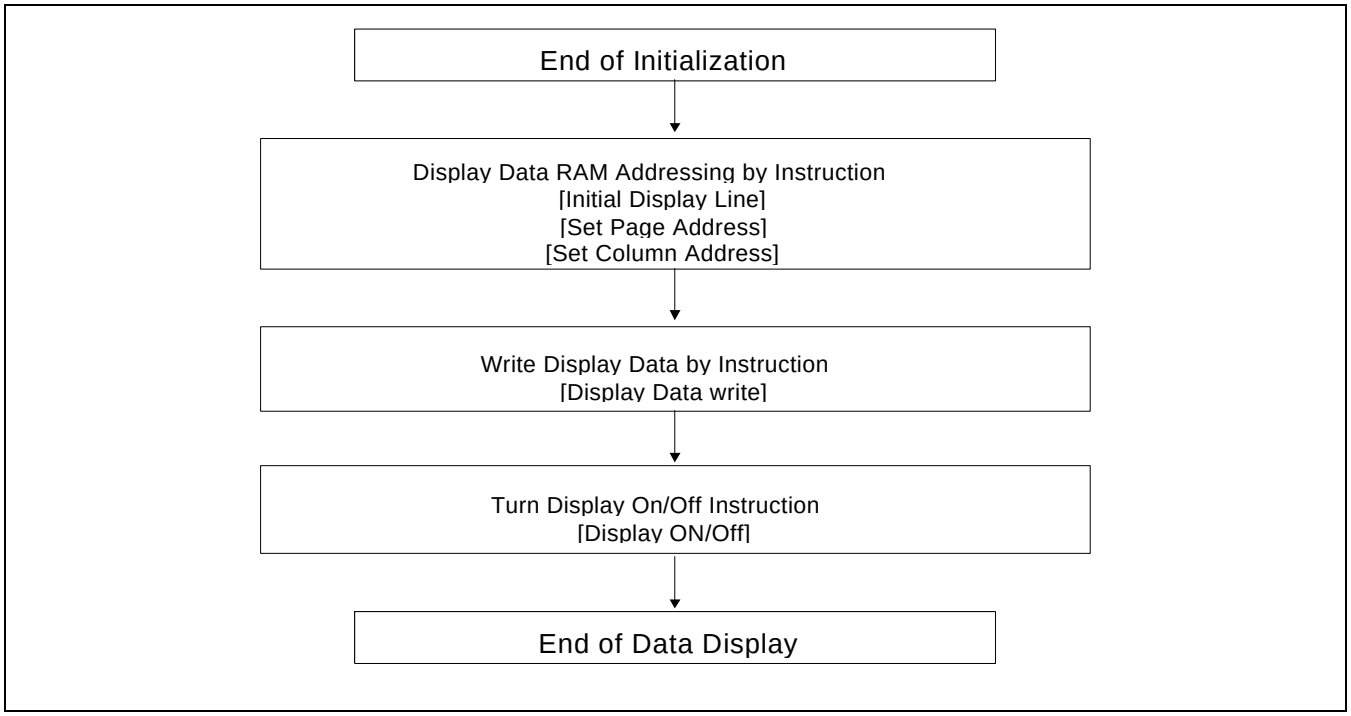


Figure 31. Data Displaying

Referential Instruction Setup Flow: Power OFF

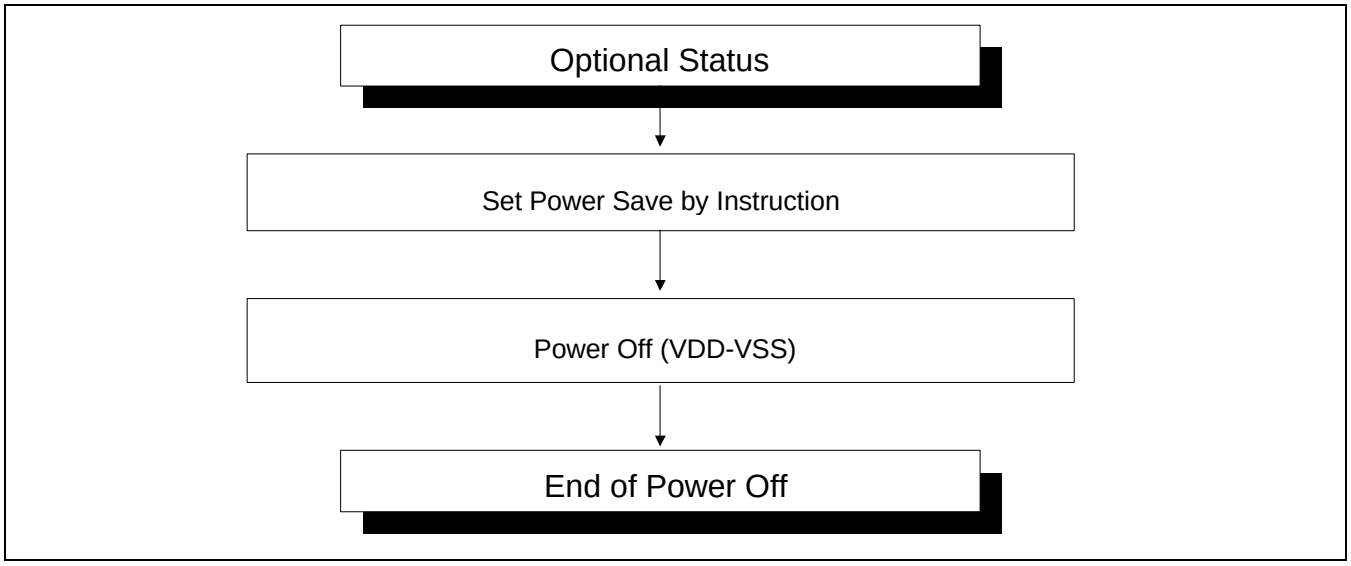


Figure 32. Power OFF

Referential Instruction Setup Flow: Partial Duty Changing

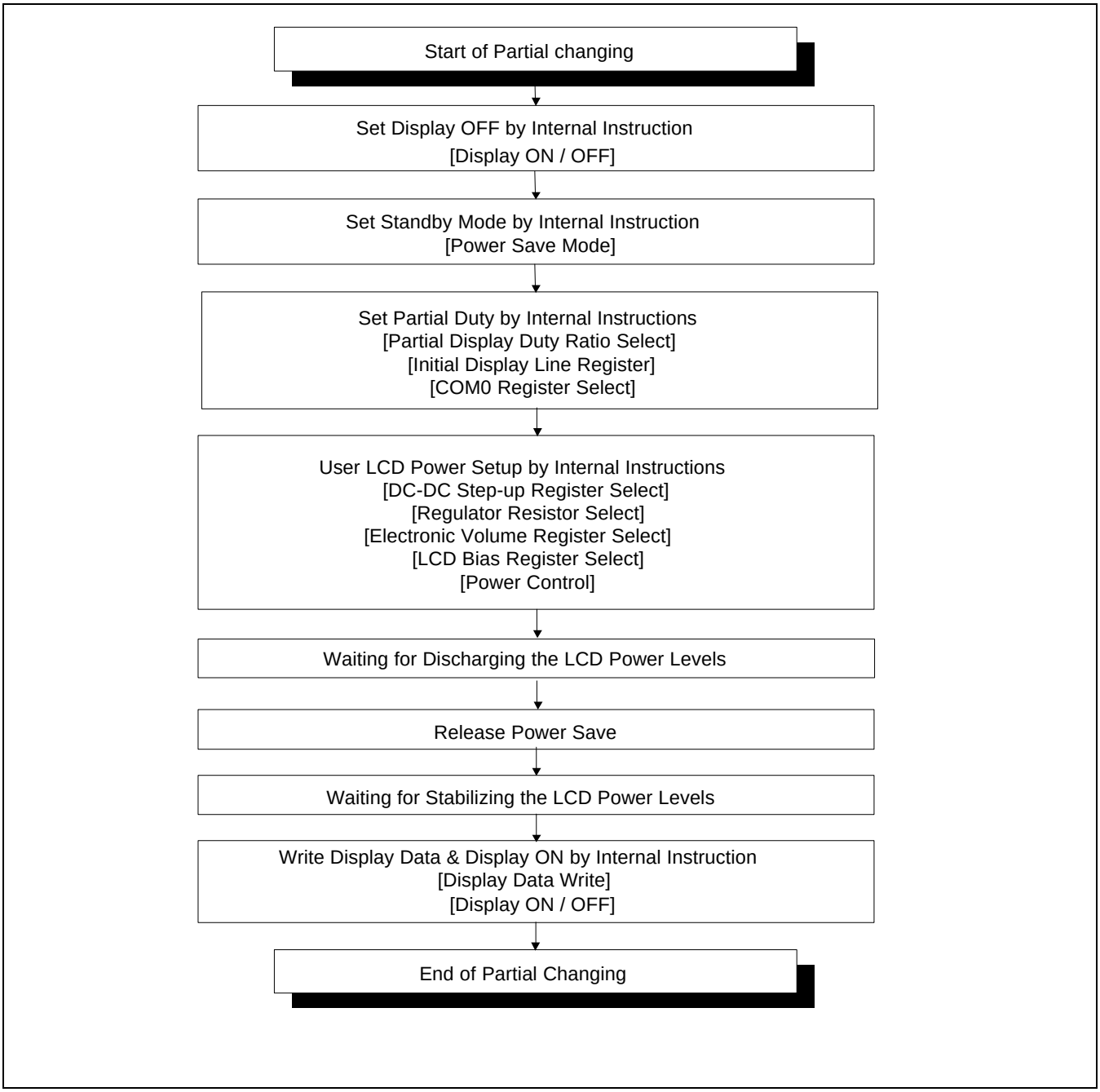


Figure 33. Partial Duty Changing

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 18. Absolute Maximum Ratings

(Vss = 0V)

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	- 0.3 ~ + 7.0	V
	V0, VOUT	+ 0.3 ~ + 20.0	V
	V1, V2, V3, V4	+ 0.3 ~ V0	V
External reference voltage	VEXT	+0.3 ~ V_{DD}	
Input voltage range	V_{IN}	- 0.3 ~ V_{DD} + 0.3	V
Operating temperature range	T_{OPR}	- 40 ~ + 85	°C
Storage temperature range	T_{STR}	- 55 ~ + 125	°C

NOTES :

1. VDD, V0, VOUT, V1 to V4, VEXT and VCI are based on Vss = 0V.
2. Voltage VOUT ≥ V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS must always be satisfied.
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently. It is desirable to use this LSI under electrical characteristic conditions during general operation. Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 19. DC Characteristics

(V_{SS} = 0V, V_{DD} = 2.4 to 3.6V, Ta = -40~85°C)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Operating voltage (1)		V_{DD}		2.4	-	3.6	V	V_{DD} *1
Operating voltage (2)		V0		4.0	-	17.0	V	V0, *2
Input voltage	High	V_{IH}		0.8V_{DD}	-	V_{DD}	V	*3
	Low	V_{IL}		V_{SS}	-	0.2V_{DD}		
Output voltage	High	V_{OH}	I_{OH} = -0.5mA	0.8V_{DD}	-	V_{DD}	V	*4
	Low	V_{OL}	I_{OL} = 0.5mA	V_{SS}	-	0.2V_{DD}		
Input leakage current		I_{IL}	V_{IN} = V_{DD} or V_{SS}	- 1.0	-	+ 1.0	µA	*3
Output leakage current		I_{OZ}	V_{IN} = V_{DD} or V_{SS}	- 3.0	-	+ 3.0	µA	*5
LCD driver ON resistance		R_{ON}	Ta = 25°C, V0 = 8V	-	2.0	3.0	kΩ	SEGn COMn *6
Frame frequency		f_{FR}	Ta = 25°C	70	85	100	Hz	*7 FR

Table 20. DC Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Voltage converter circuit output voltage	VOUT	×3/ ×4/ ×5/ ×6/ ×7/ voltage conversion (no-load)	95	99	-	%	VOUT
Voltage regulator circuit operating voltage	VOUT		6.0	-	19.0	V	VOUT
Voltage follower circuit operating voltage	V0		4.0	-	17.0	V	V0 *8
Reference voltage	V_{REF}	Ta = 25°C	1.940	2.000	2.060	V	*9

Dynamic Current Consumption (1) when an External Power Supply is used.

Table 21. Display OFF

(VDD = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (1)	IDD1	V0 - Vss = 10.0V, duty = 1/64			TBD	µA	*10
		V0 - Vss = 15.0V, duty = 1/128			TBD		

Table 22. Checker Pattern

(VDD = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (1)	IDD1	V0 - Vss = 10.0V, duty = 1/64			TBD	µA	*10
		V0 - Vss = 15.0V, duty = 1/128			TBD		

Dynamic Current Consumption (2) when the Internal Power Supply is ON

Table 23. Display OFF

(VDD = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (2)	IDD2	V0 - Vss = 10.0V, X4 boosting, duty = 1/64, bias = 1/9	-	-	TBD	µA	*10
		V0 - Vss = 15.0V, X6 boosting, duty = 1/128, bias = 1/12	-	-	TBD	µA	*10

Table 24. Check Pattern

(VDD = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Dynamic current consumption (2)	IDD2	V0 - Vss = 10.0V, X4 boosting, duty = 1/64, bias = 1/9	-	-	TBD	µA	*10
		V0 - Vss = 15.0V, X6 boosting, duty = 1/128, bias = 1/12	-	-	TBD		

Dynamic Current Consumption during Power Save Mode

Table 25. Power Save Mode

(VDD = 3.0V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin used
Power save mode current	IDDS	During power save	-	-	2	µA	

Table 26. The Relationship between Oscillation Frequency and Frame Frequency

Duty ratio	Item	f_{CL}	f_{osc}
1/N	On-chip oscillator circuit is used	f_{FR} x N	f_{FR} x 2 x N

(f_{OSC}: oscillation frequency, f_{CL}: display clock frequency, f_{FR}: frame frequency, N = 16 to 128)

[* Remark Solves]
*1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
*2. In case of external power supply is applied.
*3. CS1B, CS2, RS, DB0 to DB7, E_RD, RW_WR, RESETB, C68, PS, INTRS, REF, CL, M
*4. DB0 to DB7, CL, M
*5. Applies when the DB0 to DB7 pins are in high impedance.
*6. Resistance value when -0.1[mA] is applied during the On status of the output pin SEGn or COMn.
RON [kΩ] = ΔV[V] / 0.1[mA] (ΔV : voltage change when -0.1[mA] is applied in the ON status.)
*7. See Table 26 for the relationship between oscillation frequency and frame frequency.
*8. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range.
*9. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
*10. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
The current consumption, when the built-in power supply circuit is on or OFF.
The current flowing through voltage regulation resistors (Rb and Ra) is not included.
It does not include the current of the LCD panel capacity, wiring capacity, etc.

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)

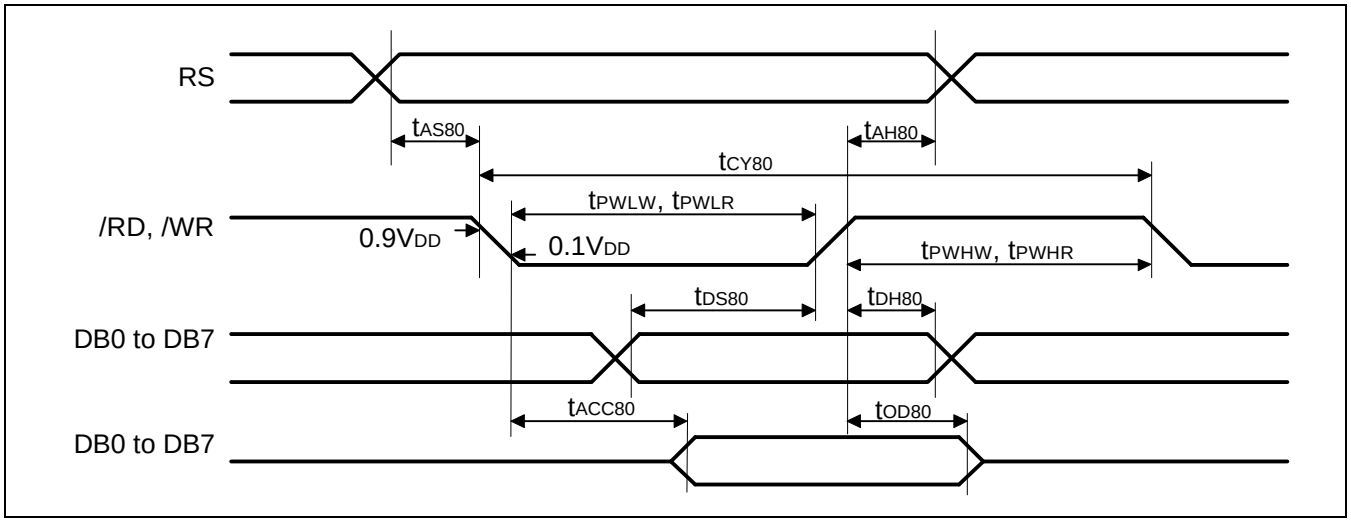


Figure 34. Parallel Interface (8080-series MPU) Timing Diagram

Table 27. AC Characteristics (8080-series Parallel Mode)

(V_{DD} = 2.4 ~ 3.6V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	RS	t_{AS80} t_{AH80}		TBD TBD	- -	ns
System cycle time		t_{CY80}		TBD	-	ns
Pulse width low for write Pulse width High for write	RW_WR (/WR)	t_{PWLW} t_{PWHW}		TBD TBD	- -	ns
Pulse width low for read Pulse width high for read	E_RD (/RD)	t_{PWLR} t_{PWHR}		TBD TBD	- -	ns
Data setup time Data hold time	DB0 to DB7	t_{DS80} t_{DH80}		TBD TBD	- -	ns
Read access time Output disable time		t_{ACC80} t_{OD80}	CL = 100 pF	TBD TBD	TBD TBD	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(tr + tf) < (tCY80 - tPWLW - tPWHW) for write, (tr + tf) < (tCY80 - tPWLR - tPWHR) for read

Read / Write Characteristics (6800-series Microprocessor)

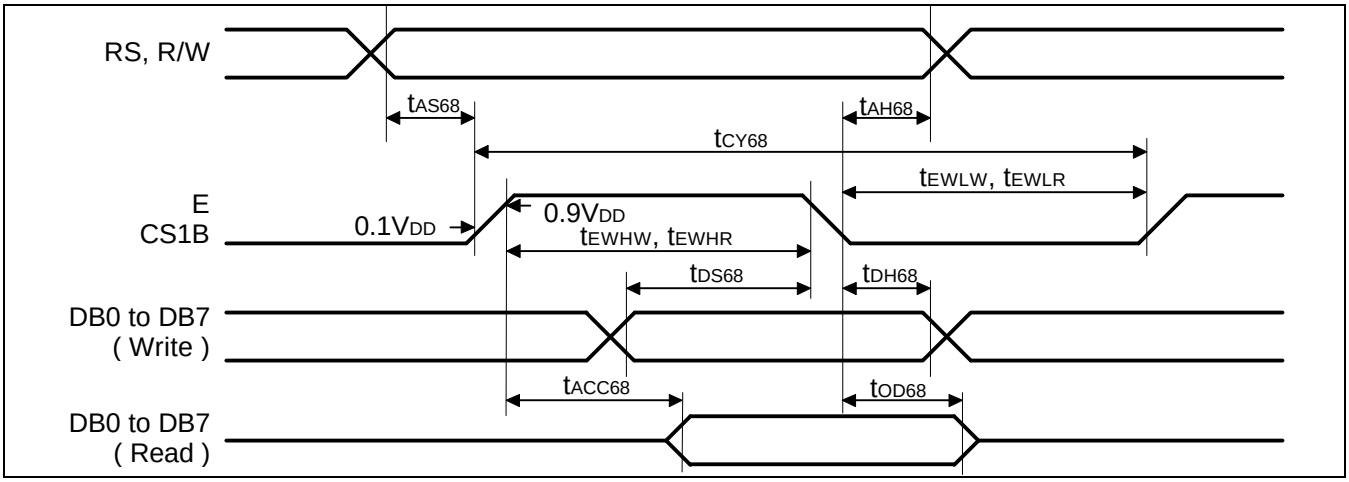


Figure 35. Parallel Interface (6800-series MPU) Timing Diagram

Table 28. AC Characteristics (6800-series Parallel Mode)

(V_{DD} = 2.4 ~ 3.6V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time Address hold time	RS RW	t_{AS68} t_{AH68}		TBD TBD	- -	ns
System cycle time		t_{CY68}		TBD	-	ns
Enable width high for write Enable width low for write	E_RD (E)	t_{EWHW} t_{EWLW}		TBD TBD	- -	ns
Enable width high for read Enable width low for read	E_RD (E)	t_{EWHR} t_{EWLR}		TBD TBD	- -	ns
Data setup time Data hold time	DB0 to DB7	t_{DS68} t_{DH68}		TBD TBD	- -	ns
Read access time Output disable time		t_{ACC68} t_{OD68}	C_L = 100 pF	- TBD	TBD TBD	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.
(tr + tf) < (tCY68 - tEWHW - tEWLW) for write, (tr + tf) < (tCY68 - tEWHR - tEWLR) for read

Serial Interface Characteristics

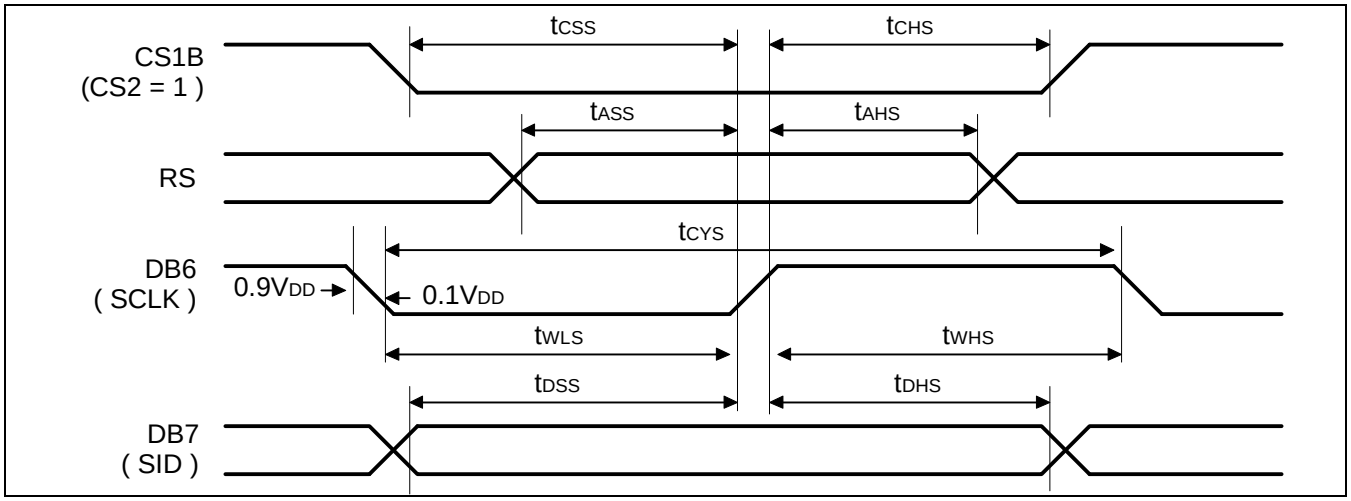


Figure 36. Serial Interface Timing Diagram

Table 29. AC Characteristics (Serial Mode)

(V_{DD} = 2.4 ~ 3.6V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock cycle SCLK high pulse width SCLK low pulse width	DB6 (SCLK)	t_{SCY} t_{SHW} t_{SLW}		TBD TBD TBD	- - -	ns
Address setup time Address hold time	RS	t_{ASS} t_{AHS}		TBD TBD	- -	ns
Data setup time Data hold time	DB7 (SID)	t_{DSS} t_{DHS}		TBD TBD	- -	ns
CS1B setup time CS1B hold time	CS1B	t_{CSS} t_{CHS}		TBD TBD	- -	ns

NOTE: *1. The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Reset Input Timing

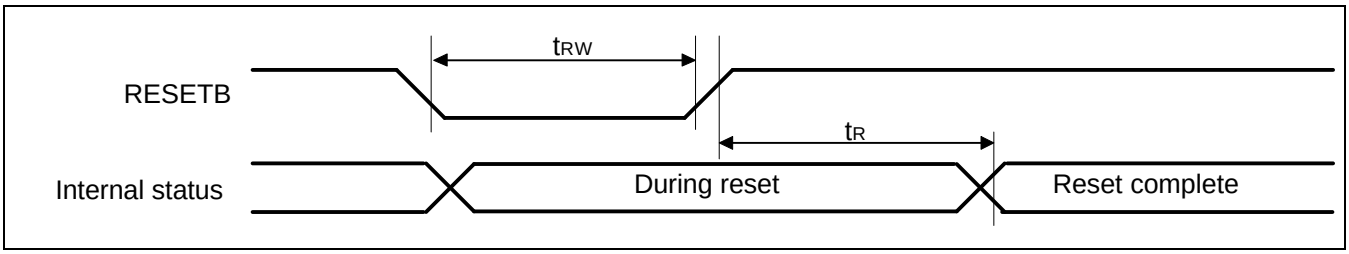


Figure 37. Reset Input Timing Diagram

Table 30. AC Characteristics (Reset mode)

(V_{DD} = 2.4 ~ 3.6V, Ta = -40 ~ +85°C)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Reset low pulse width	RESETB	t_{RW}		1000	-	ns
Reset time	-	t_R		-	1000	ns

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

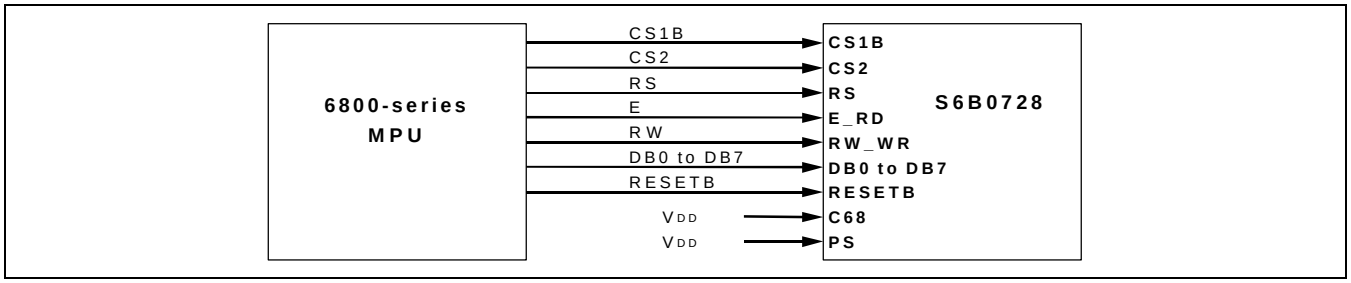


Figure 38. In Case of Interfacing with 6800-series (PS = “H”, C68 = “H”)

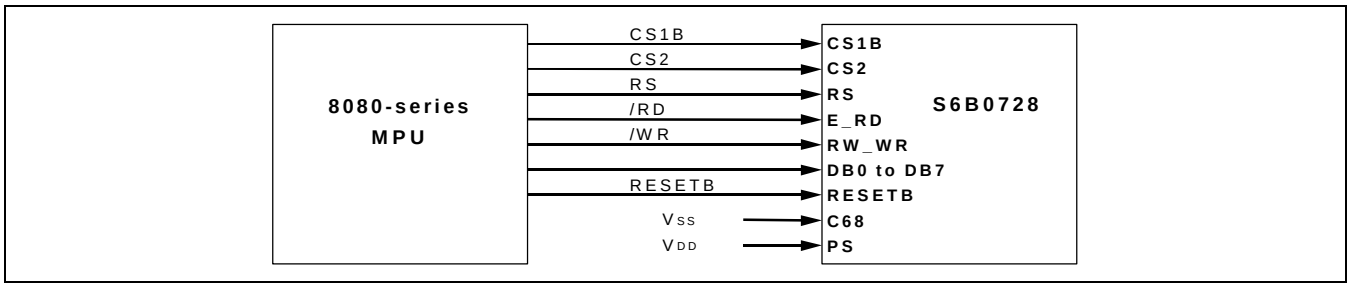


Figure 39. In Case of Interfacing with 8080-series (PS = “H”, C68 = “L”)

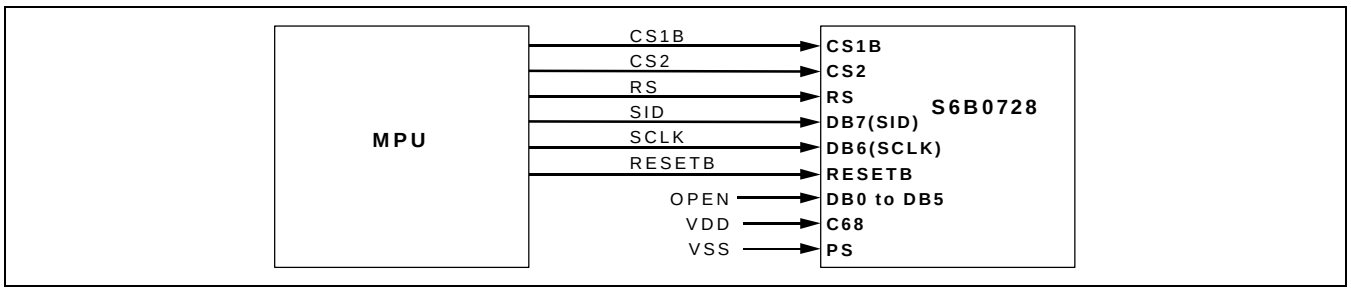


Figure 40. In Case of 4-Pin SPI Interface (PS = “L”, C68 = “H”)

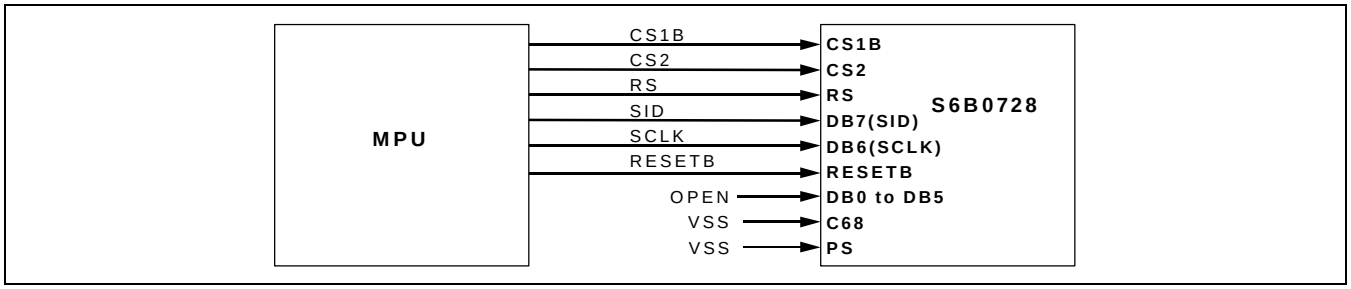


Figure 41. In Case of 3-Pin SPI Interface (PS = “L”, C68 = “L”)

CONNECTIONS BETWEEN S6B0728 AND LCD PANEL

(1/128 Duty configurations)

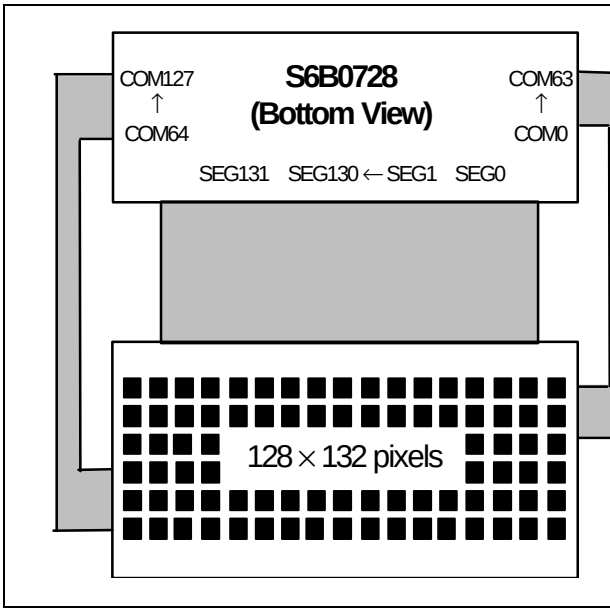


Figure 42. SHL = 0, ADC = 0

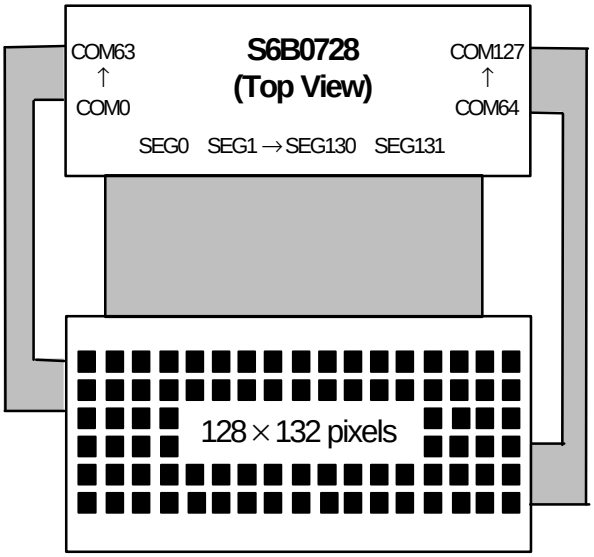


Figure 43. SHL = 0, ADC = 1

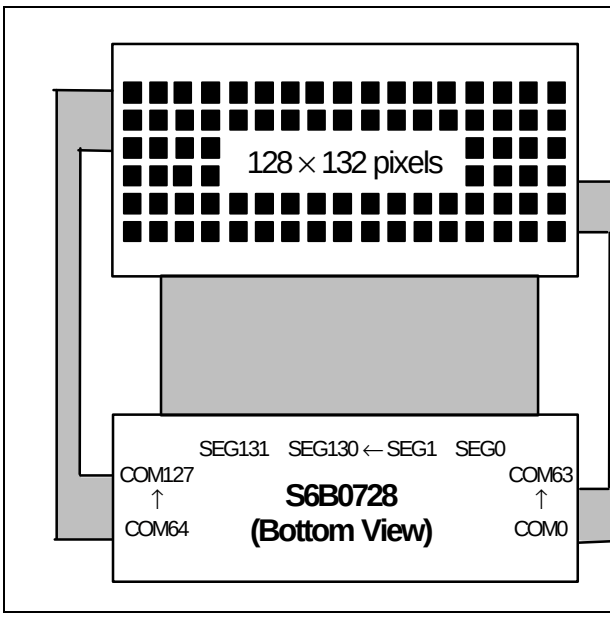


Figure 44. SHL = 1, ADC = 0

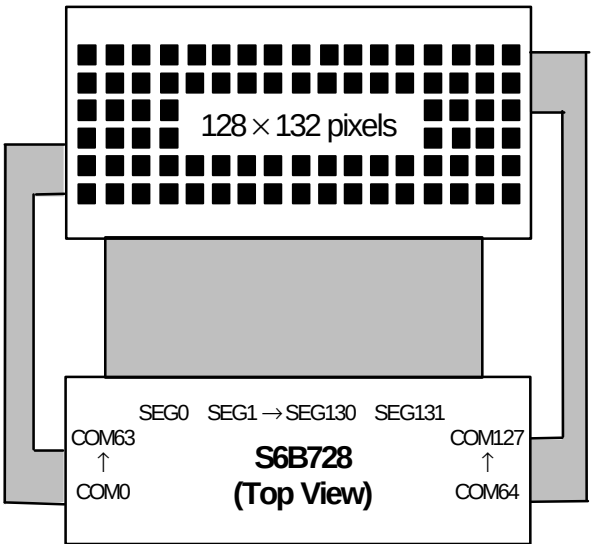


Figure 45. SHL = 1, ADC = 1