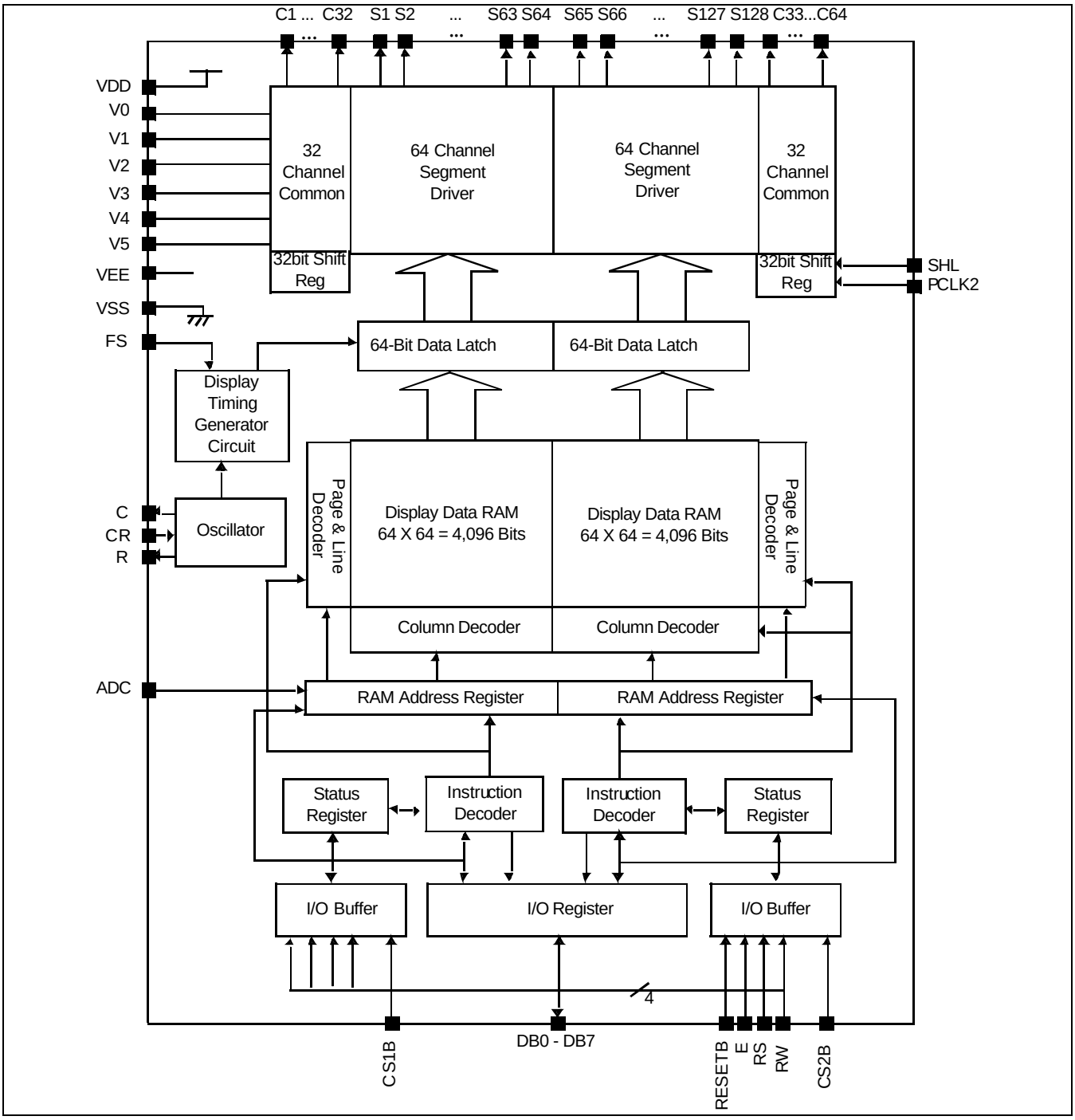
INTRODUCTION

S6B0708 is a single-chip LCD driver IC for liquid crystal dot-matrix graphic display systems. It incorporates 192 driver circuit for 64 common and 128 segment and 64 x 128-bit bit-map RAM. It is capable of interfacing with the microprocessor, accepting 8-bit parallel display data directly from it, and storing data in an one chip display data RAM. And it generates internal signals for using LCD driving independent of microprocessor clock.

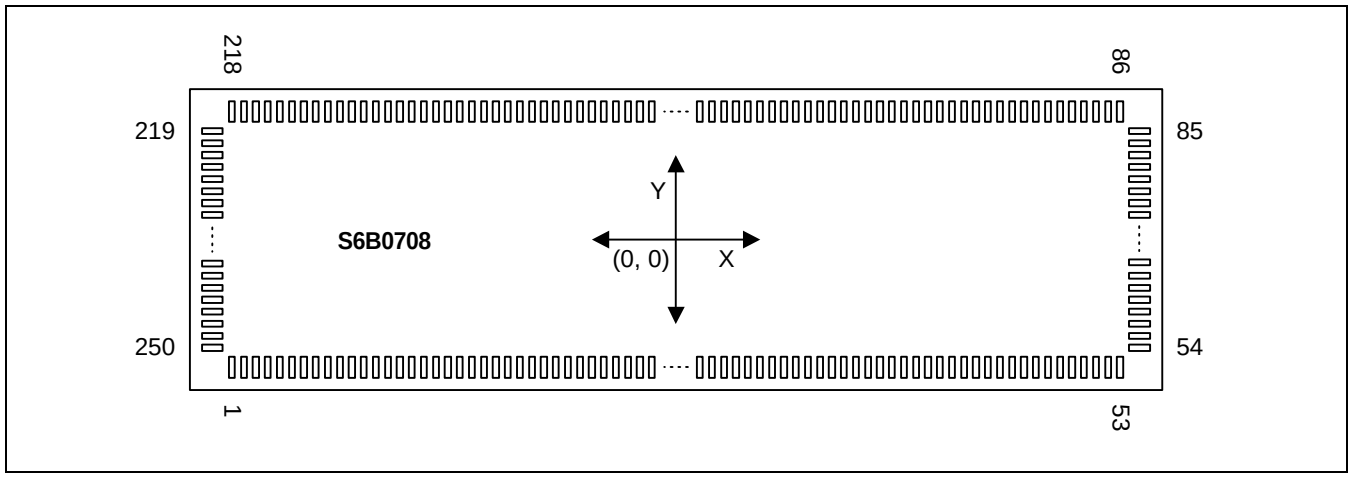
FEATURES

- 64-channel common & 128-channel segment driver for dot matrix LCD
- On-chip display data RAM: 64 × 128 = 8192bits
- Display data is stored in display data RAM from MPU
  - RAM bit data: ON(1), OFF(0)
- Internal timing generator circuit for dynamic display
- 8-bit parallel bi-directional data bus
- Applicable LCD duty: 1/64
- Power supply voltages: Power supply voltage range: 4.5 - 5.5V (VDD)
- LCD driving voltage range: 8.0 - 17.0V (VLCD = VDD-VEE)
- Wide operating temperature range: Ta = -30°C - 85°C
- High voltage CMOS process
- Gold bumped chip available

BLOCK DIAGRAM



PAD CONFIGURATION



Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	12590	3630	µm
Pad pitch	-	90 (min.)		
Bumped pad size	1 - 53	56	140	
	54 - 85	140	56	
	86 - 218	56	140	
	219 - 250	140	56	
Bumped pad height	All Pad	17 (typ.)		

PAD CENTER COORDINATES

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
1	Dummy	-6115	-1600	35	CS2B	1343	-1600	69	C16	6115	-36.5
2	Dummy	-6025	-1600	36	C	1563	-1600	70	C17	6115	53.5
3	Dummy	-5935	-1600	37	CR	1783	-1600	71	C18	6115	143.5
4	VEE	-5477	-1600	38	R	2003	-1600	72	C19	6115	233.5
5	VEE	-5257	-1600	39	DB0	2175	-1600	73	C20	6115	323.5
6	VEE	-5037	-1600	40	DB1	2467	-1600	74	C21	6115	413.5
7	V5	-4817	-1600	41	DB2	2759	-1600	75	C22	6115	503.5
8	V5	-4597	-1600	42	DB3	3051	-1600	76	C23	6115	593.5
9	V5	-4377	-1600	43	DB4	3343	-1600	77	C24	6115	683.5
10	V4	-4157	-1600	44	DB5	3635	-1600	78	C25	6115	773.5
11	V4	-3937	-1600	45	DB6	3927	-1600	79	C26	6115	863.5
12	V4	-3717	-1600	46	DB7	4219	-1600	80	C27	6115	953.5
13	V3	-3497	-1600	47	RS	4559	-1600	81	C28	6115	1043.5
14	V3	-3277	-1600	48	RW	4779	-1600	82	C29	6115	1133.5
15	V3	-3057	-1600	49	E	4999	-1600	83	C30	6115	1223.5
16	V2	-2837	-1600	50	CS1B	5219	-1600	84	C31	6115	1313.5
17	V2	-2617	-1600	51	RESETB	5439	-1600	85	C32	6115	1403.5
18	V2	-2397	-1600	52	Dummy	6025	-1600	86	Dummy	6115	1635
19	V1	-2177	-1600	53	Dummy	6115	-1600	87	Dummy	6025	1635
20	V1	-1957	-1600	54	C1	6115	-1386.5	88	S1	5715	1635
21	V1	-1737	-1600	55	C2	6115	-1296.5	89	S2	5625	1635
22	V0	-1517	-1600	56	C3	6115	-1206.5	90	S3	5535	1635
23	V0	-1297	-1600	57	C4	6115	-1116.5	91	S4	5445	1635
24	V0	-1077	-1600	58	C5	6115	-1026.5	92	S5	5355	1635
25	VDD	-857	-1600	59	C6	6115	-936.5	93	S6	5265	1635
26	VDD	-637	-1600	60	C7	6115	-846.5	94	S7	5175	1635
27	VDD	-417	-1600	61	C8	6115	-756.5	95	S8	5085	1635
28	VSS	-197	-1600	62	C9	6115	-666.5	96	S9	4995	1635
29	VSS	23	-1600	63	C10	6115	-576.5	97	S10	4905	1635
30	VSS	243	-1600	64	C11	6115	-486.5	98	S11	4815	1635
31	PCLK2	463	-1600	65	C12	6115	-396.5	99	S12	4725	1635
32	FS	683	-1600	66	C13	6115	-306.5	100	S13	4635	1635
33	SHL	903	-1600	67	C14	6115	-216.5				
34	ADC	1123	-1600	68	C15	6115	-126.5				

Table 1. Pad Center Coordinates (Continued)

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
101	S14	4545	1635	135	S48	1485	1635	169	S82	-1575	1635
102	S15	4455	1635	136	S49	1395	1635	170	S83	-1665	1635
103	S16	4365	1635	137	S50	1305	1635	171	S84	-1755	1635
104	S17	4275	1635	138	S51	1215	1635	172	S85	-1845	1635
105	S18	4185	1635	139	S52	1125	1635	173	S86	-1935	1635
106	S19	4095	1635	140	S53	1035	1635	174	S87	-2025	1635
107	S20	4005	1635	141	S54	945	1635	175	S88	-2115	1635
108	S21	3915	1635	142	S55	855	1635	176	S89	-2205	1635
109	S22	3825	1635	143	S56	765	1635	177	S90	-2295	1635
110	S23	3735	1635	144	S57	675	1635	178	S91	-2385	1635
111	S24	3645	1635	145	S58	585	1635	179	S92	-2475	1635
112	S25	3555	1635	146	S59	495	1635	180	S93	-2565	1635
113	S26	3465	1635	147	S60	405	1635	181	S94	-2655	1635
114	S27	3375	1635	148	S61	315	1635	182	S95	-2745	1635
115	S28	3285	1635	149	S62	225	1635	183	S96	-2835	1635
116	S29	3195	1635	150	S63	135	1635	184	S97	-2925	1635
117	S30	3105	1635	151	S64	45	1635	185	S98	-3015	1635
118	S31	3015	1635	152	S65	-45	1635	186	S99	-3105	1635
119	S32	2925	1635	153	S66	-135	1635	187	S100	-3195	1635
120	S33	2835	1635	154	S67	-225	1635	188	S101	-3285	1635
121	S34	2745	1635	155	S68	-315	1635	189	S102	-3375	1635
122	S35	2655	1635	156	S69	-405	1635	190	S103	-3465	1635
123	S36	2565	1635	157	S70	-495	1635	191	S104	-3555	1635
124	S37	2475	1635	158	S71	-585	1635	192	S105	-3645	1635
125	S38	2385	1635	159	S72	-675	1635	193	S106	-3735	1635
126	S39	2295	1635	160	S73	-765	1635	194	S107	-3825	1635
127	S40	2205	1635	161	S74	-855	1635	195	S108	-3915	1635
128	S41	2115	1635	162	S75	-945	1635	196	S109	-4005	1635
129	S42	2025	1635	163	S76	-1035	1635	197	S110	-4095	1635
130	S43	1935	1635	164	S77	-1125	1635	198	S111	-4185	1635
131	S44	1845	1635	165	S78	-1215	1635	199	S112	-4275	1635
132	S45	1755	1635	166	S79	-1305	1635	200	S113	-4365	1635
133	S46	1665	1635	167	S80	-1395	1635				
134	S47	1575	1635	168	S81	-1485	1635				

Table 1. Pad Center Coordinates (Continued)

Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate		Pad No.	Pad Name	Coordinate	
		X	Y			X	Y			X	Y
201	S114	-4455	1635	235	C48	-6115	-36.5				
202	S115	-4545	1635	236	C47	-6115	-126.5				
203	S116	-4635	1635	237	C46	-6115	-216.5				
204	S117	-4725	1635	238	C45	-6115	-306.5				
205	S118	-4815	1635	239	C44	-6115	-396.5				
206	S119	-4905	1635	240	C43	-6115	-486.5				
207	S120	-4995	1635	241	C42	-6115	-576.5				
208	S121	-5085	1635	242	C41	-6115	-666.5				
209	S122	-5175	1635	243	C40	-6115	-756.5				
210	S123	-5265	1635	244	C39	-6115	-846.5				
211	S124	-5355	1635	245	C38	-6115	-936.5				
212	S125	-5445	1635	246	C37	-6115	-1026.5				
213	S126	-5535	1635	247	C36	-6115	-1116.5				
214	S127	-5625	1635	248	C35	-6115	-1206.5				
215	S128	-5715	1635	249	C34	-6115	-1296.5				
216	Dummy	-5935	1635	250	C33	-6115	-1386.5				
217	Dummy	-6025	1635								
218	Dummy	-6115	1635								
219	C64	-6115	1403.5								
220	C63	-6115	1313.5								
221	C62	-6115	1223.5								
222	C61	-6115	1133.5								
223	C60	-6115	1043.5								
224	C59	-6115	953.5								
225	C58	-6115	863.5								
226	C57	-6115	773.5								
227	C56	-6115	683.5								
228	C55	-6115	593.5								
229	C54	-6115	503.5								
230	C53	-6115	413.5								
231	C52	-6115	323.5								
232	C51	-6115	233.5								
233	C50	-6115	143.5								
234	C49	-6115	53.5								

PAD DESCRIPTION

POWER SUPPLY

Name	I/O Type	Description
VDD	Supply	Power supply. connect to MPU power supply pin VCC
VSS	Supply	Ground
VEE	Supply	For LCD driver circuit
V0, V1 V2, V3 V4, V5	Supply	LCD driver supply voltages The voltages must satisfy the following relationship VDD ≥ V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5 ≥ VEE

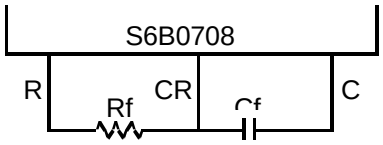
OSCILLATOR

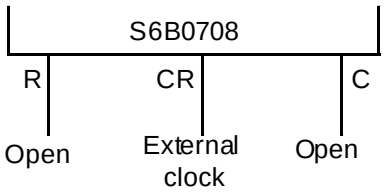
<table>
<tr><th>Name</th><th>I/O Type</th><th>Description</th></tr>
<tr><td>C

CR

R</td><td>O

I

O</td><td>RC oscillator
- Internal clock


- External clock

</td></tr>
<tr><td>FS</td><td>I</td><td>Frequency selection
When the frame frequency is 70Hz, the oscillation frequency should be as the following table.
<table>
<tr><td>FS</td><td>Oscillation Frequency</td></tr>
<tr><td>H</td><td>Fosc = 430kHz</td></tr>
<tr><td>L</td><td>Fosc = 215kHz</td></tr>
</table></td></tr>
</table>

MICROPROCESSOR INTERFACE

<table>
<tr><th>Name</th><th>I/O Type</th><th>Description</th></tr>
<tr><td>CS1B</td><td>I</td><td>First chip(S1 ~ S64) select input.
Data input/output is enabled via E, RS, RW, and DB[0:7]when CS1B = Low.</td></tr>
<tr><td>CS2B</td><td>I</td><td>Second chip(S65 ~ S128) select input.
Data input/output is enabled via E, RS, RW, and DB[0:7] when CS2B = Low.</td></tr>
<tr><td>RS</td><td>I</td><td>Register selection
<table>
<tr><th>RS</th><th>Description</th></tr>
<tr><td>H</td><td>The data in DB[7:0] is display data.</td></tr>
<tr><td>L</td><td>The data in DB[7:0] is control data.</td></tr>
</table></td></tr>
<tr><td>RW</td><td>I</td><td>Read or write
<table>
<tr><th>RW</th><th>Description</th></tr>
<tr><td>H</td><td>Data appears at DB[7:0] when E = high.</td></tr>
<tr><td>L</td><td>Display data DB[7:0] can be written at falling edge of E</td></tr>
</table></td></tr>
<tr><td>E</td><td></td><td>Enable signal.
<table>
<tr><th>E</th><th>Description</th></tr>
<tr><td>H</td><td>Read data in DB[7:0] appears while E = high.</td></tr>
<tr><td>L</td><td>Display data DB[7:0] is latched at falling edge of E.</td></tr>
</table></td></tr>
<tr><td>DB0 - DB7</td><td>I/O</td><td>Data bus [0 - 7]
Bi-directional data bus</td></tr>
</table>

RESET

Name	I/O Type	Description
RESETB	I	Reset input Chip is initialized when RESETB is low

LCD DRIVER OUTPUTS

Name	I/O Type	Description
C1 - C64	O	LCD driver common output
S1 - S128	O	LCD driver segment output
PCLK2	I	Phase of internal shift clock (CLK2) PCLK2 | Phase of Internal Shift Clock (CLK2) H | Data shift at the rising edge of CLK2 L | Data shift at the falling edge of CLK2
ADC	I	Address control signal of Y address counter. ADC | Segment Output Direction H | S1 → S2 ..... S63 → S65 → S66 ..... S127 → S128 L | S64 → S63 ..... S2 → S1 → S128 → S127..... S66 → S65
SHL	I	Selection of data shift direction SHL | Data Shift Direction H | C1 → C2 → C3 ..... C62 → C63 → C64 L | C64 → C63 → C62 ..... C3 → C2 → C1

FUNCTIONAL DESCRIPTION

CHIP SELECT INPUT

The S6B0708 has two chip select pins, CS1B and CS2B. It can interface with a microprocessor when these pins (CS1B or CS2B) are low. When both of these pins are set to high, DB0 to DB7 are at high impedance and RS, RW, and E inputs are disabled. CS1B pin controls the display status of S1 to S64, and CS2B does that of S65 to S128. When CS1B and CS2B are low at the same time, it is impossible to execute read operation. Therefore one of CS1B or CS2B should be set to low ((CS1B = H & CS2B = L) or (CS1B = L & CS2B = H)) in read operation. The RESETB signal is entered independent of the status of chip select.

Table 2. Relationship Between Chip Select Pins and Read/Write Operation

CS1B	CS2B	Read Operation		Write Operation	
		CS1	CS2	CS1	CS2
H	H	X	X	X	X
L	H	O	X	O	X
H	L	X	O	X	O
L	L	-	-	O	O

(-: Not recommended, O: Operation, X: No operation)

MICROPROCESSOR INTERFACE

S6B0708 transfers 8-bit parallel in either direction between the controlling microprocessor and the S6B0708 through the 8-bit I/O buffer (DB0 to DB7). RS, RW and E identify the type of parallel data transfer to be made as shown below in Table 3.

Table 3. Microprocessor Interface

RS	RW	Description
H	H	Read display data
H	L	Write display data
L	H	Status read
L	L	Write to internal register (instruction)

BUSY FLAG

Busy flag indicates whether S6B0708 is operating or not. When it is high, S6B0708 is in internal operation. When it is low, S6B0708 can accept the data or instruction. DB7 indicates busy flag of the S6B0708.

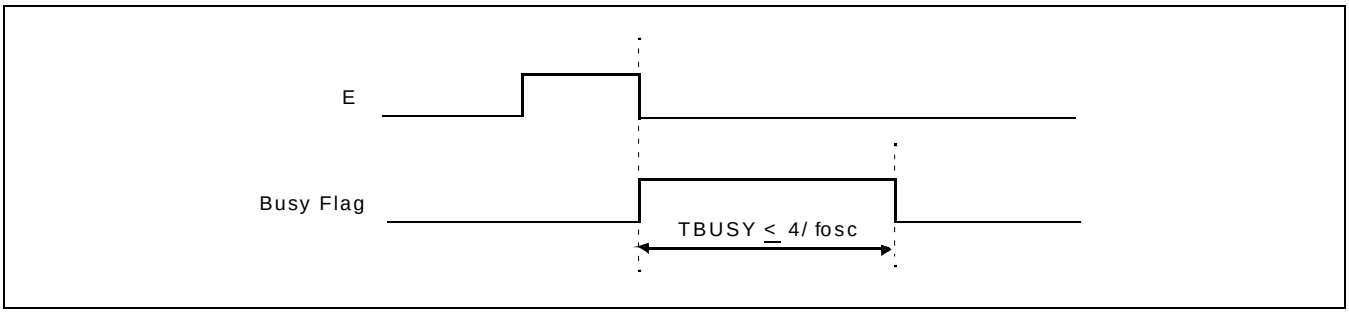


Figure 1. Busy Timing

DISPLAY TIMING GENERATOR CIRCUIT

This section explains how the timing generation circuit operates.

- Signal generation to display start line counter and display data latch circuit.
- The display clock (CLK2) generates a clock to the line counter. The display start line address of the display RAM is synchronized with the display clock. 128-bit display data is latched by the display data latch circuit in synchronization with the display clock and output to the segment LCD drive output pin.
- LCD AC signal (M) generation.

DISPLAY DATA RAM (DDRAM)

The display data RAM stores pixel data for the LCD. It is a 128-column x 64-row addressable array as shown in Table 4. The 64 rows are divided into 8 pages of 8 lines. Data is read from or written to the 8 lines of each page directly through DB0 to DB7. The microprocessor reads data from and writes data to RAM through the I/O buffer. Since the LCD controller operates independently, data can be written to RAM at the same time as the data is being displayed, without causing a LCD flicker.

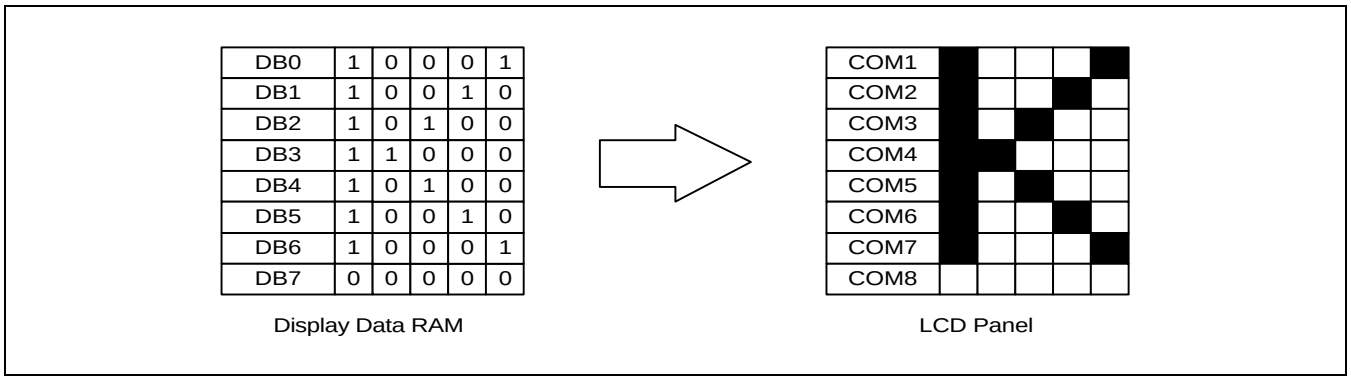


Figure 2. RAM to LCD Panel Data Transfer

Table 4. Display Data RAM

Page Address	Line Address	Segment Output (S1-S64)					Data Bus	Segment Output (S6-S128)					Line Address	Page Address
		S1	S2	···	S63	S64		S65	S66		S127	S128		
000	00 01 02 03 04 05 06 07						DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7						00 01 02 03 04 05 06 07	000
001	08 09 10 11 12 13 14 15						DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7						08 09 10 11 12 13 14 15	001
010	16 17 18 19 20 21 22 23						DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7						16 17 18 19 20 21 22 23	010
011	24 25 26 27 28 29 30 31						DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7						24 25 26 27 28 29 30 31	011
100	32 33 34 35 36 37 38 39						DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7						32 33 34 35 36 37 38 39	100

Table 4. Display Data RAM (Continued)

Page Address	Line Address	Segment Output (S1-S64)					Data Bus	Segment Output (S6-S128)					Line Address	Page Address
		S1	S2	···	S63	S64	DB0	S65	S66		S127	S128		
101	40						DB0						40	101
	41						DB1						41	
	42						DB2						42	
	43						DB3						43	
	44						DB4						44	
	45						DB5						45	
	46						DB6						46	
	47						DB7						47	
110	48						DB0						48	110
	49						DB1						49	
	50						DB2						50	
	51						DB3						51	
	52						DB4						52	
	53						DB5						53	
	54						DB6						54	
	55						DB7						55	
111	56						DB0						56	111
	57						DB1						57	
	58						DB2						58	
	59						DB3						59	
	60						DB4						60	
	61						DB5						61	
	62						DB6						62	
	63						DB7						63	
ADC	1	0	1		62	63		0	1		62	63	1	ADC
	0	63	62		1	0		63	62		1	0	0	
		Column Address						Column Address						
Chip Select (CS1B)								Chip Select (CS2B)						

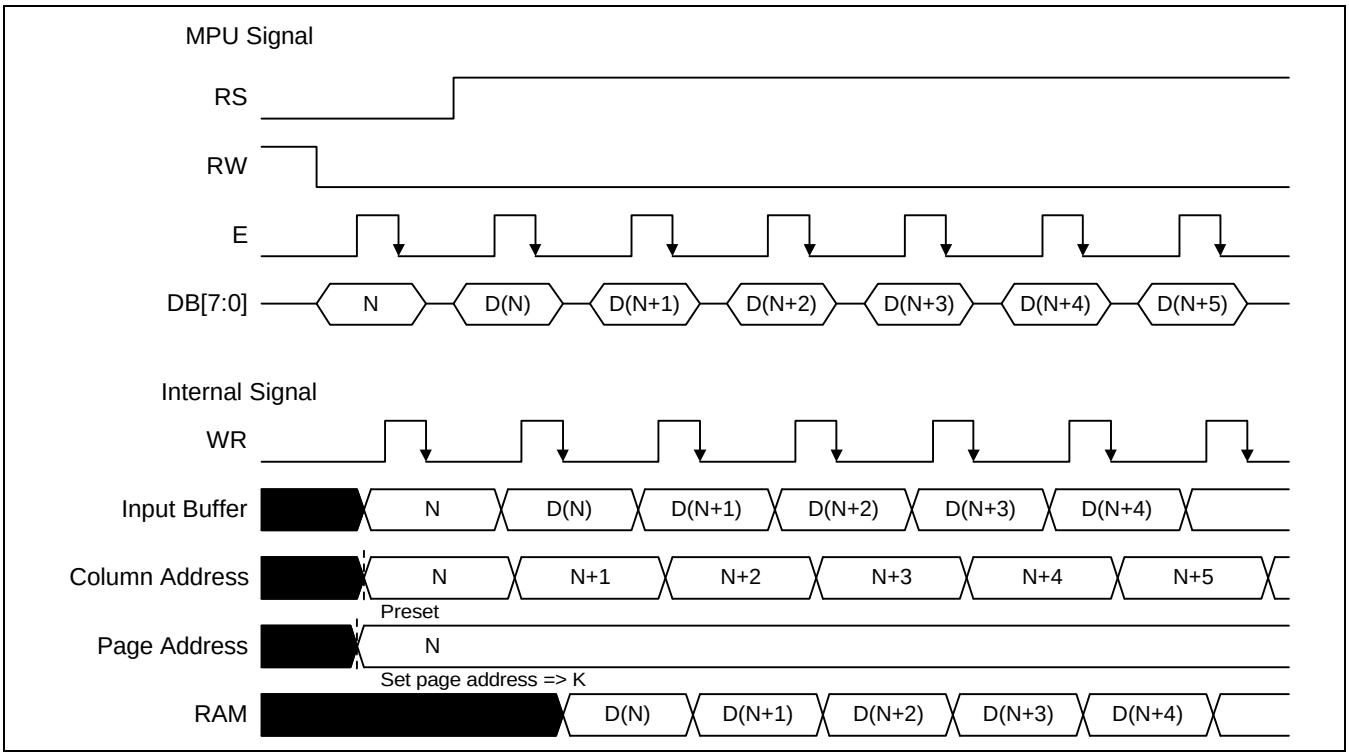


Figure 3. Write Timing

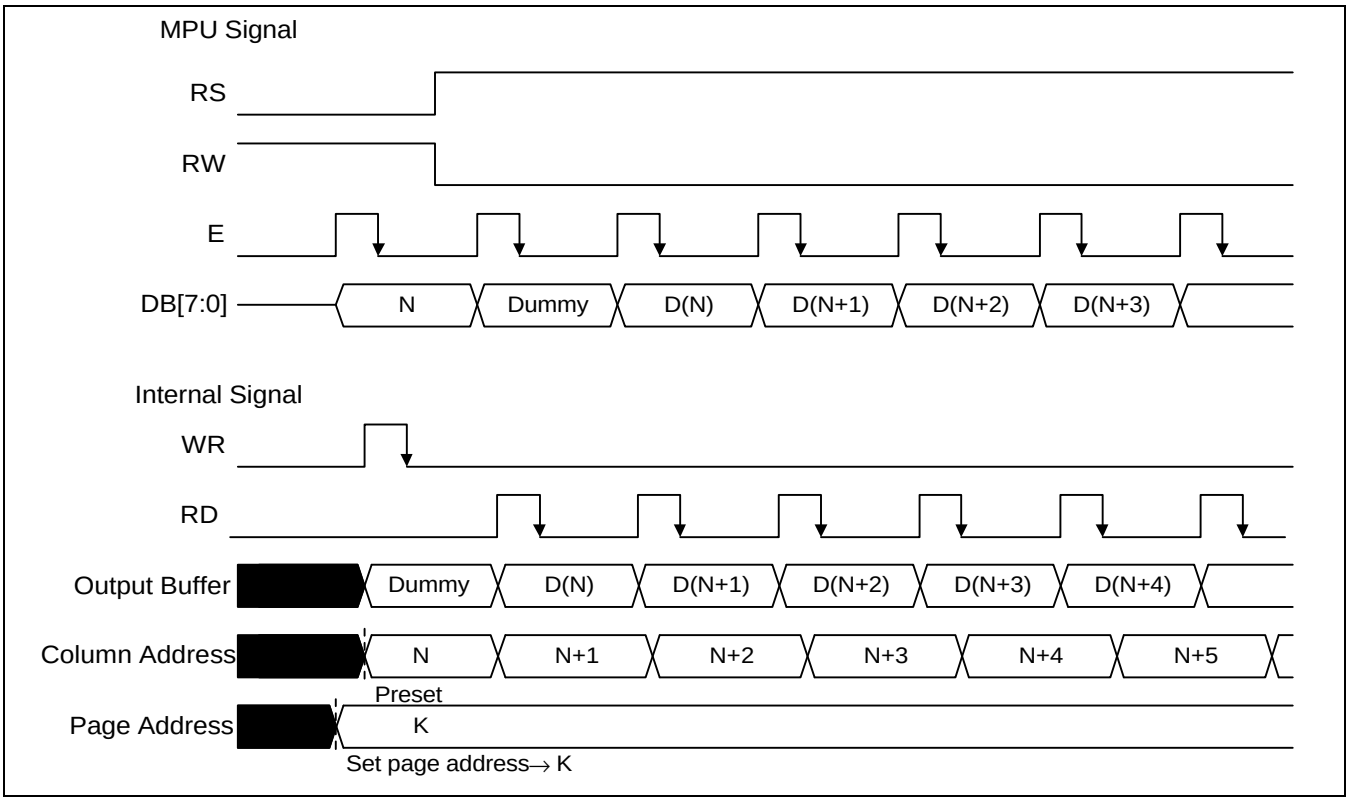


Figure 4. Read Timing

DATA TRANSFER

To match the timing of the display data RAM and registering to that of the controlling microprocessor, S6B0708 uses an internal data bus and bus buffer. When the microprocessor reads the contents of display data RAM, the data for the initial read cycle is first stored in the bus buffer (dummy read cycle). On the next read cycle, the data is read from the bus buffer onto the microprocessor bus. At the same time, the next block of data is transferred from RAM to the bus buffer. Otherwise, when the microprocessor write data to display data RAM, the data is written to RAM after the falling edge of "E". Therefore, it is necessary to check busy flag to write or read the next data. (refer to Figure 3, 4)

PAGE ADDRESS REGISTER

The 3-bit page address register provides the page address to display data RAM (refer to Table 4). The microprocessor issues set page address instruction to change the page and to access another page.

COLUMN ADDRESS COUNTER

The column address counter is a 6-bit pre-settable counter that provides column address to display data RAM (refer to Table 4). It is incremented by 1 automatically after execution of each read/write data instruction. The column address counter loops the values 0 to 127, and it is independent of page address register. The ADC pin is issued to change the relationship between RAM column address and display segment output.

DISPLAY START LINE REGISTER

The display start line register stores the line address of display data RAM that corresponds to the first (normally the top) line (COM1) of liquid crystal display (LCD) panel. When displaying contents in display data RAM on the LCD panel, 6-bit data (DB[5:0]) of the set display start line is latched in display start line register. latched data are transferred to the line address counter just before COM1 is high, pre-setting the line address counter. The line counter is then incremented on the display latch clock signal once for every display line. It is used for vertical scrolling of the liquid crystal display screen.

LCD DRIVER

LCD driver circuit has 192 outputs of 128 segment outputs, 64 common outputs for LCD driving. Each common output has a shift register. LCD driving output voltage is determined by the combination of display data and internal AC signal.

Display Data	Common Output	Segment Output
0	V1	V2
	V4	V3
1	V5	V0
	V0	V5
Display Off	-	V2 or V3

RESET CIRCUIT

Reset function can initialize system by setting RESETB terminal at low level. When RESETB becomes low, following procedure occurs.

- Display start line: 0 (first)
- Display on/off: Off

While RESETB is in low level, no instruction except status read can be accepted. Reset status appears at DB4. Refers to read status of "instruction description"

The conditions of power supply at initial power up are shown in table 5.

Table 5. Power supply initial conditions.

Item	Symbol	Min	Typ	Max	Unit
Reset time	tRESETB	1.0	-	-	s
Rise time	tr	-	-	200	ns

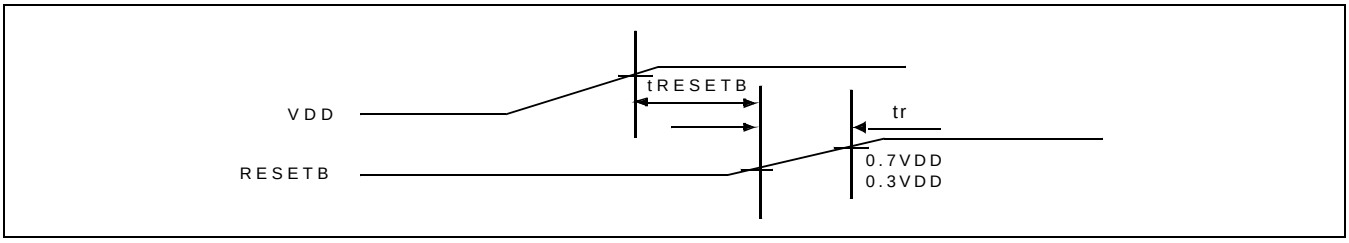


Figure 5. Reset timing

INSTRUCTION DESCRIPTION

Table 6. Instruction Table

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Read display data	1	1	Read Data								Reads data (DB[0:7]) from display data RAM to the data bus.
Write display data	1	0	Write Data								Writes data(DB[0:7]) into display data RAM. After writing instruction, column address is incremented by1 automatically.
Status read	0	1	busy	0	on/ off	reset	0	0	0	0	Reads status BUSY 0: Ready 1: In operation ON/OFF 0: Display ON 1: Display OFF RESET 0: Normal 1: Reset
Set column address	0	0	0	1	Column Address (0-63)						Sets the column address at the column address counter
Set display start line	0	0	1	1	Display Start Line (0-63)						Indicates the display data RAM displayed at the top of the screen.
Set page address	0	0	1	0	1	1	1	Page (0-7)			Sets the page address at the Page address register.
Display on/off	0	0	0	0	1	1	1	1	1	0/1	Controls the display on or off. Internal status and display RAM data is not affected. 0: OFF 1: ON

DETAILED INSTRUCTION DESCRIPTIONS

Read Display Data

Reads 8-bit data in the display data RAM area specified by column address and page address. As the column address is incremented by 1 automatically after each read operation, the microprocessor can continue to read data of multiple words.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read Data							

Write Display Data

Writes 8-bit data to the display data RAM
As the column address is incremented by 1 automatically after each write operation, the microprocessor can continue to write data of multiple words.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write Data							

Read Status

Indicates the internal status conditions of the device to the microprocessor.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	Busy	0	On/Off	RESET	0	0	0	0

Flag	Description
Busy	The device is busy due to internal operation or reset. Any instruction is rejected until BUSY goes low.
On/Off	Indicates whether the display is on or off. When low, the display is on. When high, the display is off. This is the opposite of Display ON/OFF instruction.
RESET	Indicates the initialization is in progress by RESETB signal. When low, the chip is in active. When high, the chip is being reset.

Set Page Address

Sets the page address of display RAM from the microprocessor into the page address register. Along with column address register, Page address register assigns the address of the display RAM to be written to or read from display data. Changing the address doesn't affect the display status.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	X2	X1	X0

X2	X1	X0	Page
0	0	0	0
0	0	1	1
:	:	:	:
1	1	1	7

Set Column Address

Sets the column address of display RAM from the microprocessor into the column address register. When the microprocessor reads or writes display data to or from display RAM, the address are automatically incremented.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	Y5	Y4	Y3	Y2	Y1	Y0

Y5	Y4	Y3	Y2	Y1	Y0	Column Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Set Display Start Line

Sets the line address of display RAM to determine the display start line. The display data on the specified line of the display RAM is displayed at the top row COM1 of LCD panel. It is followed by the higher number of lines in ascending order corresponding to the determined duty cycle. When this instruction changes the display start line address, the LCD panel can be scrolled.

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	Z5	Z4	Z3	Z2	Z1	Z0

Z5	Z4	Z3	Z2	Z1	Z0	Line Address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
:	:	:	:	:	:	:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Display ON / OFF

Turns the display ON or OFF

RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D0

D0 = 1: Display ON
D0 = 0: Display OFF

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Operating voltage	V_{DD}	-0.3 - +7.0	V	(1)
Supply voltage	V_{EE}	VDD-19.0 - VDD+0.3		(4)
Driver supply voltage	V_B	-0.3 - VDD+0.3		(1), (3)
	V_{LCD}	VEE-0.3 - VDD+0.3		(2)

NOTES:
1. Based on Vss = 0V
2. VLCD = VDD - VEE
3. Applies to SHL, FS, PCLK2, CR, RESETB, ADC, CS1B, CS2B, E, RW, RS and DB0 - DB7.
4. Voltage level VDD ≥ V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ V5 ≥ VEE

TEMPERATURE CHARACTERISTICS

Parameter	Symbol	Rating	Unit	Note
Operating temperature	Topr	-30 - +85	°C	
Storage temperature	Tstg	-55 - +125		

ELECTRICAL CHARACTERISTICS

DC Characteristics (VDD = 4.5 to 5.5V, Ta = -30 to +85°C)

Item		Symbol	Condition	Min	Typ	Max	Unit	Note
Operating voltage		V_{DD}	-	4.5	-	5.5	V	
Input high voltage		V_{IH1}	-	0.7VDD	-	VDD		(1)
		V_{IH2}	-	2.0	-	VDD		(2)
Input low voltage		V_{IL1}	-	0	-	0.3VDD		(1)
		V_{IL2}	-	0	-	0.8		(2)
Output high voltage		V_{OH}	IOH = -200uA	2.4	-	-		(3)
Output low voltage		V_{OL}	IOL = 1.6mA	-	-	0.4		
Input leakage current		I_{LKG}	VIN = VSS - VDD	-1.0	-	+1.0	µA	(4)
Tri-state leakage current		I_{TSL}	VIN = VSS - VDD	-5.0	-	+5.0		(5)
Driver input leakage current		I_{DLKG}	VIN = VEE - VDD	-10	-	+10		(6)
Operating current		I_{DD1}	During display	-	-	0.8	mA	(7)
		I_{DD2}	During access	-	-	1.0		(8)
On resistance	COM	R_{ONC}	ILOAD = ± 0.1mA	-	-	1.5	kΩ	(9)
	SEG	R_{ONS}		-	-	7.5		(10)
Oscillation frequency		fosc	Ta = 25°C, VDD = 5V Rf = 47kΩ ± 2% Cf = 20pF ± 5%	315	450	585	kHz	

NOTES:

1. FS, CR, ADC, SHL, PCLK2, RESETB
2. CS1B, CS2B, E, RW, RS, DB0 - DB7
3. DB0 - DB7
4. Excepted DB0 - DB7
5. DB0 - DB7 at high impedance
6. V0, V1, V2, V3, V4, V5
7. C = 20pF, R = 47kΩ, fose = 450kHz, DB0 - DB7 = VDD, output = No load
8. External clock = 430kHz, RAM access cycle = 1MHz
9. V0 = 5V, V1 = 3.2V, V2 = 1.4V, V3 = -8.4V, V4 = -10.2V, V5 = -12V, C1 - C64
10. V0 = 5V, V1 = 3.2V, V2 = 1.4V, V3 = -8.4V, V4 = -10.2V, V5 = -12V, S1 - S128

AC Characteristics (VDD = 4.5 to 5.5V, Ta = -30 to +85°C)

Mode	Item	Symbol	Min	Typ	Max	Unit
Write mode	E cycle time	t_{cyc}	1000	-	-	ns
(refer to figure 6)	E rise/fall time	t_r, t_f	-	-	25	
	E pulse width high	t_{PWH}	450	-	-	
	RW and RS setup time	t_{AS}	140	-	-	
	RW and RS hold time	t_{AH}	10	-	-	
	Data setup time	t_{DS}	200	-	-	
	Data hold time	t_{DH}	10	-	-	
Read mode	E cycle time	t_{cyc}	1000	-	-	ns
(refer to figure 7)	E rise/fall time	t_r, t_f	-	-	25	
	E pulse width high	t_{PWH}	450	-	-	
	RW and RS setup time	t_{AS}	140	-	-	
	RW and RS hold time	t_{AH}	10	-	-	
	Data setup time	t_{DS}		-	320	
	Data hold time	t_{DH}	20	-	-	

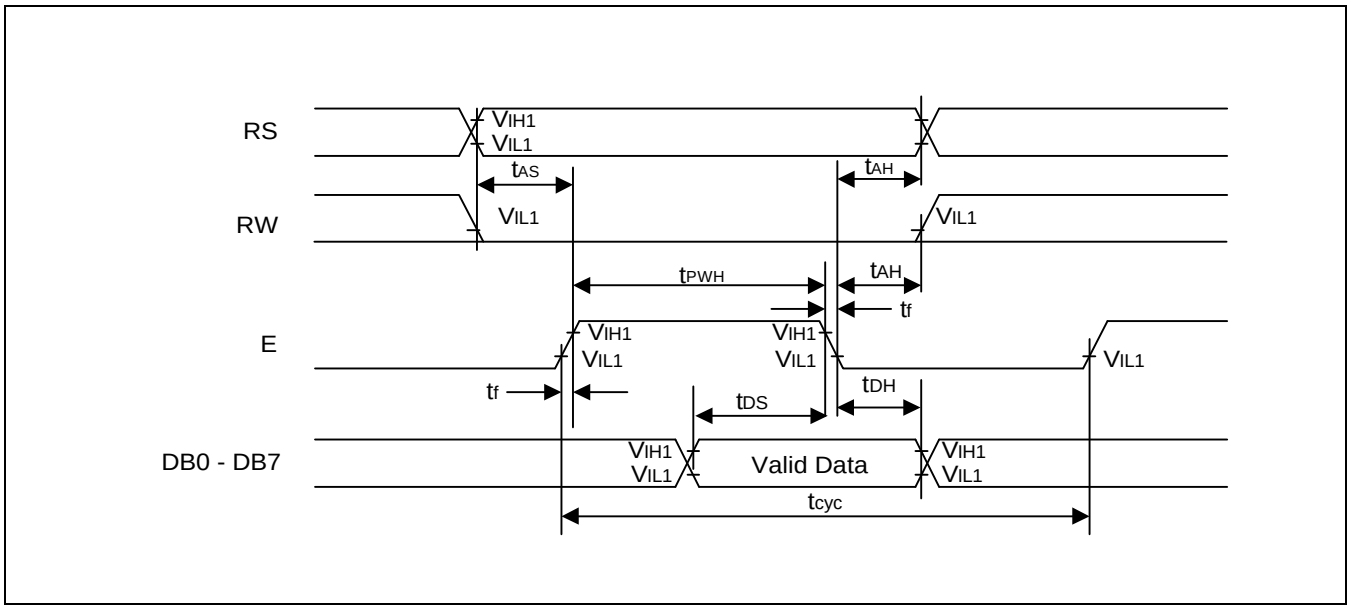


Figure 6. Write Mode Timing Diagram

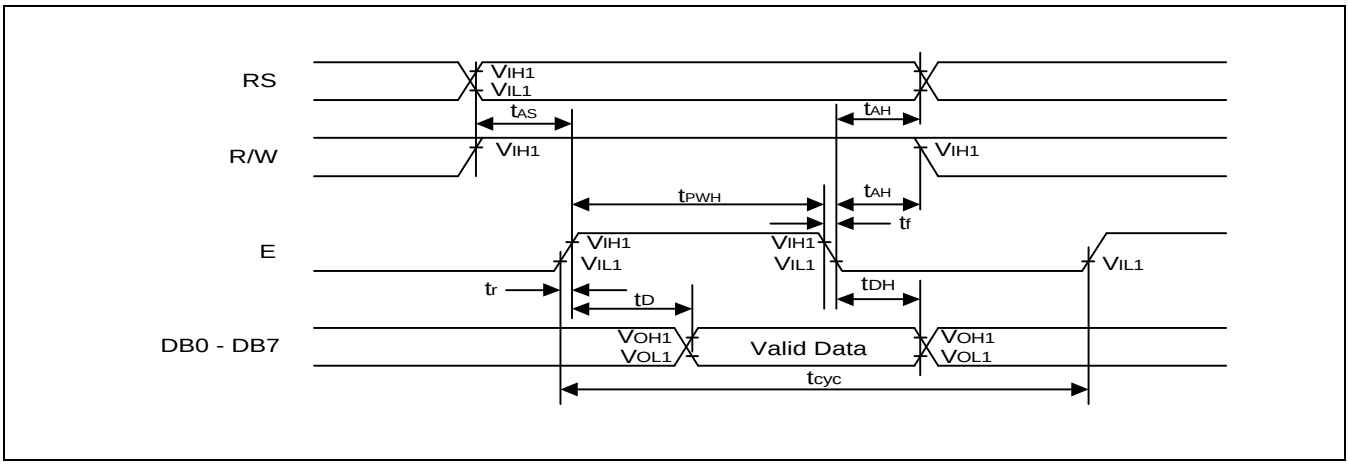
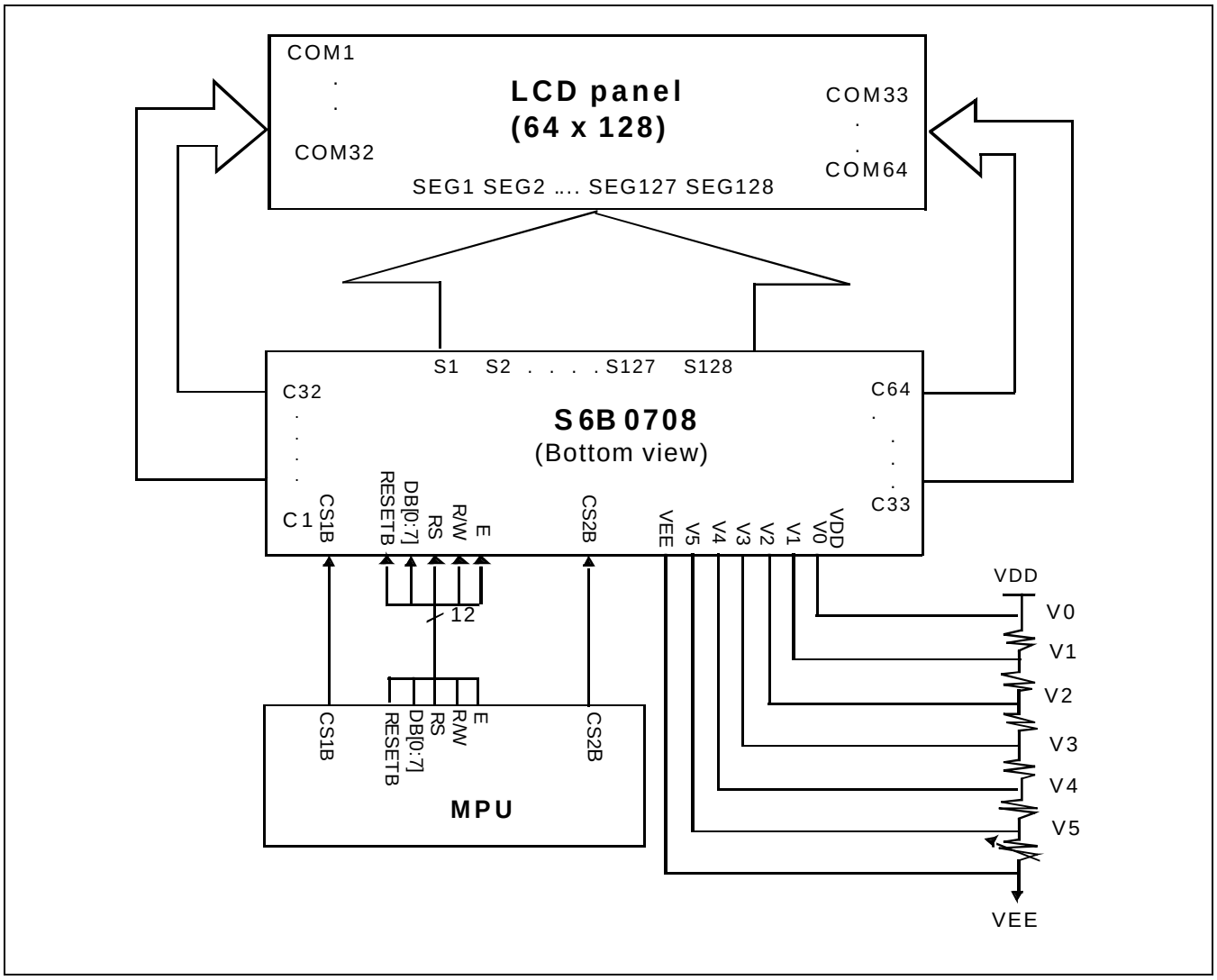
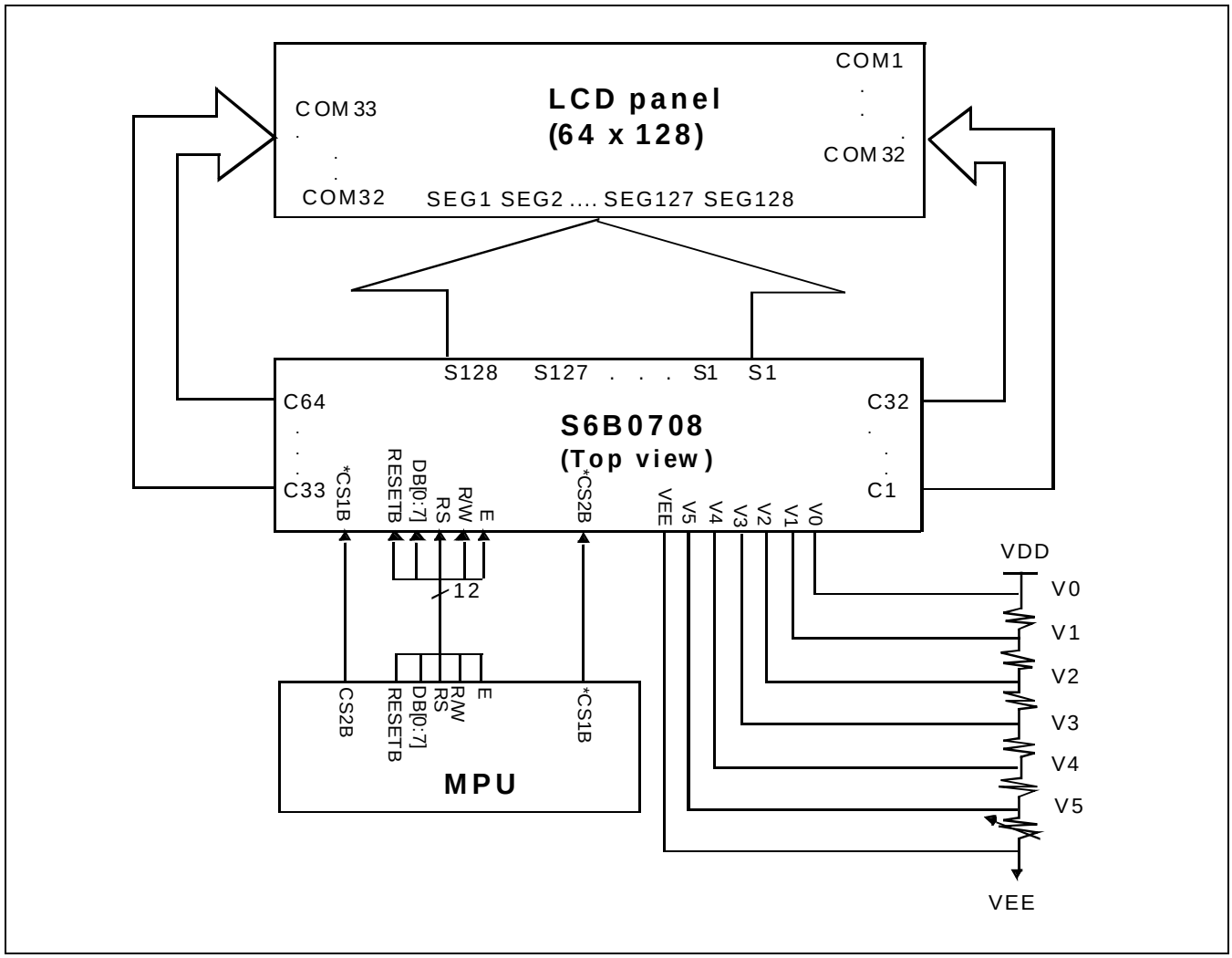


Figure 7. Read Mode Timing Diagram

APPLICATION DIAGRAM1 (ADC = H, SHL = H)



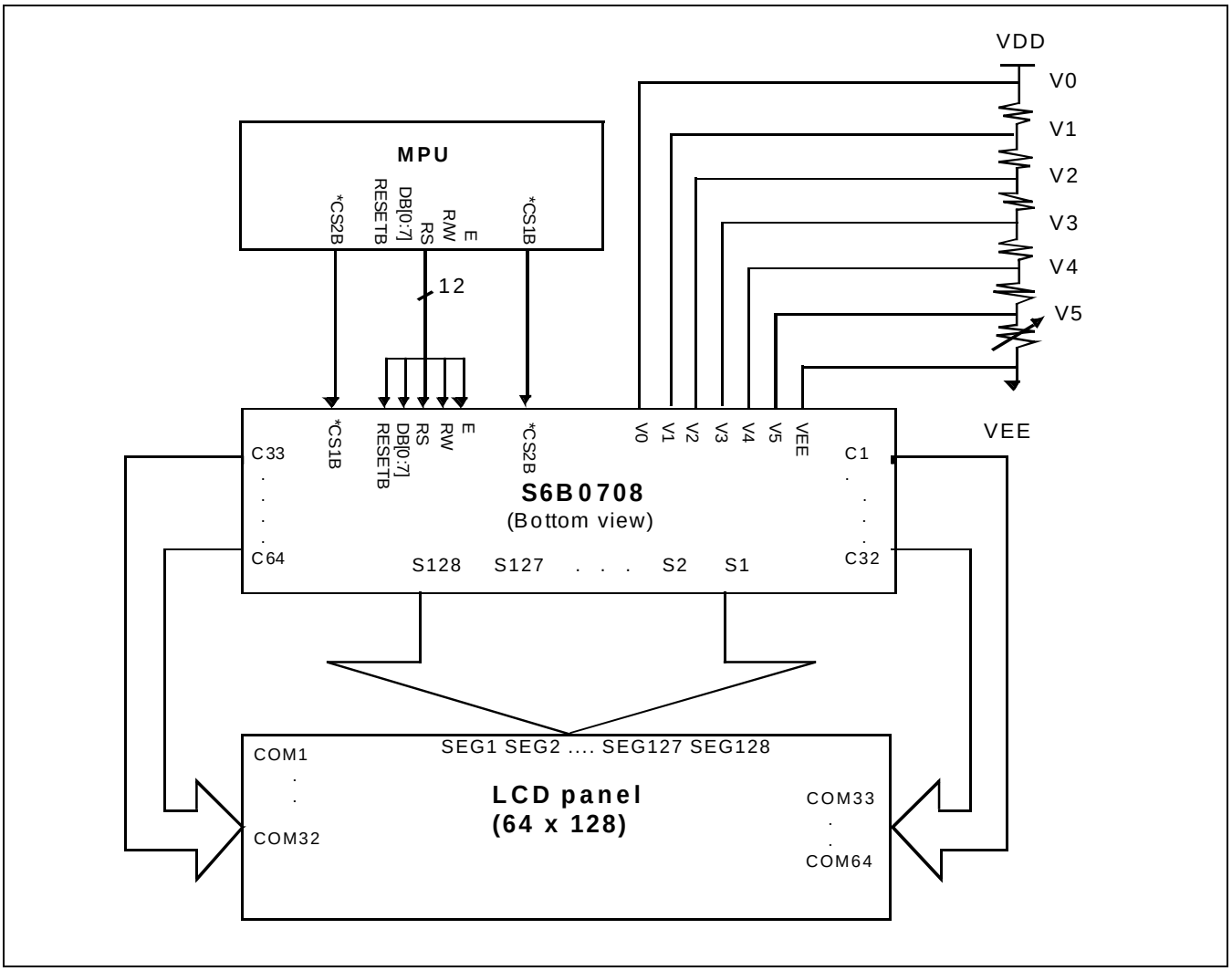
APPLICATION DIAGRAM 2 (ADC = H, SHL = H)



Note: When ADC=L, connects chip select pins (CS1B, CS2B) as follows.

- CS1B (MPU) -> CS2B (S6B0708)
- CS2B (MPU) -> CS1B (S6B0708)

APPLICATION DIAGRAM3 (ADC = H, SHL = H)



Note: When ADC=L, connects chip select pins (CS1B, CS2B) as follows.

- CS1B (MPU) -> CS2B (S6B0708)
- CS2B (MPU) -> CS1B (S6B0708)

APPLICATION DIAGRAM4 (ADC = H, SHL = H)

