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30-Volt Dichroic LCD Driver

S4520

Features

- ☐ High Voltage Outputs Capable of a 32-Volt Swing
- ☐ Drives Up to 38 Devices
- ☐ Cascadable
- ☐ On-Chip Oscillator
- ☐ Requires Only 4 Control Lines
- ☐ CMOS Construction For:
  - Wide Supply Range
  - Low Power Consumption
  - High Noise Immunity
  - Wide Temperature Range
- ☐ **Military Version (screened per Mil. Std. 883 method 5004 and tested per method 5010) will be available upon request.**

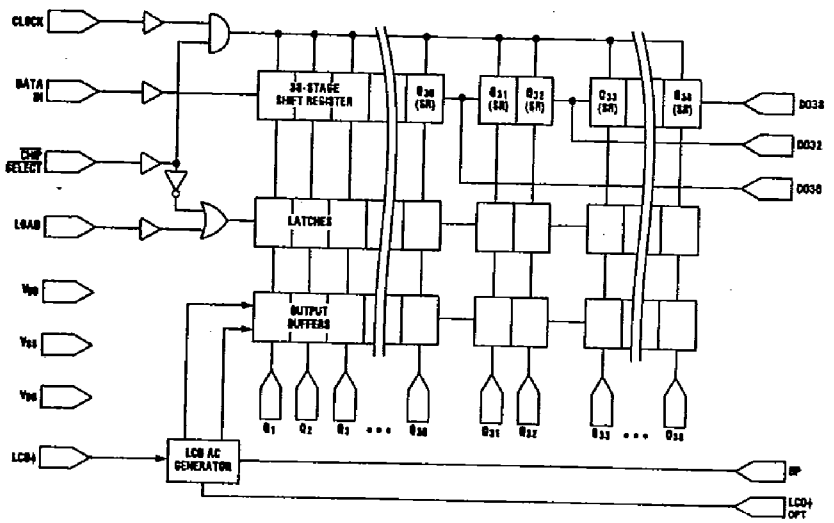
Applications

- ☐ Liquid Crystal Displays
- ☐ Flat Panel Displays
- ☐ Print Head Drives

General Description

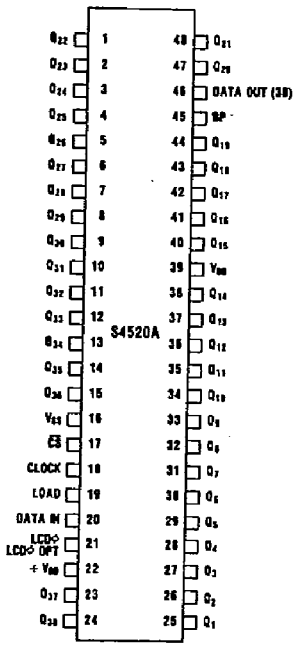
The S4520 is a CMOS/LSI circuit that drives high-voltage dichroic liquid crystal displays, usually under microprocessor control. The S4520 requires only four control inputs (CLOCK, DATA IN, LOAD and CHIP SELECT) due to its serial input construction. It can latch the data to be output, relieving the microprocessor from the task of generating the required waveforms, or it may be used to bring data directly to the drivers. The A.C. frequency of the backplane output can be generated by the internal oscillator or, the user has the option of supplying this signal from an external source. If the internal oscillator is used to generate the backplane signal, the frequency will be determined by an external resistor and capacitor. One S4520 circuit can drive 38 segments. Other packaging options can provide 30 or 32 segment drivers.

Block Diagram



Pin Configuration

(Other Packaging Options — Page 8)



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S4520

Absolute Maximum Ratings

V_{DD} ..... −0.3V to +17V
V_{BB} ..... V_{SS} + 0.3V to V_{DD} − 32V
Inputs (CLK, DATA IN, LOAD) ..... V_{SS} − 0.3V to V_{DD} + 0.3V
Inputs (LCDϕ) ..... V_{BB} − 0.3V to V_{DD} + 0.3V
Power Dissipation 250mW
Storage Temperature ..... −65°C to +125°C
Operating Temperature ..... −55°C to +85°C

Electrical Characteristics: $3V \leq V_{DD} \leq 16V$, $-55°C \leq T_A \leq +85°C$, unless otherwise noted

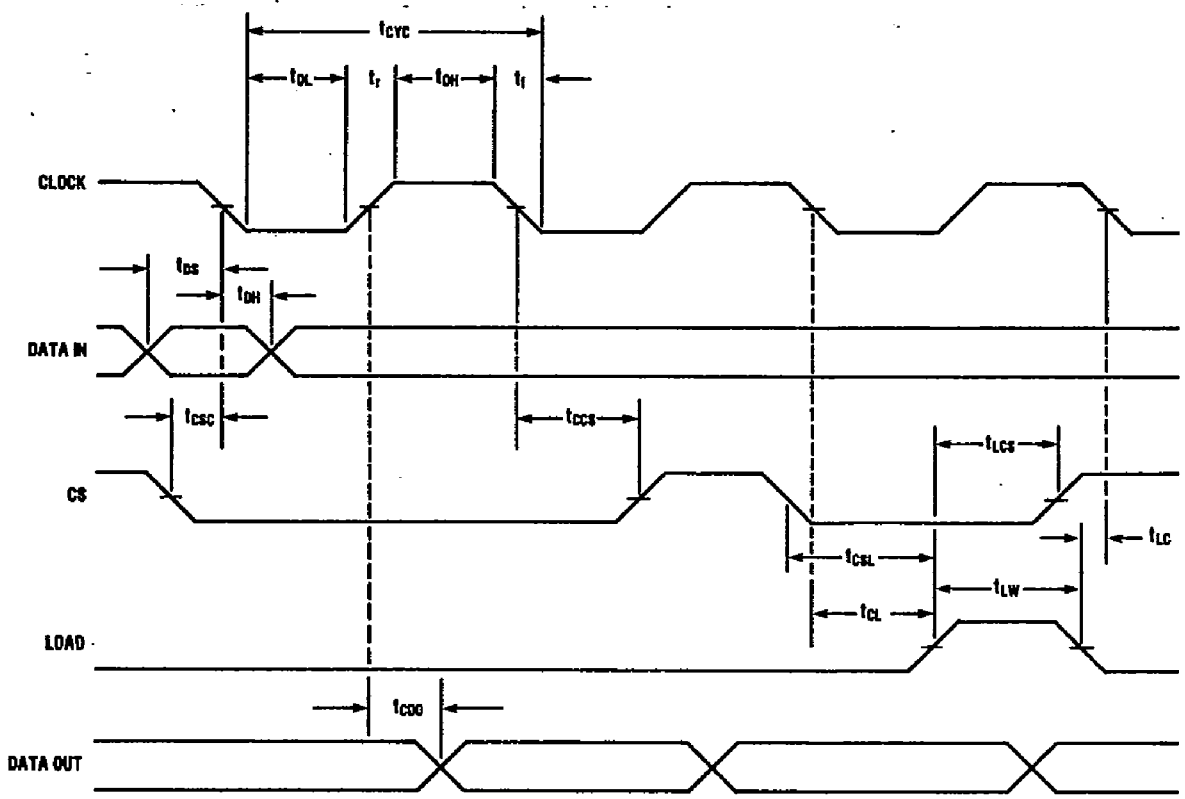
Symbol	Parameter	Min.	Max.	Units	Test Condition
	Power Supply				
V_{DD}	Logic Supply Voltage	3	16	V	
V_{BB}	Display Supply Voltage	$V_{DD}-32$	$V_{DD}-5$	V	$V_{BB} \leq V_{SS}$
I_{DD}	Supply Current (external oscillator) Supply Current (internal oscillator)		*200 *200 *750	μA μA μA	CMOS input levels. No loads. $V_{DD} \leq 5V$ $V_{DD} = 16V$; CMOS input levels. No loads.
I_{BB}	Display Driver Current		*−200	μA	$f_{BP} = 100Hz$. No loads.
	Inputs (CLK, DATA IN, LOAD, $\overline{CS}$)				
V_{IH}	Input High Level	$0.5V_{DD}$	V_{DD}	V	$V_{DD} \geq 5V$
V_{IL}	Input Low Level	V_{SS}	$0.2V_{DD}$	V	
I_L	Input Leakage Current		5	μA	
C_I	Input Capacitance		5	pF	
$V_{O_{AVG}}$	DC Bias (Average) Any Segment Output to Backplane		±25	mV	$f_{BP} \leq 100Hz$
V_{IH}	LCDϕ Input High Level	$0.9V_{DD}$	V_{DD}	V	Externally Driven
V_{IL}	LCDϕ Input Low Level	V_{BB}	$0.1V_{DD}$	V	Externally Driven
	Capacitance Loads (typical)				
$C_{L_{SEG}}$	Segment Output		1000	pF	$f_{BP} \leq 100Hz$
$C_{L_{BP}}$	Backplane Output		40000	pF	$f_{BP} \leq 100Hz$
R_{SEG}	Segment Output Impedance		10	KΩ	$I_L = 10\ \mu A$
R_{BP}	Backplane Output Impedance		312	Ω	$I_L = 10\ \mu A$
R_{DO}	Data Out Output Impedance		3	KΩ	$I_L = 10\ \mu A$

* Characteristics may vary

Timing Characteristics:

Symbol	Parameter	Min.	Max.	Units	V_{DD}
t_{CYC}	Cycle time (noncascaded)	1000		ns	3.0V
		500		ns	5.0V
		320		ns	≥7.5V
t_{CYC}	Cycle time (cascaded)	1300		ns	3.0V
		600		ns	5.0V
		350		ns	≥7.5V
t_{OL}, t_{OH}	Clock pulse width low/high	450		ns	3.0V
		220		ns	5.0V
		140		ns	≥7.5V
t_{OH}	Clock pulse width high (cascaded)	750		ns	3.0V
		320		ns	5.0V
		180		ns	≥7.5V
t_r, t_f	Clock rise, fall (Note 12)		1	μs	
t_{DS}	Data In setup	300		ns	3.0V
		150		ns	5.0V
		120		ns	≥7.5V
t_{CSC}	$\overline{CS}$ setup to Clock	200		ns	3.0V
		100		ns	5.0V
		50		ns	≥7.5V
t_{DH}	Data hold	10		ns	
t_{CCS}	$\overline{CS}$ hold	450		ns	3.0V
		220		ns	5.0V
		140		ns	≥7.5V
t_{CL}	Load pulse setup (Note 5)	500		ns	3.0V
		280		ns	5.0V
		180		ns	≥7.5V
t_{LCS}	$\overline{CS}$ hold (rising LOAD to rising $\overline{CS}$)	300		ns	3.0V
		200		ns	5.0V
		150		ns	≥7.5V
t_{LW}	Load pulse width (Note 5)	500		ns	3.0V
		220		ns	5.0V
		140		ns	≥7.5V
t_{LC}	Load pulse delay (Falling load to falling clock)	0		ns	
t_{CDO}	Data Out valid from Clock		550	ns	3.0V
			220	ns	5.0V
			110	ns	≥7.5V
t_{CSL}	$\overline{CS}$ setup to LOAD	0		ns	

Figure 1. Signal Timing Diagram



Logic Truth Table

DATA IN	CLOCK	CHIP SELECT	LOAD	Q_1(SR)	Q_N(SR)	BP	Q_N(DRIVER)
X	X	1	0	NC	NC	0	QN(L)
X	X	1	1	NC	NC	1	QN(L)
0	⌐	0	0	NC	NC	1	QN(L)
0	⌐	0	1	NC	NC	1	QN(L)
0	¬	0	0	0	QN—1→QN	1	QN(L)
0	¬	0	1	0	QN—1→QN	1	QN(SR)
1	⌐	0	0	NC	NC	1	QN(L)
1	⌐	0	1	NC	NC	1	QN(L)
1	¬	0	0	1	QN—1→QN	1	QN(L)
1	¬	0	1	1	QN—1→QN	1	QN(SR)

Notes: NC = No Change SR = Shift Register L = Latch

Operating Notes

1. The shift register loads and shifts on the falling edge of CLK. DATA OUT changes on the rising edge of CLK.
2. The buffer number corresponds to how many clock pulses have occurred since its data was present at the input (e.g., the data on Q_{10} was input 10 clock pulses earlier). DATA is shifted into Segment 1 and shifted out from Segments 30, 32 or 38, depending on bonding option used.
3. A logic 1, shifted into the shift register (through DATA IN), causes the corresponding segment's output to be out of phase with the backplane.
4. A logic 1 on LOAD causes a parallel load of the data in the shift register, into the latches that control the output drivers.
5. LOAD may also be held high while clocking. In this case, the latch is transparent and, the falling edge of LOAD will latch the data.
6. To cascade units, (a) connect the DATA OUT of one chip to the DATA IN of the next chip, and (b) either connect the backplane of one chip to LCDϕ of all other chips (thus one RC provides frequency control for all chips) or connect LCDϕ of all chips to a common driving signal. If the former is chosen, the backplane that is tied to the LCDϕ of the other chips should not also be connected to the backplanes of those chips.
7. The LCDϕ pin can be used in two modes, driven or self-oscillating. If LCDϕ is driven, the circuit will sense this condition. If the LCDϕ pin is allowed to oscillate, its frequency is determined by an external capacitor. The Backplane frequency is a divide by 256 of the LCDϕ frequency, in the self-oscillating mode.
8. If LCDϕ is driven externally, it is in phase with the backplane output.
9. Backplanes can be tied together, if they have the same signal applied to their LDCϕ inputs.
10. In the self-oscillating mode, the backplane frequency is approximately defined by the relationship $f_{BP}(Hz) = 10 \div R(C + .0002)$ at $V_{DD} = 5V$, R in KΩ, C in μF.

    examples: R = 56KΩ, C = .0015μF: $f_{BP} \doteq 100Hz$
    R = 110KΩ, C = .00068μF: $f_{BP} \doteq 100Hz$
11. Minimum value of R for RC oscillator is 50KΩ.
12. Power consumption increases for clock rise or fall times greater than 100ns.

Ordering Information

1. All orders must specify a package type (i.e. S4520A, 48-pin plastic DIP)
2. All orders must specify whether an internal oscillator or external oscillator will be used (i.e. S4520B, external oscillator).
3. A set-up charge or minimum order quantity may apply for packaging options not shown.
4. Standard products available (refer to pages 1 and 8 for pin out descriptions):

Version	Package	Segments	Oscillator	Data Out
S4520A	48 DIP	38	Internal	38
S4520B	48 DIP	38	External	38
S4520C	48 CLCC	38	Internal	38
S4520D	48 CLCC	38	External	38
S4520F	48 DIP	38	External	32
S4520G	44 PLCC	32	Int or Ext	32

Chip Select Inverse Input

The $\overline{CS}$ input is used to enable clocking of the shift register. When $\overline{CS}$ is low, the chip will be selected and the shift register will be enabled. When $\overline{CS}$ is high, the shift register will be disabled and the output buffers will be driven by the data in the latches.

Clock Input

The CLOCK input is used to clock data serially, into the shift register. A clock signal may be continuously present, because the shift register is enabled only when $\overline{CS}$ is low.

Load Input

The LOAD input controls the operation of the data latches and allows new data to be loaded into the shift register, without changing the appearance of the display. When LOAD is high, the values in the shift register will be loaded into the data latches. If desired, LOAD can be held high and the data latches will be transparent. The LOAD input is disabled when $\overline{CS}$ is high.

LCD Oscillator Input

When used with an external oscillator, the LCD oscillator is driven by the input voltage level. In this configuration, the backplane output will be in phase with the input waveform. In the self-oscillating mode, an external resistor and capacitor are connected to the oscillator input pin, and the backplane frequency will be a divide by 256 of the internal oscillator frequency.

LCD Oscillator Options

Internal Oscillator — The LCD oscillator option (LCDϕ OPT) is internally (or externally) connected to the LCD oscillator input (LCDϕ) and, it provides the oscillator feedback.

External Oscillator — The LCD oscillator option is not connected.

Data Input

Data present at DATA IN will be clocked into the shift register, when $\overline{CS}$ is low. Data is loaded into the shift register on the falling edge of the clock and shifts to the output on the rising clock edge.

Data Output

Depending on the packaging option selected, DO30, DO32 and DO38 are buffered outputs driven by the corresponding element of the shift register. The value of DOxx will be the same as the value of the matching shift register bit (i.e. the value at DO32 will be the same as bit 32 of the shift register). The data output is typically used to drive the data input of another S4520. By cascading S4520 circuits in this manner, additional display elements can be driven.

Backplane Output

The backplane output provides the voltage waveform for the LCD backplane. When used with the internal oscillator, the backplane frequency will be equal to the oscillator frequency divided by 256:

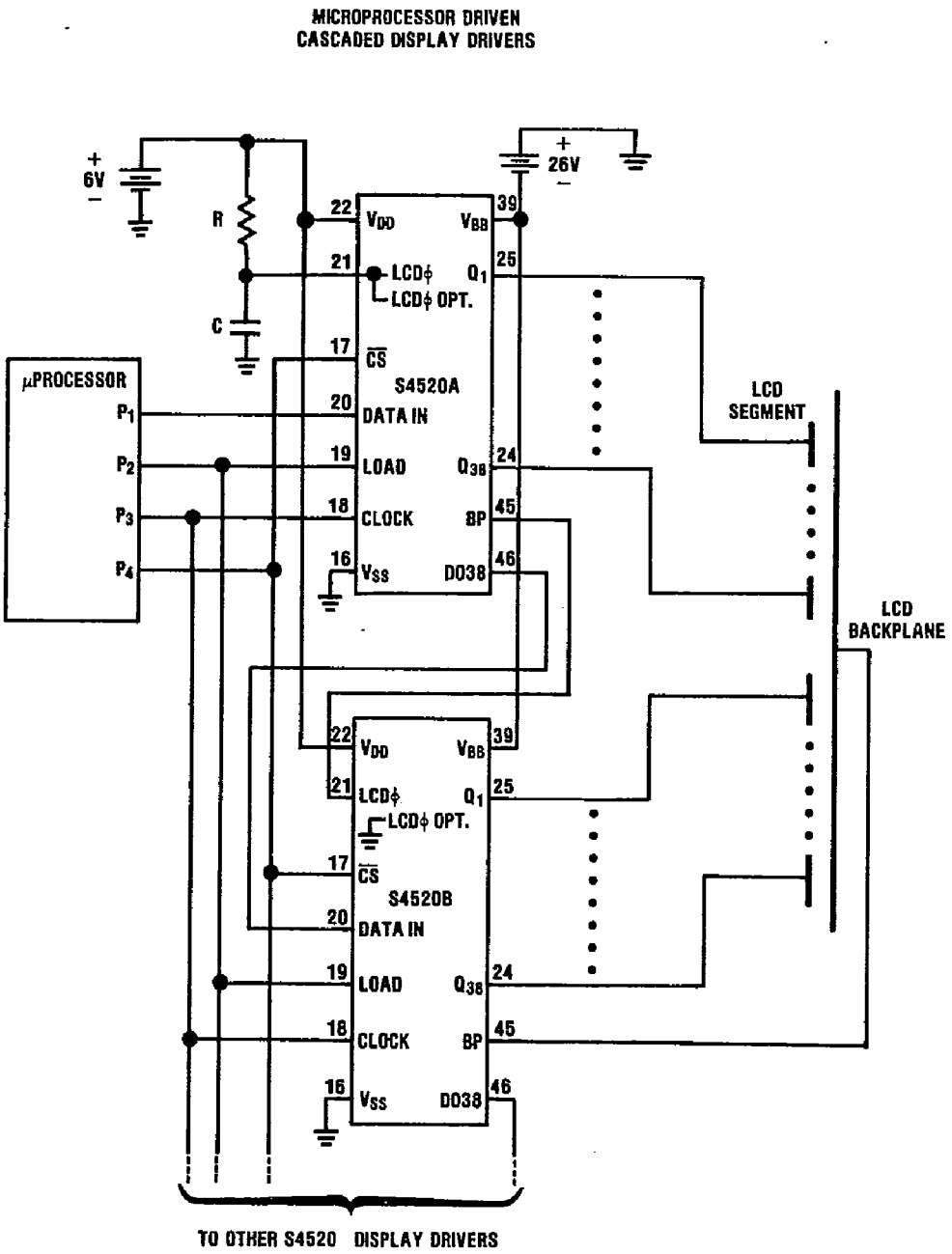
$$f_{BP} = f_{OSC}\,(\text{Int}) \div 256.$$

With an external oscillator, the backplane frequency will be in phase with and equal in magnitude to the input signal.

Segment Drive Outputs

The segment drive outputs provide the segment drive voltage to the LCD. With a logic level "1" in the latch associated with the segment drive output, the output voltage will be out of phase with the backplane (i.e the segment will be ON). A logic level "0" will cause the segment drive to be in phase with the backplane output voltage.

Figure 2. Typical Application



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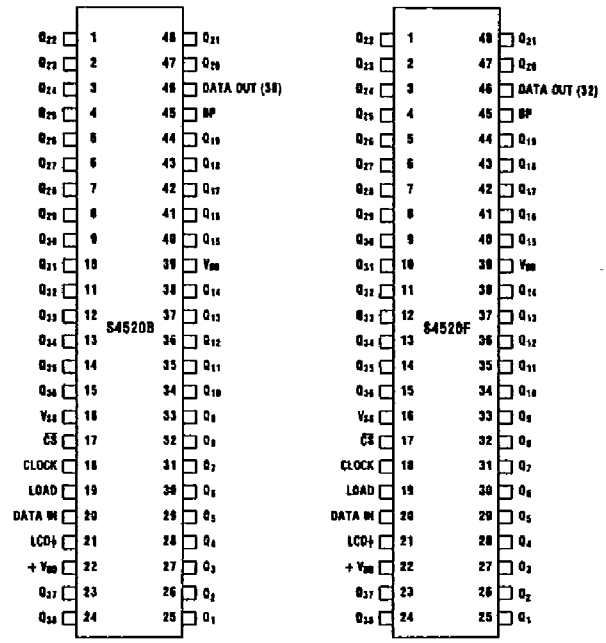
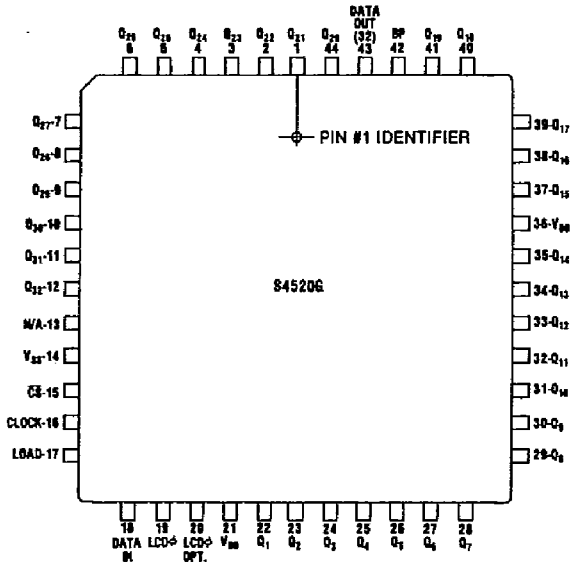
S4520

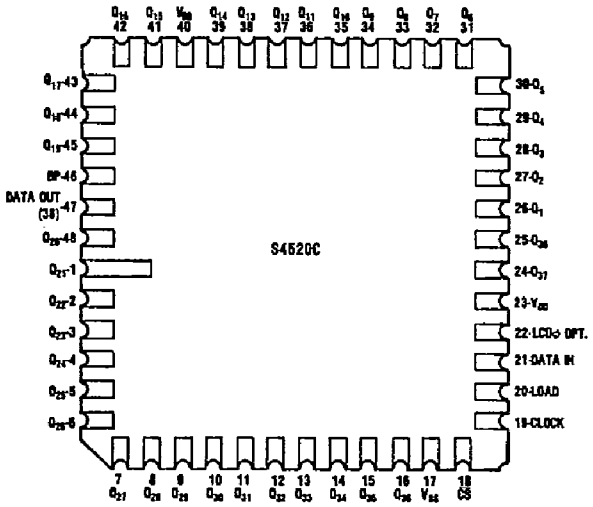
48-Lead Plastic Dual In Line Package

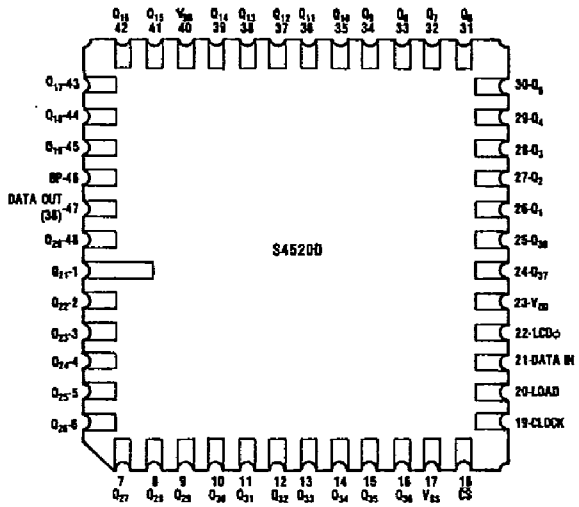


44-Plastic Leaded Chip Carrier (PLCC)



48-Ceramic Leadless Chip Carrier (CLCC)





NOTE: Viewed From Top Side of Package