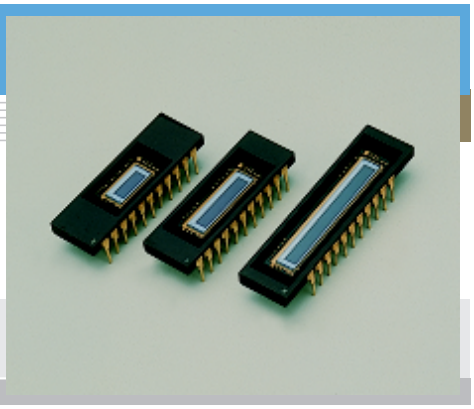


NMOS linear image sensor
S3901/S3904 series

Current output, high UV sensitivity, excellent linearity, low power consumption

NMOS linear image sensors are self-scanning photodiode arrays designed specifically as detectors for multichannel spectroscopy. The scanning circuit is made up of N-channel MOS transistors, operates at low power consumption and is easy to handle. Each photodiode has a large active area, high UV sensitivity yet very low noise, delivering a high S/N even at low light levels. NMOS linear image sensors also offer excellent output linearity and wide dynamic range.
The photodiodes of S3901 series have a height of 2.5 mm and are arrayed in a row at a spacing of 50 µm. The photodiodes of S3904 series also have a height of 2.5 mm but are arrayed at a spacing of 25 µm. The photodiodes are available in 3 different pixel quantities for each series: 128 (S3901-128Q), 256 (S3901-256Q, S3904-256Q), 512 (S3901-512Q, S3904-512Q) and 1024 (S3904-1024Q). Quartz glass is the standard window material.

Features

- Wide active area
  Pixel pitch: 50 µm (S3901 series)
  25 µm (S3904 series)
  Pixel height: 2.5 mm
- High UV sensitivity with good stability
- Low dark current and high saturation charge allow a long integration time and a wide dynamic range at room temperature
- Excellent output linearity and sensitivity spatial uniformity
- Lower power consumption: 1 mW Max.
- Start pulse and clock pulses are CMOS logic compatible

Applications

- Multichannel spectrophotometry
- Image readout system

Figure 1 Equivalent circuit

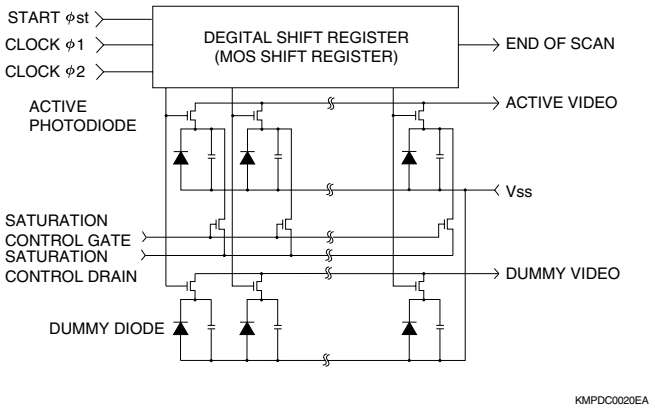
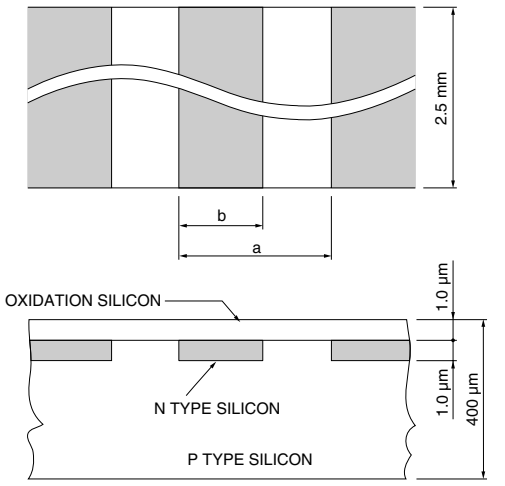


Figure 2 Active area structure



■ Absolute maximum ratings

Parameter	Symbol	Value	Unit
Input pulse (φ1, φ2, φst) voltage	Vφ	15	V
Power consumption *1	P	1	mW
Operating temperature *2	Topr	-40 to +65	°C
Storage temperature	Tstg	-40 to +85	°C

*1: Vφ=5.0 V
*2: No dew

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■ Shape specifications

Parameter	S3901-128Q	S3901-256Q	S3901-512Q	S3904-256Q	S3904-512Q	S3904-1024Q	Unit
Number of pixels	128	256	512	256	512	1024	-
Package length	31.75		40.6	31.75		40.6	mm
Number of pins	22			22			-
Window material *3	Quartz			Quartz			-
Weight	3.0		3.5	3.0		3.5	g

*3: Fiber optic plate is available.

■ Specifications (Ta=25 °C)

Parameter	Symbol	S3901 series			S3904 series			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Pixel pitch	-	-	50	-	-	25	-	μm
Pixel height	-	-	2.5	-	-	2.5	-	mm
Spectral response range (10 % of peak)	λ	200 to 1000			200 to 1000			nm
Peak sensitivity wavelength	λp	-	600	-	-	600	-	nm
Photodiode dark current *4	ID	-	0.2	0.6	-	0.1	0.3	pA
Photodiode capacitance *4	Cph	-	20	-	-	10	-	pF
Saturation exposure *4, *5	Esat	-	180	-	-	180	-	$mlx \cdot s$
Saturation output charge *4	Qsat	-	50	-	-	25	-	pC
Photo response non-uniformity *6	PRNU	-	-	±3	-	-	±3	%

*4: Vb=2.0 V, Vϕ=5.0 V
*5: 2856 K, tungsten lamp
*6: 50 % of saturation, excluding the start pixel and last pixel

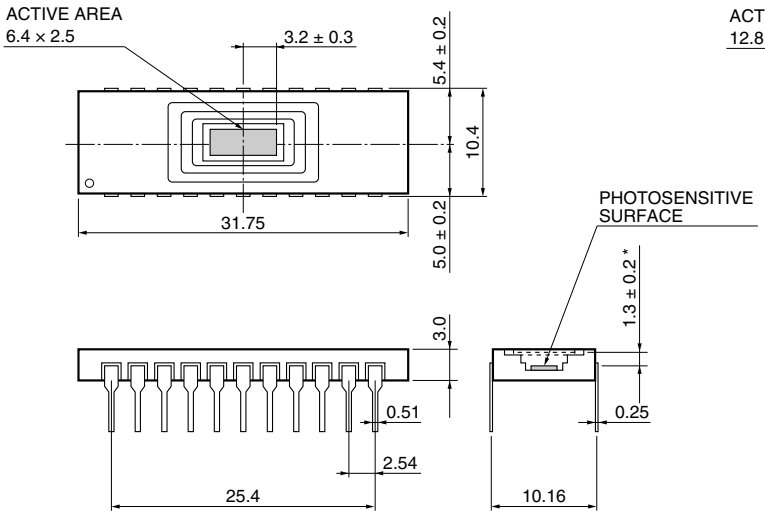
■ Electrical characteristics (Ta=25 °C)

Parameter		Symbol	Condition	S3901 series			S3904 series			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Clock pulse (ϕ1, ϕ2) voltage	High	Vϕ1, Vϕ2 (H)		4.5	5	10	4.5	5	10	V
	Low	Vϕ1, Vϕ2 (L)		0	-	0.4	0	-	0.4	V
Start pulse (ϕst) voltage	High	Vϕs (H)		4.5	Vϕ1	10	4.5	Vϕ1	10	V
	Low	Vϕs (L)		0	-	0.4	0	-	0.4	V
Video bias voltage *7		Vb		1.5	Vϕ - 3.0	Vϕ - 2.5	1.5	Vϕ - 3.0	Vϕ - 2.5	V
Saturation control gate voltage		Vscg		-	0	-	-	0	-	V
Saturation control drain voltage		Vscd		-	Vb	-	-	Vb	-	V
Clock pulse (ϕ1, ϕ2) rise / fall time *8		trϕ1, trϕ2 tfϕ1, tfϕ2		-	20	-	-	20	-	ns
Clock pulse (ϕ1, ϕ2) pulse width		tpwϕ1, tpwϕ2		200	-	-	200	-	-	ns
Start pulse (ϕst) rise / fall time		trϕs, tfϕs		-	20	-	-	20	-	ns
Start pulse (ϕst) pulse width		tpwϕs		200	-	-	200	-	-	ns
Start pulse (ϕst) and clock pulse (ϕ2) overlap		tϕov		200	-	-	200	-	-	ns
Clock pulse space *8		X1, X2		trf - 20	-	-	trf - 20	-	-	ns
Data rate *9		f		0.1	-	2000	0.1	-	2000	kHz
Video delay time		tvd	50 % of saturation *9, *10	-	80 (-128 Q)	-	-	100 (-256 Q)	-	ns
				-	120 (-256 Q)	-	-	150 (-512 Q)	-	ns
				-	160 (-512 Q)	-	-	200 (-1024 Q)	-	ns
Clock pulse (ϕ1, ϕ2) line capacitance		Cϕ	5 V bias	-	21 (-128 Q)	-	-	27 (-256 Q)	-	pF
				-	36 (-256 Q)	-	-	50 (-512 Q)	-	pF
				-	67 (-512 Q)	-	-	100 (-1024 Q)	-	pF
Saturation control gate (Vscg) line capacitance		Cscg	5 V bias	-	12 (-128 Q)	-	-	14 (-256 Q)	-	pF
				-	20 (-256 Q)	-	-	24 (-512 Q)	-	pF
				-	35 (-512 Q)	-	-	45 (-1024 Q)	-	pF
Video line capacitance		CV	2 V bias	-	7 (-128 Q)	-	-	10 (-256 Q)	-	pF
				-	11 (-256 Q)	-	-	16 (-512 Q)	-	pF
				-	20 (-512 Q)	-	-	30 (-1024 Q)	-	pF

*7: Vϕ is input pulse voltage (refer to figure 8).
*8: trf is the clock pulse rise or fall time. A clock pulse space of "rise time/fall time - 20" ns (nanoseconds) or more should be input if the clock pulse rise or fall time is longer than 20 ns (refer to figure 7).
*9: Vb=2.0 V, Vϕ=5.0 V
*10: Measured with C7883 driver circuit.

Figure 3 Dimensional outlines (unit: mm)

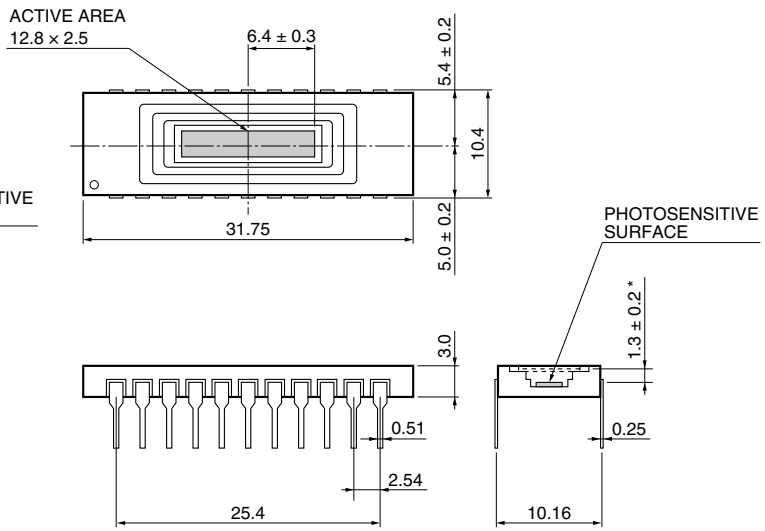
S3901-128Q, S3904-256Q



* Optical distance from the outer surface of the quartz window to the chip surface

KMPDA0060EA

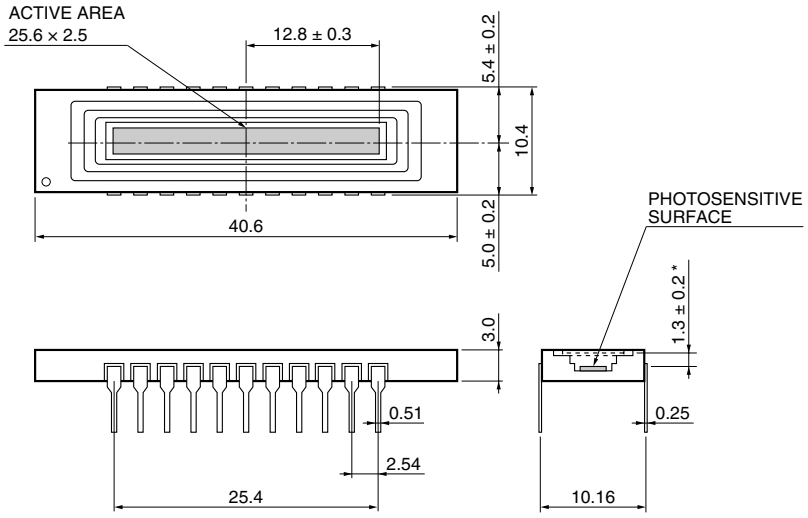
S3901-256Q, S3904-512Q



* Optical distance from the outer surface of the quartz window to the chip surface

KMPDA0061EA

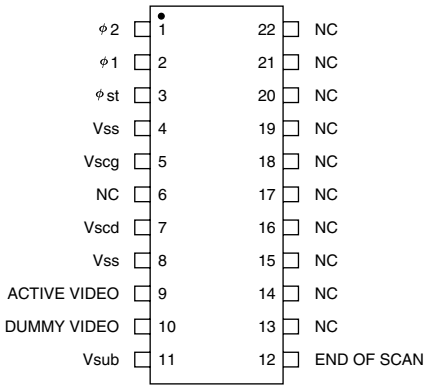
S3901-512Q, S3904-1024Q



* Optical distance from the outer surface of the quartz window to the chip surface

KMPDA0062EA

Figure 4 Pin connection



Vss, Vsub and NC should be grounded.

KMPDC0056EA

Terminal	Input or output	Description
ϕ1, ϕ2	Input (CMOS logic compatible)	Pulses for operating the MOS shift register. The video data rate is equal to the clock pulse frequency since the video output signal is obtained synchronously with the rise of ϕ2 pulse.
ϕst	Input (CMOS logic compatible)	Pulse for starting the MOS shift register operation. The time interval between start pulses is equal to the signal accumulation time.
Vss	-	Connected to the anode of each photodiode. This should be grounded.
Vscg	Input	Used for restricting blooming. This should be grounded.
Vscd	Input	Used for restricting blooming. This should be biased at a voltage equal to the video bias voltage.
Active video	Output	Video output signal. Connects to photodiode cathodes when the address is on. A positive voltage should be applied to the video line in order to use photodiodes with a reverse voltage. When the amplitude of ϕ1 and ϕ2 is 5 V, a video bias voltage of 2 V is recommended.
Dummy video	Output	This has the same structure as the active video, but is not connected to photodiodes, so only spike noise is output. This should be biased at a voltage equal to the active video or left as an open-circuit when not needed.
Vsub	-	Connected to the silicon substrate. This should be grounded.
End of scan	Output (CMOS logic compatible)	This should be pulled up at 5 V by using a 10 kΩ resistor. This is a negative going pulse that appears synchronously with the ϕ2 timing right after the last photodiode is addressed.
NC	-	Should be grounded.

Figure 5 Spectral response (typical example)

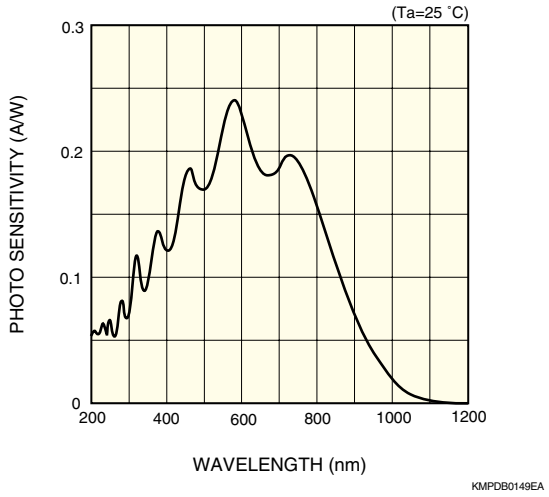
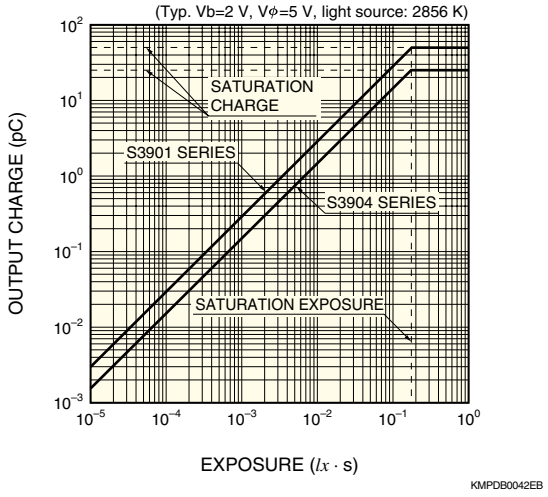


Figure 6 Output charge vs. exposure



■ Construction of image sensor

The NMOS image sensor consists of a scanning circuit made up of MOS transistors, a photodiode array, and a switching transistor array that addresses each photodiode, all integrated onto a monolithic silicon chip. Figure 1 shows the circuit of a NMOS linear image sensor.

The MOS scanning circuit operates at low power consumption and generates a scanning pulse train by using a start pulse and 2-phase clock pulses in order to turn on each address sequentially. Each address switch is comprised of an NMOS transistor using the photodiode as the source, the video line as the drain and the scanning pulse input section as the gate.

The photodiode array operates in charge integration mode so that the output is proportional to the amount of light exposure (light intensity × integration time).

Each cell consists of an active photodiode and a dummy photodiode, which are respectively connected to the active video line and the dummy video line via a switching transistor. Each of the active photodiodes is also connected to the saturation control drain via the saturation control transistor, so that the photodiode blooming can be suppressed by grounding the saturation control gate. Applying a pulse signal to the saturation control gate triggers all reset. (See “Auxiliary functions”.)

Figure 2 shows the schematic diagram of the photodiode active area. This active area has a PN junction consisting of an N-type diffusion layer formed on a P-type silicon substrate. A signal charge generated by light input accumulates as a capacitive charge in this PN junction. The N-type diffusion layer provides high UV sensitivity but low dark current.

■ Driver circuit

S3901/S3904 series do not require any DC voltage supply for operation. However, the Vss, Vsub and all NC terminals must be grounded. A start pulse ϕst and 2-phase clock pulses ϕ1, ϕ2 are needed to drive the shift register. These start and clock pulses are positive going pulses and CMOS logic compatible.

The 2-phase clock pulses ϕ1, ϕ2 can be either completely separated or complementary. However, both pulses must not be "High" at the same time.

A clock pulse space (X1 and X2 in Figure 7) of a "rise time/fall time - 20" ns or more should be input if the rise and fall times of ϕ1, ϕ2 are longer than 20 ns. The ϕ1 and ϕ2 clock pulses must be held at "High" at least 200 ns. Since the photodiode signal is obtained at the rise of each ϕ2 pulse, the clock pulse frequency will equal the video data rate.

The amplitude of start pulse ϕst is the same as the ϕ1 and ϕ2 pulses. The shift register starts the scanning at the "High" level of ϕst, so the start pulse interval determines the length of signal accumulation time. The ϕst pulse must be held "High" at least 200 ns and overlap with ϕ2 at least for 200 ns. To operate the shift register correctly, ϕ2 must change from the "High" level to the "Low" level only once during "High" level of ϕst. The timing chart for each pulse is shown in Figure 7.

■ End of scan

The end of scan ($\overline{EOS}$) signal appears in synchronization with the ϕ2 timing right after the last photodiode is addressed, and the $\overline{EOS}$ terminal should be pulled up at 5 V using a 10 kΩ resistor.

Figure 7 Timing chart for driver circuit

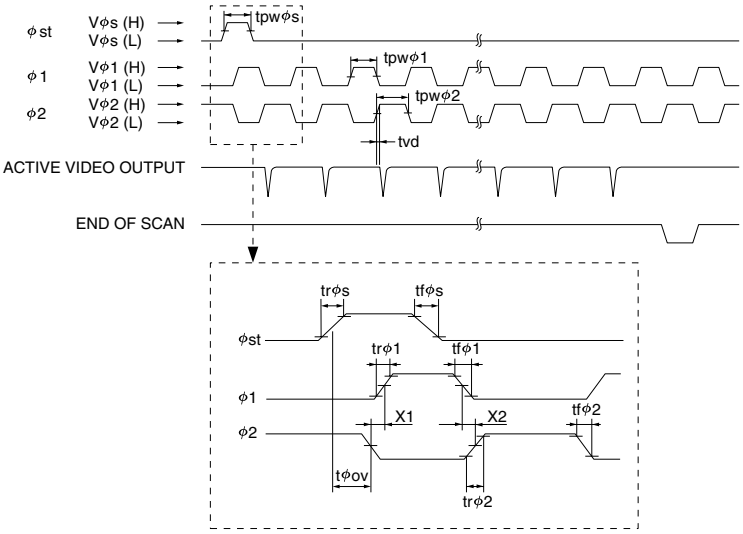
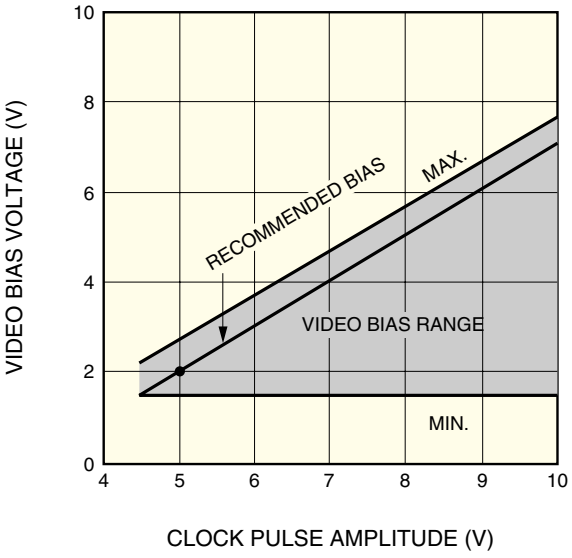


Figure 8 Video bias voltage margin



KMPDC0022EA KMPDB0043EA

■ Signal readout circuit

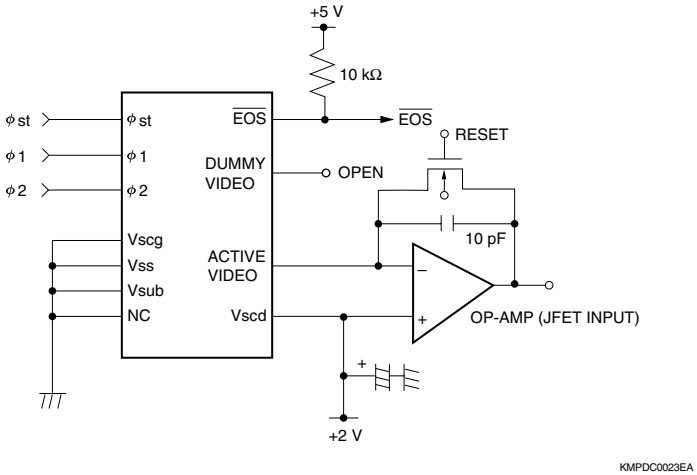
There are two methods for reading out the signal from an NMOS linear image sensor. One is a current detection method using the load resistance and the other is a current integration method using a charge amplifier. In either readout method, a positive bias must be applied to the video line because photodiode anodes of NMOS linear image sensors are set at 0 V (Vss). Figure 8 shows a typical video bias voltage margin. As the clock pulse amplitude is higher, the video bias voltage can be set larger so the saturation charge can be increased. The rise and fall times of the video output waveform can be shortened if the video bias voltage is reduced while the clock pulse amplitude is still higher. When the amplitude of ϕ1, ϕ2 and ϕst is 5 V, setting the video bias voltage at 2 V is recommended.

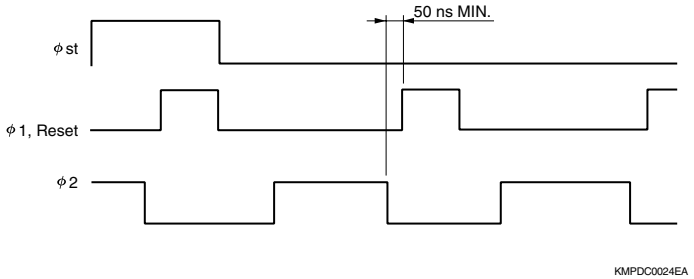
To obtain good linearity, using the current integration method is advised. In this method, the integration capacitance is reset to the reference voltage level immediately before each photodiode is addressed and the signal charge is then stored as an integration capacitive charge when the address switch turns on. Figures 9 and 10 show a typical current integration circuit and its pulse timing chart. To ensure stable output, the rise of a reset pulse must be delayed at least 50 ns from the fall of ϕ2.

Hamamatsu provides the following driver circuits and related products (sold separately).

Product name	Type No.	Content	Feature
Driver circuit	C7883	High-speed driver circuit	High-speed operation Single power supply (+15 V) operation Compact
	C7883G	C7883 + C8225-01	
	C7884	Precision driver circuit	Low noise Good output linearity Boxcar waveform output
	C7884G	C7884 + C8225-01	
	C7884-01	High precision driver circuit	Ultra-low noise Good output linearity Boxcar waveform output
	C7884G-01	C7884-01 + C8225-01	
Pulse generator	C8225-01	C7883, C7884 series	
Cable	A8226	C7883 to C7885 series	BNC, length 1 m

Figure 9 Readout circuit example and timing chart





Output voltage Vout is

$$Vout\ [V] = \frac{\text{Output charge [C]}}{10 \times 10^{-12}\ [F]}$$

shown in.

■ Anti-blooming function

If the incident light intensity is higher than the saturation charge level, even partially, a signal charge in excess of the saturation charge cannot accumulate in the photodiode. This excessive charge flows out into the video line degrading the signal purity. To avoid this problem and maintain the signal purity, applying the same voltage as the video bias voltage to the saturation control drain and grounding the saturation control gate are effective. If the incident light intensity is extremely high, a positive bias should be applied to the saturation control gate. The larger the voltage applied to the saturation control gate, the higher the function for suppressing the excessive saturation charge will be. However, this voltage also lowers the amount of saturation charge, so an optimum bias voltage should be selected.

■ Auxiliary functions

1) All reset

In normal operation, the accumulated charge in each photodiode is reset when the signal is read out. Besides this method that uses the readout line, S3901/S3904 series can reset the photodiode charge by applying a pulse to the saturation control gate. The amplitude of this pulse should be equal to the φ1, φ2 and φst pulses and the pulse width should be longer than 5 μs. When the saturation control gate is set at the “High” level, all photodiodes are reset to the saturation control drain potential (equal to video bias). Conversely, when the saturation control gate is set at the “Low” level (0 V), the signal charge accumulates in each photodiode without being reset.

2) Dummy video

S3901/S3904 series have a dummy video line to eliminate spike noise contained in the video output waveform. Video signal with lower spike noise can be obtained by differential amplification applied between the active video line and dummy video line outputs. When not needed, leave this unconnected.

■ Handling precautions

1) Electrostatic countermeasures

NMOS linear image sensors are designed to resist static electrical charges. However, take sufficient cautions and countermeasures to prevent damage from static charges when handling the sensors.

2) Window

If dust or grime sticks to the surface of the light input window, it appears as a black blemish or smear on the image. Before using the image sensor, the window surface should be cleaned. Wipe off the window surface with a soft cloth, cleaning paper or cotton swab slightly moistened with organic solvent such as alcohol, and then lightly blow away with compressed air. Do not rub the window with dry cloth or cotton swab as this may generate static electricity.

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