4K Serial E^2PROM with a Precision Low-V_{CC} Lockout Circuit 3 and 5 Volt Systems

FEATURES

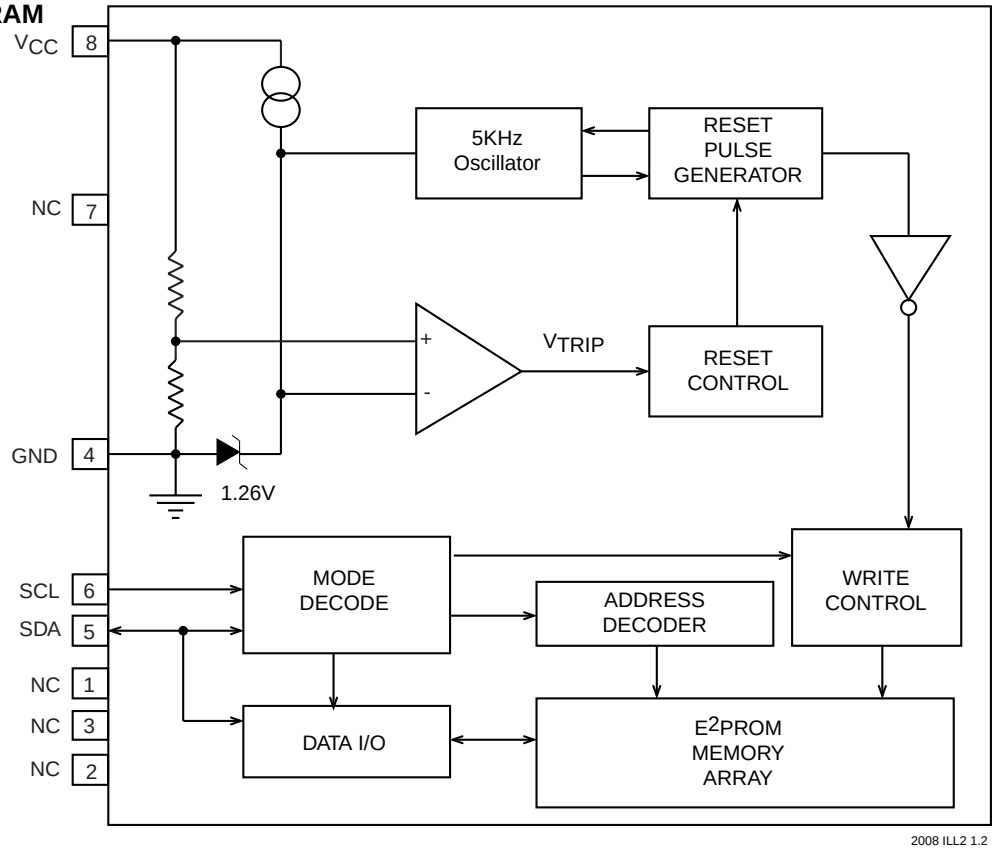
- **Voltage Protection™**
- **Precision Low-V_{CC} Write Lockout**
- **All Write Operations Inhibited When V_{CC} Falls below V_{LOCK}**
- **One 3Volt and Two 5Volt System Versions**
  - **V_{LOCK} = 2.6V+.1V/-.05V**
  - **V_{LOCK} = 4.25V +.25V/-0.0V**
  - **V_{LOCK} = 4.50 +.25V/-0.0V**
- **100% Compatible with Industry Standard I^2C™ Devices**
  - **Bi-directional data transfer protocol**
  - **Standard 100kHz and 400kHz Transfer Rates**
- **16-Byte Page-Write Mode**
  - **Minimizes total write time per byte**
- **1,000,000 Program/Erase Cycles**
- **100 Year Data Retention**
- **Commercial Industrial Temperature Range**

OVERVIEW

The S24VP04 is a 4K-bit serial E^2PROM memory integrated with a precision V_{CC} sense circuit. The sense circuit will disable write operations whenever V_{CC} falls below the V_{LOCK} voltage. It is fabricated using SUMMIT's advanced CMOS E^2PROM technology and is suitable for both 3 and 5 volt systems.

The S24VP04 is internally organized as 512 x 8. It features the I^2C serial interface and software protocol allowing operation on a simple two-wire bus.

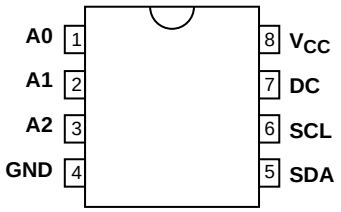
BLOCK DIAGRAM



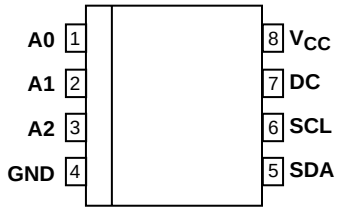
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PIN CONFIGURATIONS

Plastic Dual-in-line
"P" Package



JEDEC Small Outline
"S" Package



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PIN NAMES

A0, A1,A2	Address Inputs
SDA	Serial Data I/O
SCL	Serial Clock Input
DC	Don't Care
GND	Ground
V_{CC}	Supply Voltage

PIN DESCRIPTIONS

Serial Clock (SCL) - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

Serial Data (SDA) - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

Address Inputs A0, A1, A2- Device Address Inputs

These inputs are unused by the S24VP04; however, to ensure proper operation they should be left unconnected or tied to ground. The should not be tied high.

ENDURANCE AND DATA RETENTION

The S24VP04 is designed for applications requiring 1,000,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 1,000,000 erase/write cycles.

DEVICE OPERATION

APPLICATIONS

The S24VP04 was designed specifically for applications where the integrity of the stored data is paramount. In recent years, as the operating voltage range of serial E^2PROMs has widened, most semiconductor manufacturers have arbitrarily eliminated their V_{CC} sense circuits. The S24VP04 will protect your data by guaranteeing write lockout below the selected V_{CC} Lockout voltage.

V_{CC} Lockout

The S24VP04 has an on-board precision V_{CC} sense circuit. Whenever V_{CC} is below V_{LOCK}, the S24VP04 will disable the internal write circuitry. The V_{CC} lockout circuit will ensure a higher level of data integrity than can be expected from industry standard devices that have either a very loose specification or no V_{CC} lockout specification.

During a power-on sequence all writes will be inhibited below the V_{LOCK} level and will continue to be held in a write inhibit state for approximately 200ms after V_{CC} reaches, then stays at or above V_{LOCK}. The 200ms delay provides a buffer space for the microcontroller to complete its power-on initialization routines (reading is OK) while still protecting against inadvertent writes.

During a power-down sequence initiation of writes will be inhibited whenever V_{CC} falls below V_{LOCK}. This will guard against the system's microcontroller performing an inadvertent write within the 'danger zone'. (see AN001)

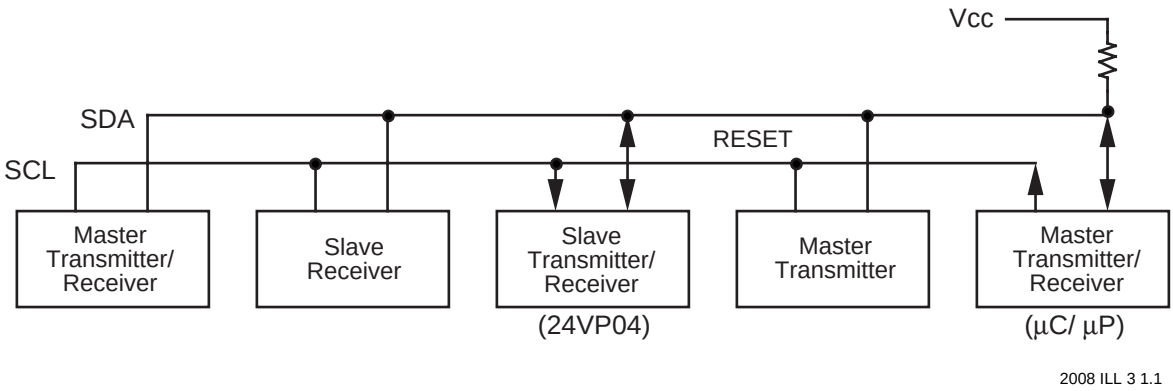


FIGURE 1. TYPICAL SYSTEM CONFIGURATION

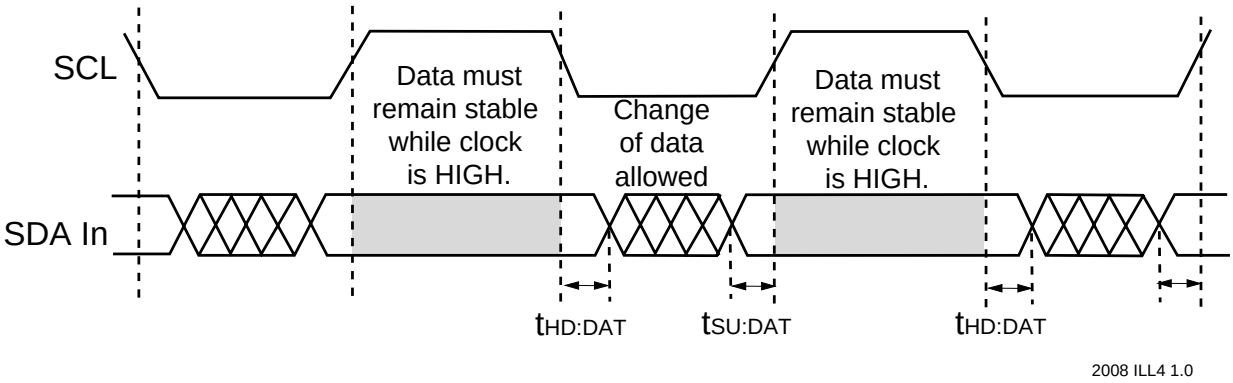


FIGURE 2. INPUT DATA PROTOCOL

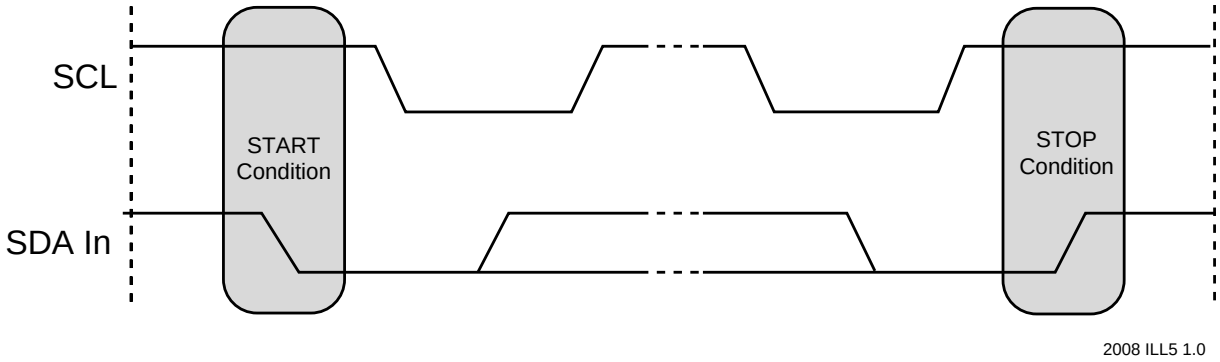


FIGURE 3. START AND STOP CONDITIONS

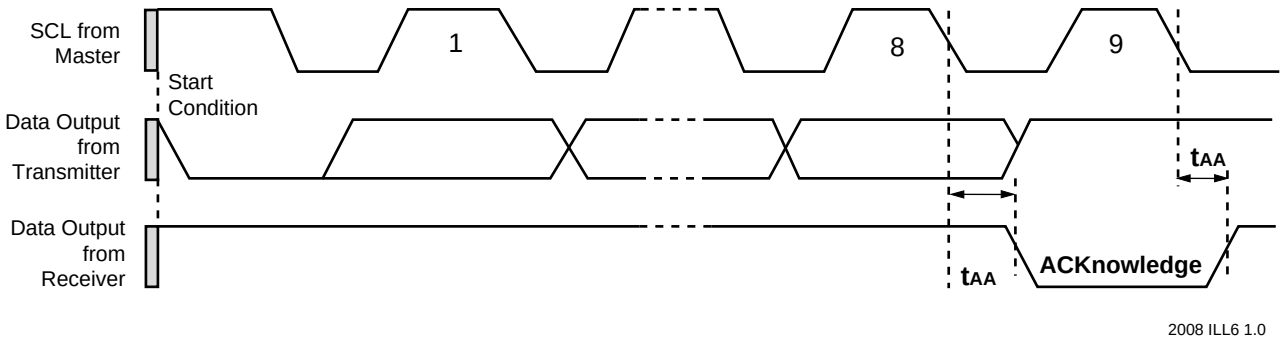


FIGURE 4. ACKNOWLEDGE RESPONSE FROM RECEIVER

CHARACTERISTICS OF THE I²C BUS

General Description

The I²C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition (See Figure 2).

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the “START” condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the “STOP” condition (See Figure 3).

DEVICE OPERATION

The S24VP04 is a 16,384-bit serial E²PROM. The device supports the I²C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a “transmitter” and any device which receives data as a “receiver.” The device controlling data transmission is called the “master” and the controlled device is called the “slave.” In all cases, the S24VP04 will be a “slave” device, since it never initiates any data transfers.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 4).

The S24VP04 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the S24VP04 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the S24VP04 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the S24VP04 will continue to transmit data. If an ACKnowledge is not detected, the S24VP04 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 5). For the S24VP04 this is fixed as 1010[B].

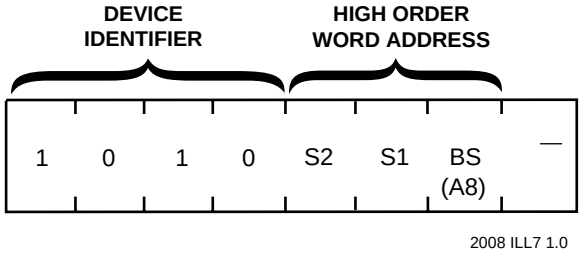


FIGURE 5. SLAVE ADDRESS BYTE

The next two bits are don't care. The S24VP04 will respond to all commands for device 1010.

Bank Select Bit
The next bit of the serial stream is the bank select bit. It is used by the host to toggle between the two 2K-bit banks of memory. It is, in effect, the most significant bit of the word address, or A8.

Read/Write Bit
The last bit of the data stream defines the operation to be performed. When set to "1," a read operation is selected; when set to "0," a write operation is selected.

WRITE OPERATIONS

The S24VP04 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR}.

Byte WRITE
After the slave address is sent (to identify the slave device, specify high order word address and a read or write operation), a second byte is transmitted which contains the low 8 bit addresses of any one of the 512 words in the array.

Upon receipt of the word address, the S24VP04 responds with an ACKnowledge. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the S24VP04 begins the internal write cycle.

While the internal write cycle is in progress, the S24VP04 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

Page WRITE
The S24VP04 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more words of data. After the receipt of each word, the S24VP04 will respond with an ACKnowledge.

The S24VP04 automatically increments the address for subsequent data words. After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than sixteen words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

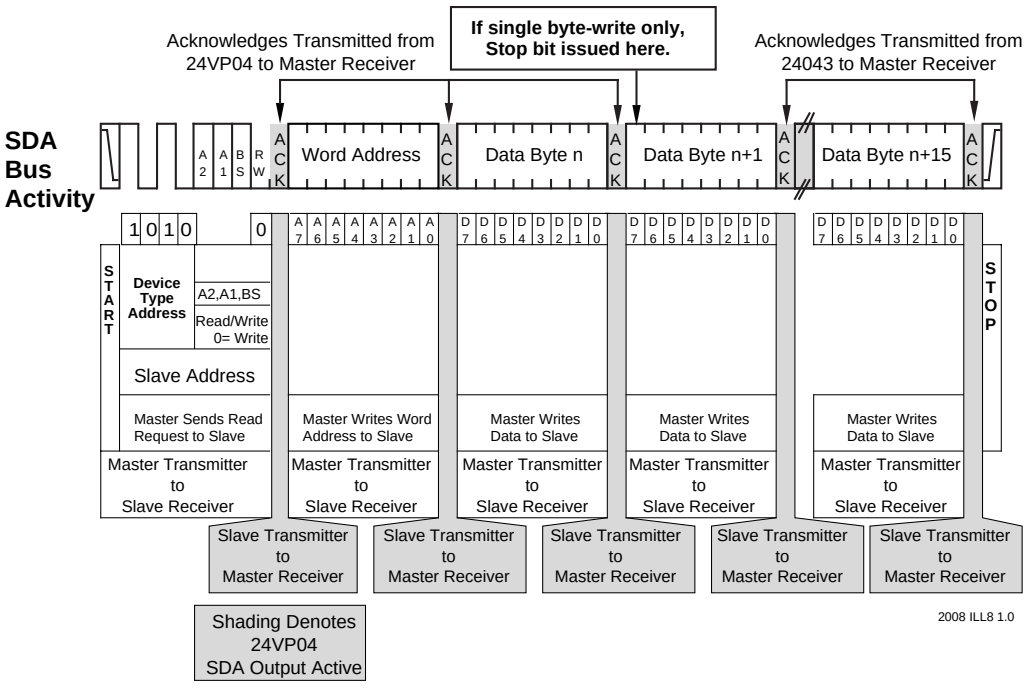


FIGURE 6. PAGE/BYTE WRITE MODE

Acknowledge Polling

When the S24VP04 is performing an internal WRITE operation, it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 7).

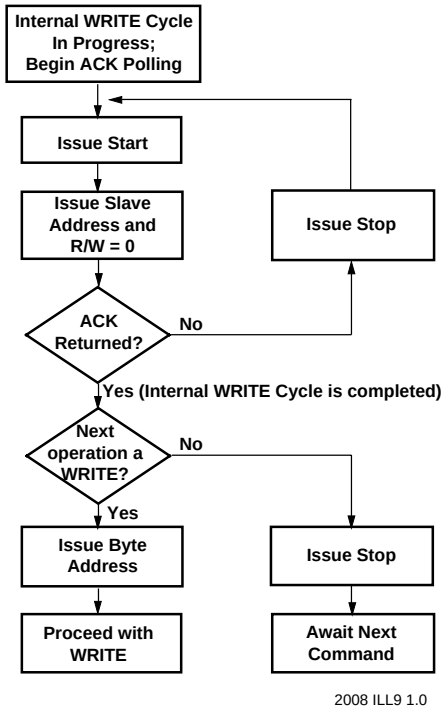


FIGURE 7. ACKNOWLEDGE POLLING

READ OPERATIONS

Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The S24VP04 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n, the next read operation would access data from address location n+1 and increment the current address pointer. When the S24VP04 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location n+1.

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the S24VP04 discontinues data transmission. See Figure 8 for the address acknowledge and data transfer sequence.

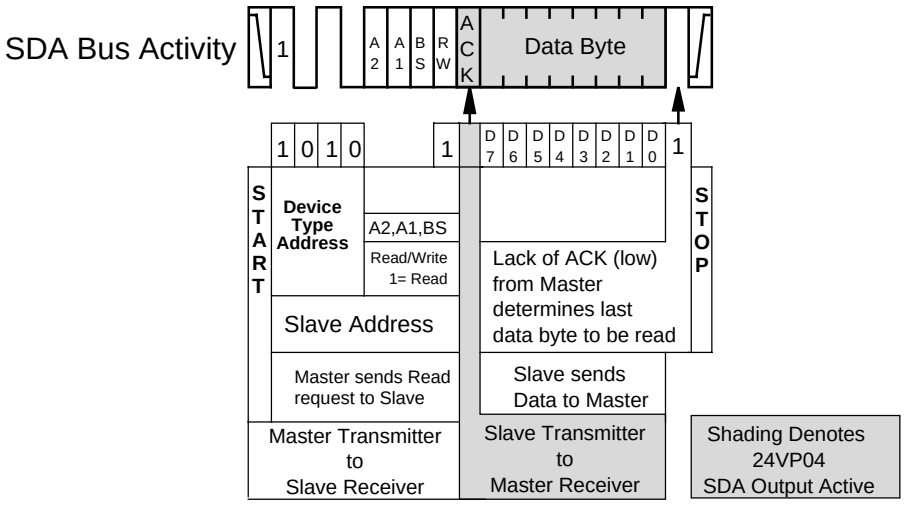


FIGURE 8. CURRENT ADDRESS BYTE READ MODE

Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the S24VP04 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The S24VP04 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The S24VP04 discontinues data transmission and reverts to its standby power mode. See Figure 9 for the address, acknowledge and data transfer sequence.

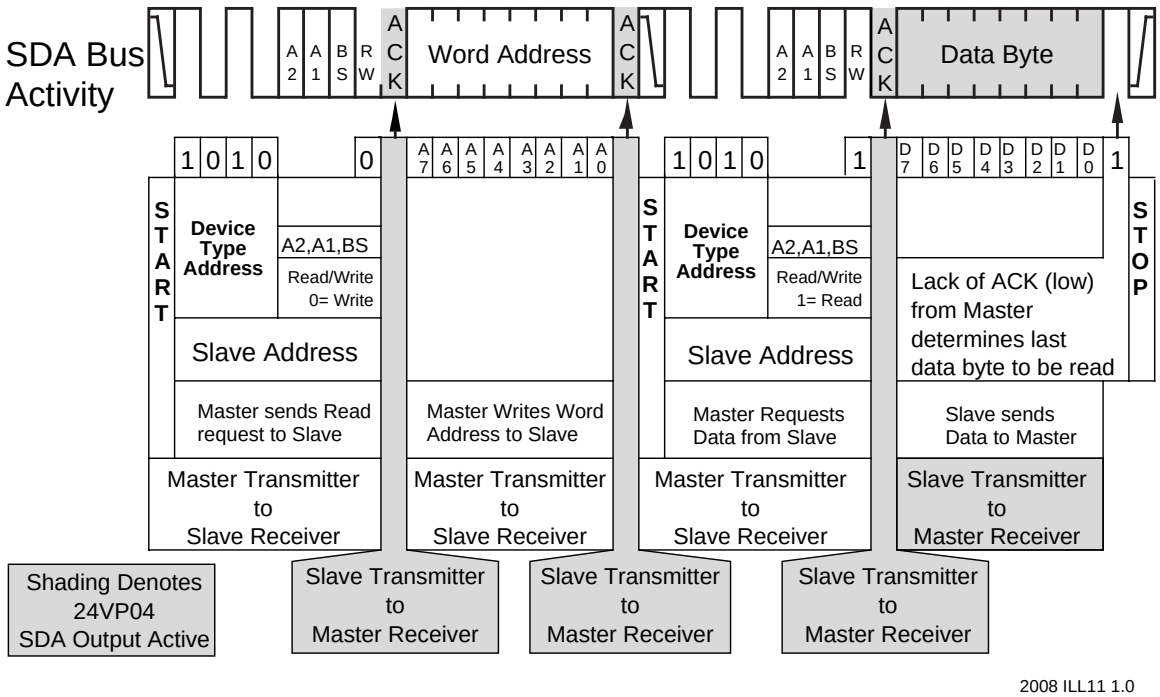


FIGURE 9. RANDOM ADDRESS BYTE READ MODE

Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the S24VP04. The S24VP04 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 10 for the address, acknowledge and data transfer sequence.

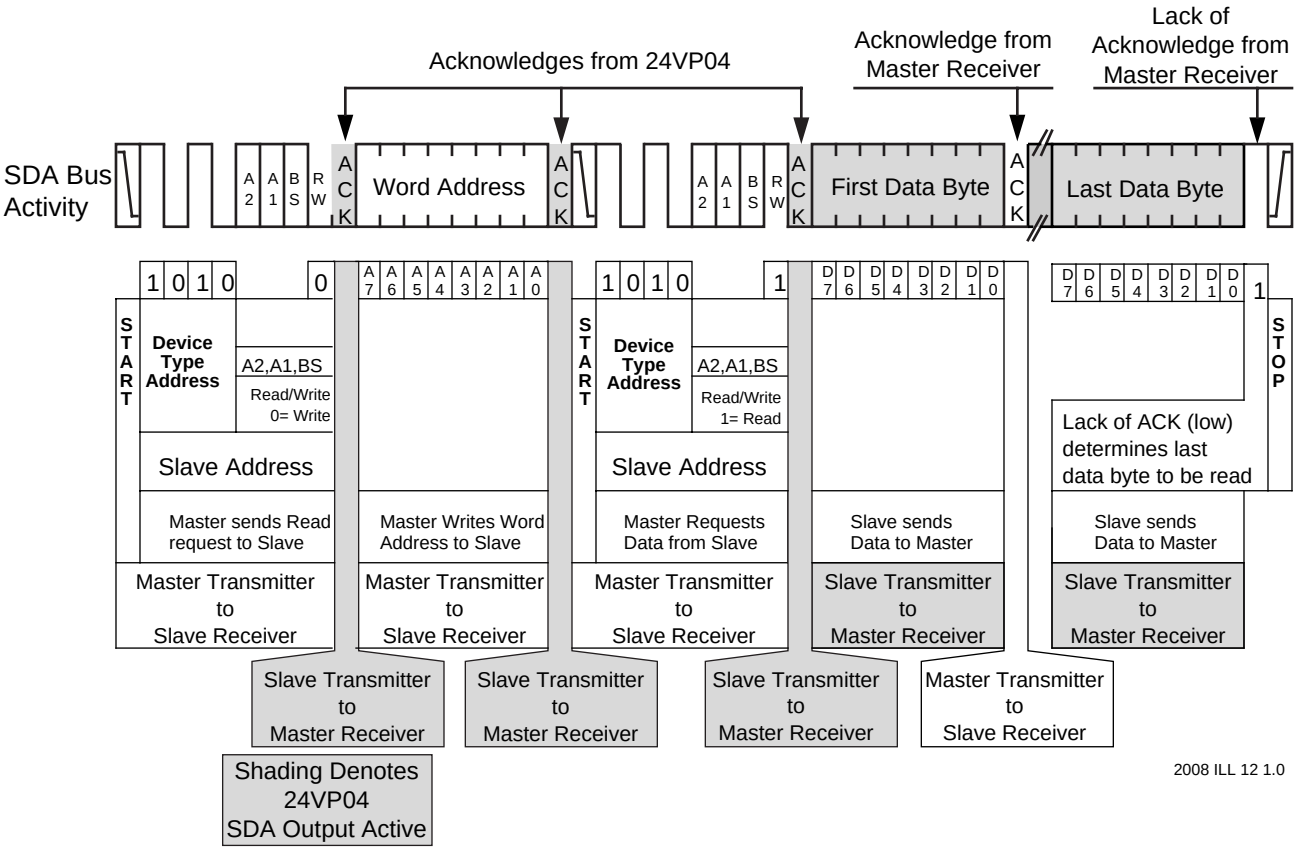


FIGURE 10. SEQUENTIAL READ OPERATION (starting with a Random Address READ)

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -40°C to +85°C
Storage Temperature ..... -65°C to +125°C
Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.3V to V_{CC}+0.3V
ESD Voltage (JEDEC method) 2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

S24VP04, T_A = -40°C to +85°C, V_{CC} = 5V ± 10%
S24VP04-3, T_A = -40°C to +85°C, V_{CC} = 2.7V to 5.5V

Symbol	Parameter	Conditions		Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	V_{CC} =5.5V		3	mA
			V_{CC} =3.3V		2	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND	V_{CC} =5.5V		50	µA
			V_{CC} =3.3V		25	µA
I_{LI}	Input Leakage	V_{IN} = 0 To V_{CC}			10	µA
I_{LO}	Output Leakage	V_{OUT} = 0 To V_{CC}			10	µA
V_{IL}	Input Low Voltage	S0, S1, S2, SCL, SDA, RESET			0.3xV_{CC}	V
V_{IH}	Input High Voltage	S0, S1, S2, SCL, SDA		0.7xV_{CC}		V
V_{OL}	Output Low Voltage	I_{OL} = 3mA			0.4	V

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AC ELECTRICAL CHARACTERISTICS

S24VP04, T_A = -40°C to +85°C, V_{CC} = 5V ± 10%
S24VP04-3, T_A = -40°C to +85°C, V_{CC} = 2.7V to 5.5V

			2.7V to 4.5V		4.5V to 5.5V		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Units
f_{SCL}	SCL Clock Frequency		0	100		400	KHz
t_{LOW}	Clock Low Period		4.7		1.3		µs
t_{HIGH}	Clock High Period		4.0		0.6		µs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		1.3		µs
$t_{SU:STA}$	Start Condition Setup Time		4.7		0.6		µs
$t_{HD:STA}$	Start Condition Hold Time		4.0		0.6		µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		0.6		µs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	0.2	0.9	µs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		0.2		µs
t_R	SCL and SDA Rise Time			1000		300	ns
t_F	SCL and SDA Fall Time			300		300	ns
$t_{SU:DAT}$	Data In Setup Time		250		100		ns
$t_{HD:DAT}$	Data In Hold Time		0		0		ns
T_I	Noise Spike Width @ SCL, SDA Inputs	Noise Suppression Time Constant		100		100	ns
t_{WR}	Write Cycle Time			10		10	ms

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CAPACITANCE

T_A = 25°C, f = 100KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

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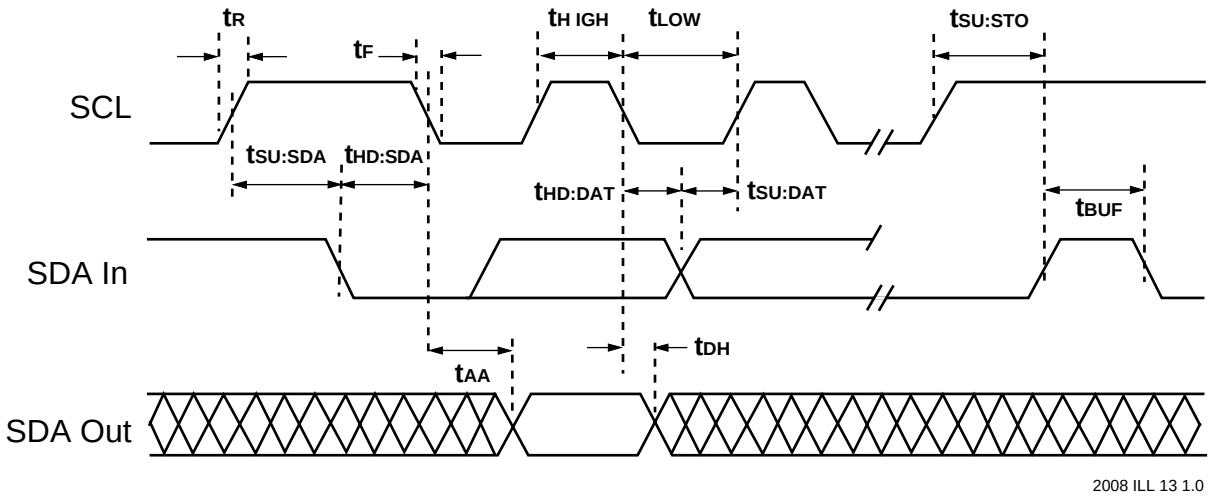


FIGURE 11. BUS TIMING

V_{LOCK} CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C

		S24VP04-2.7		S24VP04–A		S24VP04–B		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
V_{LOCK}	Write Lockout Voltage Level	2.55	2.70	4.25	4.50	4.50	4.75	V
t_{PUW}	Power-Up Write Delay	130	20	130	270	130	270	ms
t_{LDLY}	Delay to $V_{LOCKOUT}$		5		5		5	µs
t_{GLITCH}	Glitch Filter		30		30		30	ns

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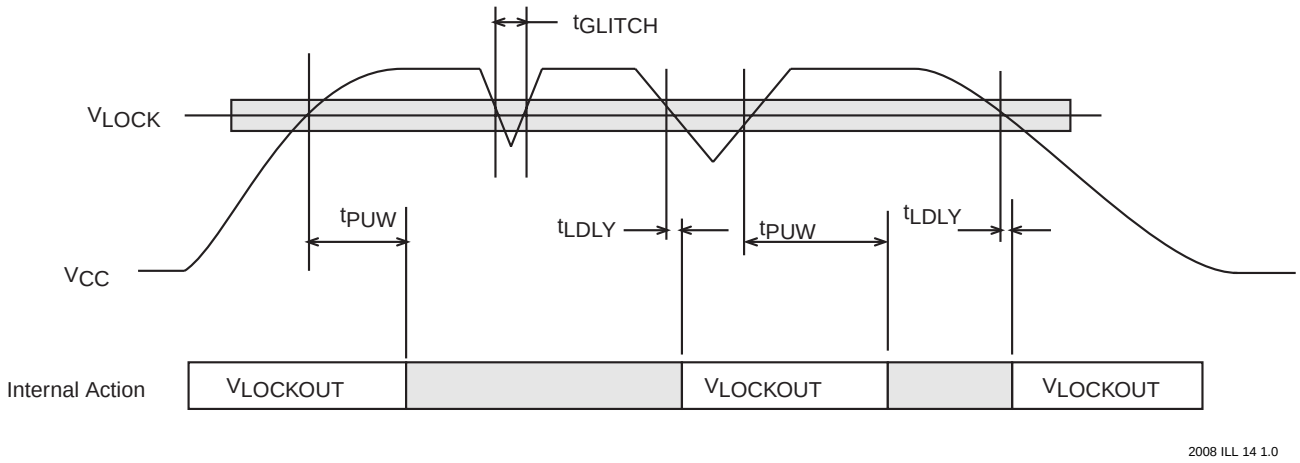
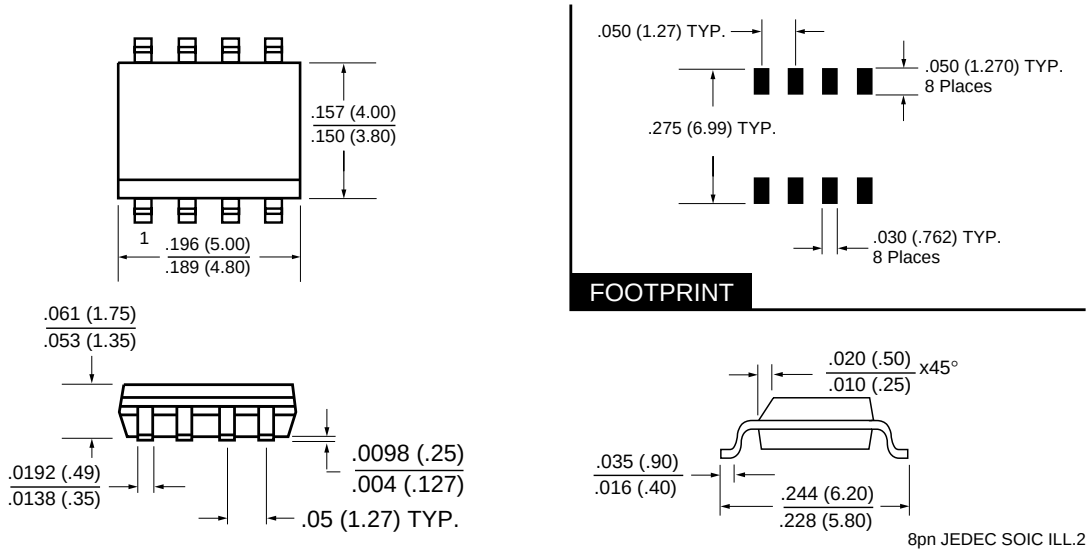
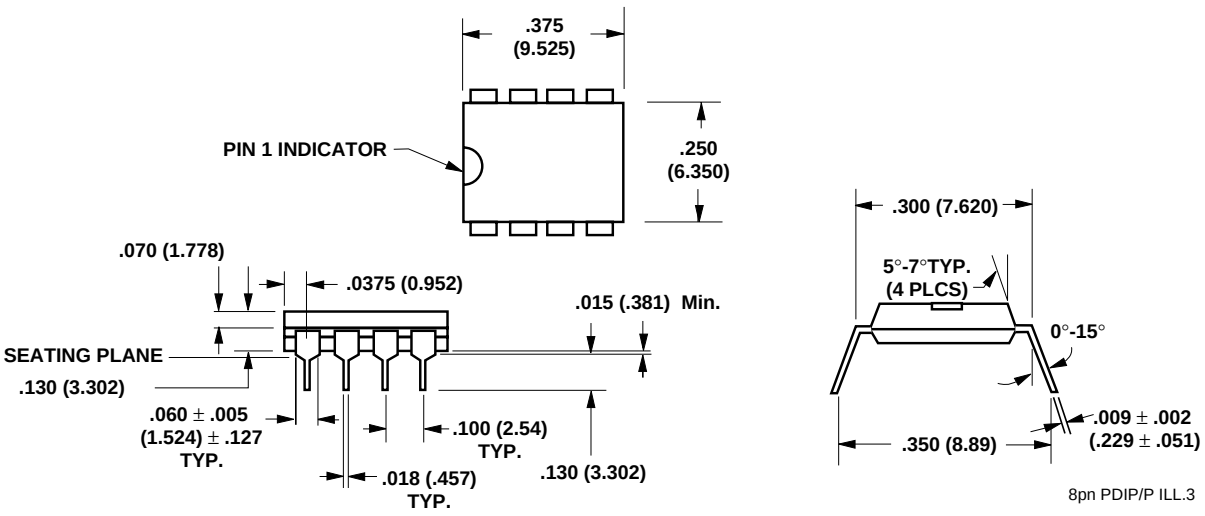


FIGURE 12. V_{LOCK} OUTPUT TIMING

8 Pin SOIC (Type S) Package JEDEC (150 mil body width)



8 Pin PDIP (Type P) Package



8pn PDIP/P ILL.3

ORDERING INFORMATION

S24VP04 P I -2.7 TE7

Base Part Number

Tape and Reel Option
TE7 = 500/reel
TE13 = 2000/reel

Package
P = 8 Lead PDIP
S = 8 Lead 150mil SOIC

Operating Voltage Range
A = 4.5V to 5.5V V_{LOCK} Min. @ 4.25V
B = 4.5V to 5.5V V_{LOCK} Min. @ 4.50V
2.7 = 2.7V to 5.5V V_{LOCK} Min. @ 2.55V

Operating Temperature Range
Blank = 0°C to +70°C
I = -40°C to +85°C

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