S-8533 Series

STEP-DOWN, SYNCHRONOUS PWM CONTROL SWITCHING REGULATOR CONTROLLER

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Rev.3.0_02

The S-8533 Series is a synchronous PWM control CMOS step-down switching regulator controller that includes a reference voltage source, synchronous circuit, oscillation circuit, error amplifier, phase compensation circuit, and PWM controller.
An efficient step-down switching regulator can be realized simply by adding external P-channel and N-channel power MOS FETs, one coil, and three capacitors.
Since the oscillation frequency is a high 300 kHz, the S-8533 can be used to configure a high efficiency step-down switching regulator capable of driving high output current using small external parts and a 3 to 10% increase in efficiency is obtained compared to conventional step-down switching regulators.
The 8-Pin TSSOP package and high oscillation frequency make the S-8533 ideal as the main power supply for portable devices.

■ Features

- Synchronous rectification system realizing high efficiency (typ. 94%)
- Use at maximum duty ratio = 100% and use of a battery up to maximum life is possible by using P-channel and N-channel power MOS FETs externally.
- Oscillation frequency : 300 kHz typ.
- Input voltage : 2.7 to 16.0 V
- Output voltage : 1.25 V
  1.3 to 6.0 V, selectable in 0.1 V steps
- Output voltage accuracy : ±2.0%
- Soft-start function set by an external capacitor (C_{SS})
- Shutdown function
- Lead-free, Sn 100%, halogen-free*1

***1.** Refer to "■ **Product Name Structure**" for details.

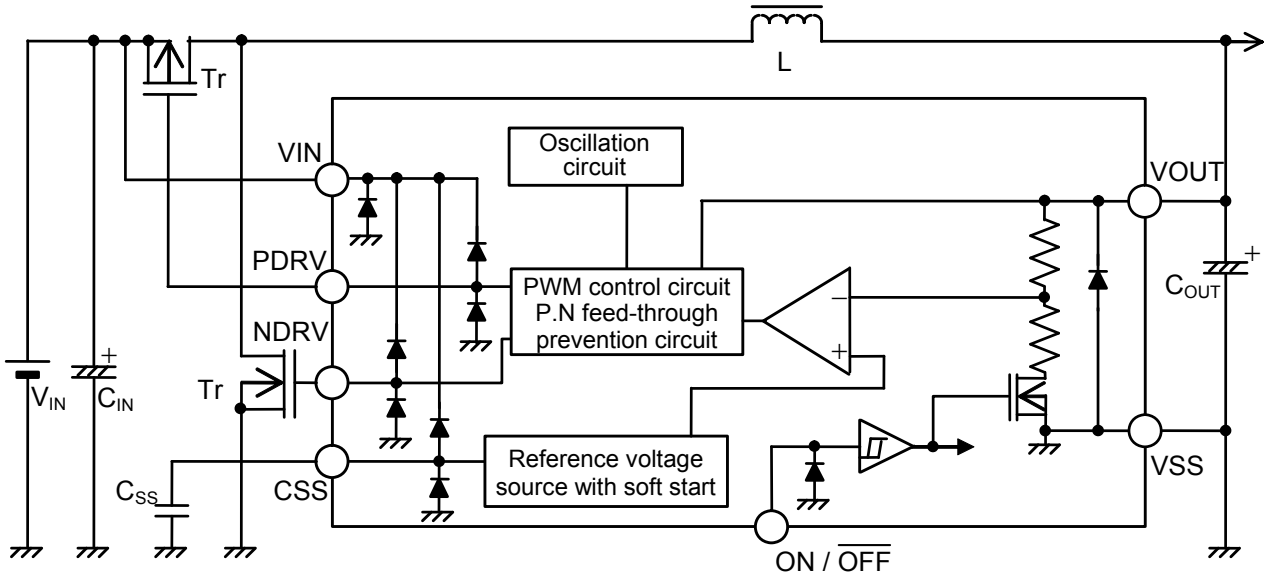
■ Applications

- Constant voltage power supply for hard disks and DVD drivers
- Power supplies for portable devices, such as digital cameras, PDAs, electronic organizers, and cellular phones
- Main or sub power supply for notebook PCs and peripherals
- Constant voltage power supply for cameras, video equipment, and communication equipment

■ Package

- 8-Pin TSSOP

■ Block Diagram



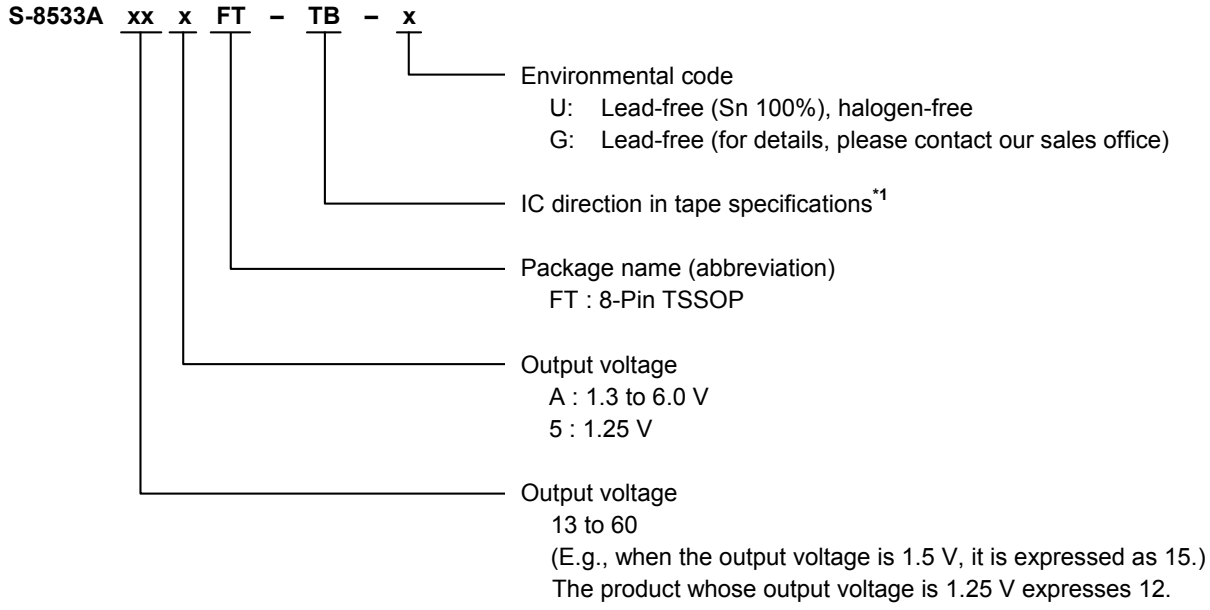
Remark All the diodes in the figure are parasitic diodes.

Figure 1

■ Product Name Structure

The output voltage for the S-8533 Series can be selected depending on usage. Refer to "**1. Product Name**" for the definition of the product name, "**2. Package**" regarding the package drawings and "**3. Product Name List**" for the full product names.

1. Product Name



***1.** Refer to the tape specifications.

2. Package

Package Name		Drawing Code		
		Package	Tape	Reel
8-Pin TSSOP	Environmental code = G	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-SD
	Environmental code = U	FT008-A-P-SD	FT008-E-C-SD	FT008-E-R-S1

3. Product Name List

Output Voltage	Product Name
1.25 V	S-8533A125FT-TB-x
1.3 V	S-8533A13AFT-TB-x
1.4 V	S-8533A14AFT-TB-x
1.5 V	S-8533A15AFT-TB-x
1.8 V	S-8533A18AFT-TB-x
2.5 V	S-8533A25AFT-TB-x
2.7 V	S-8533A27AFT-TB-x
2.8 V	S-8533A28AFT-TB-x
3.0 V	S-8533A30AFT-TB-x
3.3 V	S-8533A33AFT-TB-x
3.9 V	S-8533A39AFT-TB-x
4.1 V	S-8533A41AFT-TB-x
4.5 V	S-8533A45AFT-TB-x
4.8 V	S-8533A48AFT-TB-x
4.9 V	S-8533A49AFT-TB-x
5.0 V	S-8533A50AFT-TB-x
5.2 V	S-8533A52AFT-TB-x
5.5 V	S-8533A55AFT-TB-x
6.0 V	S-8533A60AFT-TB-x

Remark 1. Contact the ABLIC Inc. marketing department for the availability of product samples other than those specified above.
2. x: G or U
3. Please select products of environmental code = U for Sn 100%, halogen-free products.

■ Pin Configurations

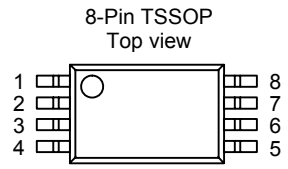


Figure 2

Table 1

Pin No.	Symbol	Pin Description
1	NC*1	No connection
2	VOUT	Output voltage pin
3	ON/$\overline{\text{OFF}}$	Shutdown pin H : Normal operation (step-down operation) L : Step-down operation stopped (all circuits deactivated)
4	CSS	Soft start capacitor connection pin
5	VSS	GND pin
6	NDRV	External N-channel connection pin
7	PDRV	External P-channel connection pin
8	VIN	IC power supply pin

***1.** The NC pin is electrically open. Connection of this pin to VIN or VSS is allowed.

■ Absolute Maximum Ratings

Table 2

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Absolute Maximum Rating	Unit
VIN pin voltage	V_{IN}	V_{SS} − 0.3 to V_{SS} + 18	V
VOUT pin voltage	V_{OUT}	V_{SS} − 0.3 to V_{SS} + 18	V
ON/$\overline{OFF}$ pin voltage	$V_{ON/\overline{OFF}}$	V_{SS} − 0.3 to V_{SS} + 18	V
CSS pin voltage	V_{CSS}	V_{SS} − 0.3 to V_{IN} + 0.3	V
NDRV pin voltage	V_{NDRV}	V_{SS} − 0.3 to V_{IN} + 0.3	V
PDRV pin voltage	V_{PDRV}	V_{SS} − 0.3 to V_{IN} + 0.3	V
NDRV pin current	I_{NDRV}	±100	mA
PDRV pin current	I_{PDRV}	±100	mA
Power dissipation	P_D	300 (When not mounted on board)	mW
		700[*1]	mW
Operating ambient temperature	T_{opr}	−40 to +85	°C
Storage temperature	T_{stg}	−40 to +125	°C

***1.** When mounted on board

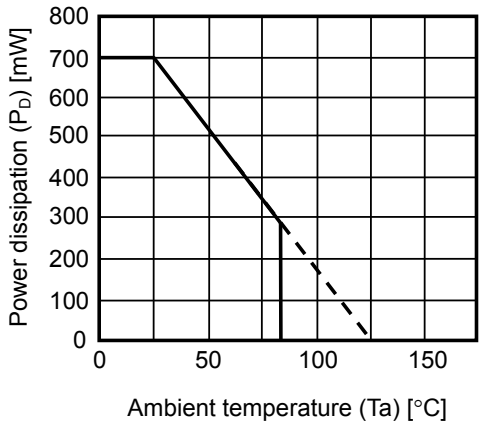
[Mounted board]

(1) Board size : 114.3 mm × 76.2 mm × t1.6 mm

(2) Board name : JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

(1) When mounted on board



(2) When not mounted on board

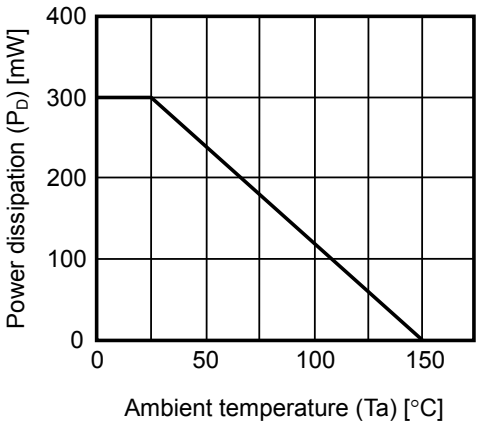


Figure 3 Power Dissipation of Package

■ Electrical Characteristics

Table 3

$V_{IN} = V_{OUT} \times 1.5$ V, $I_{OUT} = V_{OUT}/50$ A (In case $V_{OUT} \leq 1.8$ V, $V_{IN} = 2.7$ V) (Ta = 25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Measurement Circuit
Output voltage*1	$V_{OUT(E)}$	–		$V_{OUT(S)} \times 0.98$	$V_{OUT(S)}$	$V_{OUT(S)} \times 1.02$	V	2
Input voltage	V_{IN}	–		2.7	–	16.0	V	1
Current consumption 1	I_{SS1}	No external parts, $V_{OUT} = V_{OUT(S)} \times 0.95$ (Duty ratio 100%)		–	30	70	μA	1
Current consumption during power-off	I_{SSS}	$V_{ON/\overline{OFF}} = 0$ V		–	–	1.0	μA	1
PDRV pin output current	I_{PDRVH}	No external parts, $V_{OUT} = V_{OUT(S)} \times 1.5$, $V_{IN} = 9.0$ V, $V_{PDRV} = V_{IN} - 0.2$ V		−12	−18	–	mA	1
	I_{PDRVL}	No external parts, $V_{OUT} = V_{OUT(S)} \times 0.95$, $V_{IN} = 9.0$ V, $V_{PDRV} = 0.2$ V		19	27	–	mA	1
NDRV pin output current	I_{NDRVH}	No external parts, $V_{OUT} = V_{OUT(S)} \times 1.5$, $V_{IN} = 9.0$ V, $V_{NDRV} = V_{IN} - 0.2$ V		−10	−14	–	mA	1
	I_{NDRVL}	No external parts, $V_{OUT} = V_{OUT(S)} \times 0.95$, $V_{IN} = 9.0$ V, $V_{NDRV} = 0.2$ V		35	50	–	mA	1
Line regulation	ΔV_{OUT1}	$V_{IN} = V_{OUT(S)} \times 1.2$ to 16 V*2	S-8533A125, S-8533A13A to 29A	–	$V_{OUT(E)} \times 1.0\%$	$V_{OUT(E)} \times 2.5\%$	V	2
			S-8533A30A to 60A	–	$V_{OUT(E)} \times 1.0\%$	$V_{OUT(E)} \times 2.0\%$	V	2
Load regulation	ΔV_{OUT2}	$I_{OUT} = 10$ μA to I_{OUT} (see above) × 1.25		–	$V_{OUT(E)} \times 0.5\%$	$V_{OUT(E)} \times 1.0\%$	V	2
Output voltage temperature coefficient	$\frac{\Delta V_{OUT}}{\Delta Ta \bullet V_{OUT}}$	Ta = −40 to +85°C		–	±100	–	ppm/°C	–
Oscillation frequency	f_{OSC}	Measure waveform at the PDRV pin.		255	300	345	kHz	2
Maximum duty ratio	MaxDuty	The same condition as I_{SS1}. Measure waveform at the PDRV pin.		100	–	–	%	1
VOUT pin input current	I_{VOUT}	$V_{OUT} = 5.0$ V		0.01	0.1	4.0	μA	1
ON/$\overline{OFF}$ pin input voltage	V_{SH}	The same condition as I_{SS1}. $V_{IN} = 2.7$ V and check that PDRV pin = "L".		1.8	–	–	V	1
	V_{SL}	The same condition as I_{SS1}. $V_{IN} = 16.0$ V and check that PDRV pin = "H".		–	–	0.3	V	1
ON/$\overline{OFF}$ pin input leakage current	I_{SH}	The same condition as I_{SS1}. $V_{ON/\overline{OFF}} = V_{IN}$		−0.1	–	0.1	μA	1
	I_{SL}	The same condition as I_{SS1}. $V_{ON/\overline{OFF}} = 0$ V		−0.1	–	0.1	μA	1
Soft-start time	t_{SS}	The same condition as I_{SS1}. Measure time until PDRV pin oscillates.		5.0	8.0	16.0	ms	1
Efficiency	EFFI	***3**, I_{OUT} = 200 to 400 mA, S-8533A33A		–	94	–	%	3

External parts :

Coil :	Sumida Corporation	CD105 (22 μH)
Diode :	Matsushita Electric Industrial Co., Ltd.	MA737 (Schottky diode)
Capacitor :	Nichicon Corporation	F93 (16 V, 47 μF, tantalum) × 2
Transistor :	Toshiba Corporation	2SA1213
Base resistance :	1 kΩ	
Base capacitor :	2200 pF	
C_{SS} :	4700 pF	
C_{NDRV} :	1000 pF	

***1.** $V_{OUT(S)}$: Nominal output voltage value
$V_{OUT(E)}$: Actual output voltage value : $V_{IN} = V_{OUT} \times 1.5$ V, $I_{OUT} = V_{OUT}/50$ A (If $V_{OUT} \leq 1.8$ V, $V_{IN} = 2.7$ V.)

***2.** In case $V_{OUT(S)} \leq 2.2$ V, $V_{IN} = 2.7$ to 16 V

***3.** External parts

Coil :	Sumida Corporation	CDRH104R (22 μH)
Capacitor :	Nichicon Corporation	F93 (16 V, 47 μF, tantalum) × 2
P-channel power MOS FET :	Sanyo Electric Co., Ltd.	CPH6303 (V_{GS} = 10 V max.)
N-channel power MOS FET :	Sanyo Electric Co., Ltd.	CPH6403 (V_{GS} = 10 V max.)
C_{SS} :	4700 pF	

■ Measurement Circuits

1.

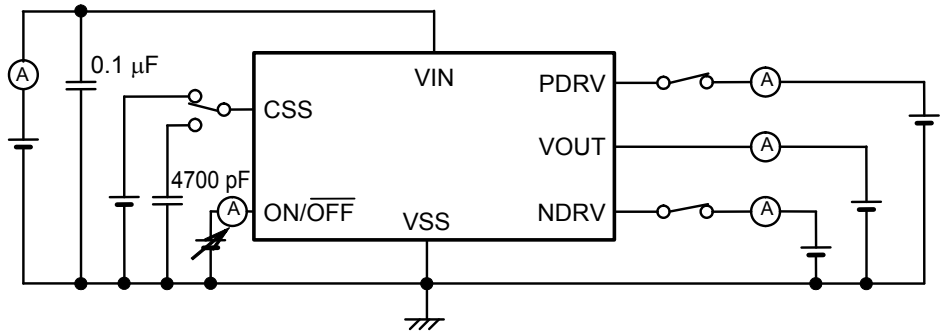


Figure 4

2.

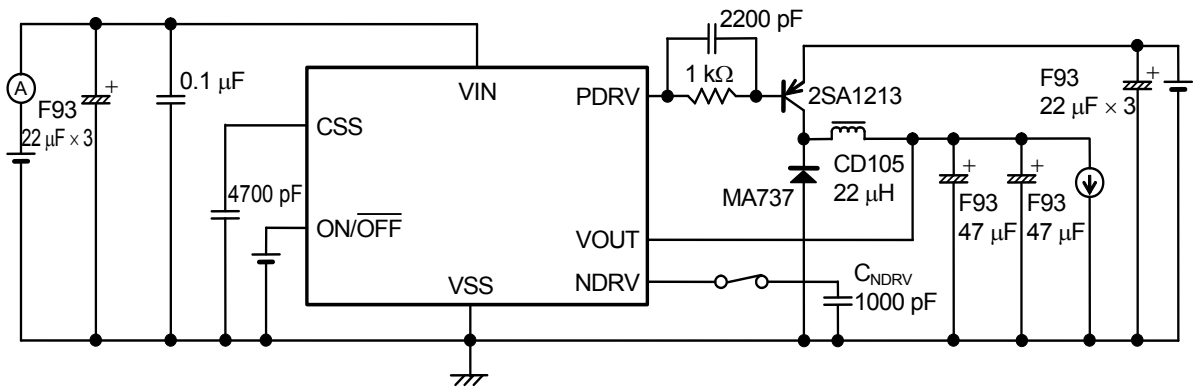


Figure 5

3.

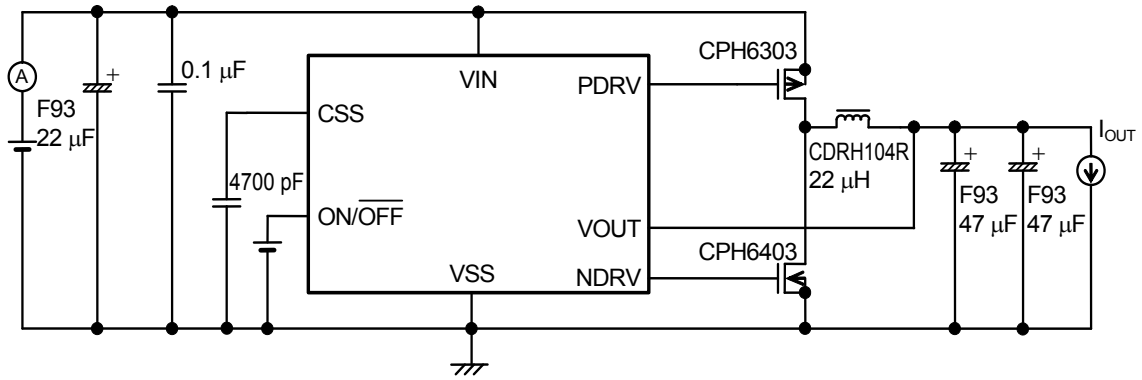


Figure 6

■ Operation

1. Synchronous PWM Control Step-down DC-DC Converter

1. 1 Synchronous Rectification

A synchronous rectifying DC-DC converter enables a greater reduction in the power consumption of the external rectifying element compared with a conventional DC-DC converter. In addition, incorporating a P and N feed-through prevention circuit reduces the feed-through current during operation of external transistors (P-channel and N-channel), making the operating power consumption extremely low.

1. 2 PWM Control

The S-8533 Series is a DC-DC converter that uses pulse width modulation (PWM) and is characterized by its low current consumption.
In conventional modulation PFM system DC-DC converters, pulses are skipped when they are operated with a low output load current, causing variations in the ripple frequency of the output voltage and an increase in the ripple voltage. Both of these effects constitute inherent drawbacks to those converters.
In the S-8533 Series, the pulse width varies in the range from 0 to 100% according to the load current, yet the ripple voltage produced by the switching can easily be eliminated by a filter since the switching frequency is always constant. When the pulse width is 0% (when there is no load or the input voltage is high), current consumption is low since pulses are skipped.

2. Soft-Start Function

The S-8533 Series has a built-in soft-start circuit.
This circuit enables the output voltage (V_{OUT}) to rise gradually over the specified soft-start time (t_{SS}) to suppress the overshooting of the output voltage, when the power is switched on or the ON/$\overline{OFF}$ pin is set “H”.
The soft-start time can be set with an external capacitance (C_{SS}).
The time needed for the output voltage to reach 95% of the set output voltage value is calculated by the following formula.

$$t_{SS}\ [ms] = 0.002 \times C_{SS}\ [pF]$$

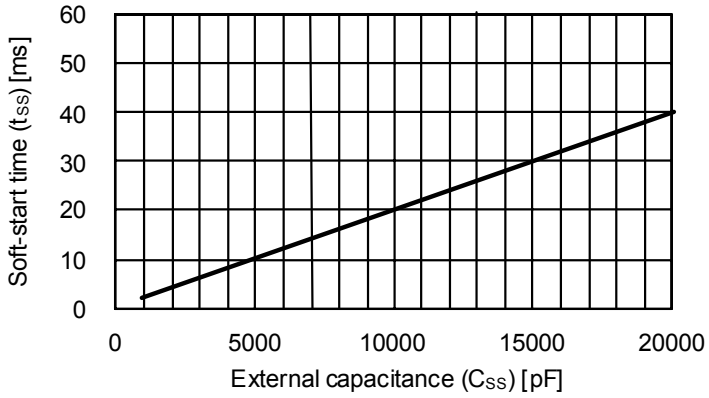
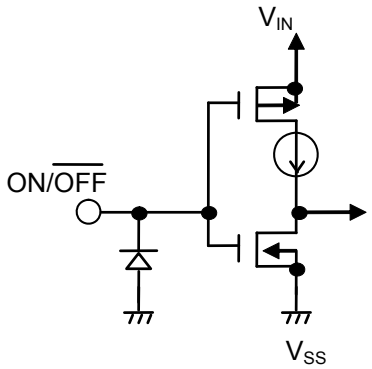


Figure 7 Soft-Start Time

The value for C_{SS} should be selected to give enough margin to the soft-start time against the power supply rise time. If the soft-start time is short, possibility for output voltage overshoot, input current rush, and malfunction of the IC increases.

3. ON/$\overline{\text{OFF}}$ Pin (Shutdown Pin)

This pin is used to activate and deactivate the step-down operation.
When the ON/$\overline{\text{OFF}}$ pin is set to "L", all the internal circuits stop working, and substantial savings in current consumption are thus achieved. The voltage of the PDRV pin goes to V_{IN} level and voltage of the NDRV pin goes to V_{SS} level to shut off the respective transistors.
The ON/$\overline{\text{OFF}}$ pin is configured as shown in **Figure 8**. Since pull-up or pull-down is not performed internally, operation where the ON/$\overline{\text{OFF}}$ pin is in a floating state should be avoided. Application of a voltage of 0.3 to 1.8 V to the pin should also be avoided lest the current consumption increases. When the ON/$\overline{\text{OFF}}$ pin is not used, it should be connected to the VIN pin.



ON/$\overline{\text{OFF}}$ Pin	CR Oscillation Circuit	Output Voltage
"H"	Active	Set value
"L"	Non-active	Open

Figure 8 ON/$\overline{\text{OFF}}$ Pin Structure

4. 100% Duty Cycle

The S-8533 Series operates with a maximum duty cycle of 100%. The switching transistor can be kept on to supply current to the load continually, even in cases where the input voltage falls below the preset output voltage value. The output voltage under these circumstances is equal to the subtraction of the lowering due to the DC resistance of the coil and the on-resistance of the switching transistor from the input voltage.

5. Back-Flow Current

Since the S-8533 Series performs PWM synchronous rectification under a light load, current flows backward in the V_{IN} direction. The back-flow current therefore reaches its peak when there is no load (see **Figure 9**). Pay attention to the maximum back-flow current value, which can be calculated from the following expressions.

Duty (I_{OUT} = 0) = V_{OUT}/V_{IN}

Example : V_{IN} = 5 V, V_{OUT} = 3 V, Duty = 60%

$\Delta I_L = \Delta V/L \times ton = (V_{IN} - V_{OUT}) \times Duty/(L \times f_{OSC}) \times 1.2$

Example : V_{IN} = 5 V, V_{OUT} = 3 V, f_{OSC} = 300 kHz, L = 22 μH, ΔI_L = 218 mA

$I_L max. = \Delta I_L/2$ = 109 mA, $I_L min. = -\Delta I_L/2$ = −109 mA

When there is no load, the current waveform becomes a triangular wave with the maximum, $I_L max.$, and the minimum, $I_L min.$, which is negative. The negative current, shaded regions in **Figure 10**, flows backward.
When the output current (I_{OUT}) is approximately 109 mA under the above conditions, the current does not flow backward since the minimum value ($I_L min$) of the triangular wave becomes 0 mA.
When an input capacitor (C_{IN}) is installed, back-flow current to the power source is negligible since the back-flow current is absorbed by the input capacitor. The input capacitor is indispensable to reduce back-flow current to the power source.

Though the conditions mentioned above are required to prevent back-flow current, they are guidelines. Check the validity by measuring the prototype or the actual device.

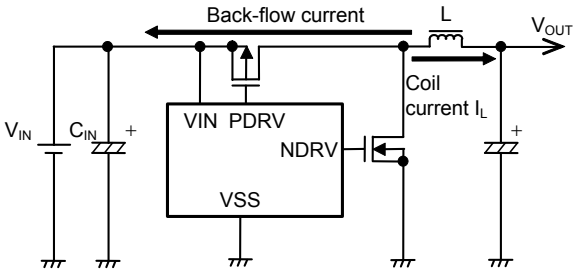


Figure 9 Back-Flow Current

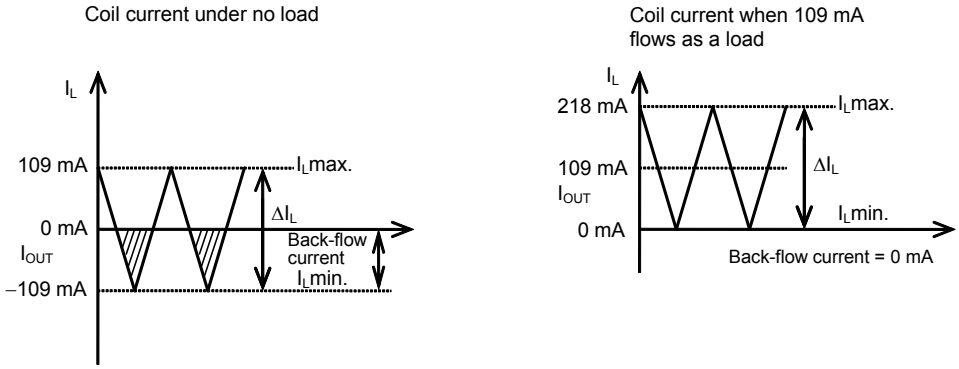


Figure 10 Example for No Back-Flow Current

■ External Parts Selection

1. Inductor

The inductance value (L) greatly affects the maximum output current (I_{OUT}) and the efficiency (η).
As the L value is reduced gradually, the peak current (I_{PK}) increases, the stability of the circuit is improved, and I_{OUT} increases. As the L value is made even smaller, the efficiency is lowered, and I_{OUT} decreases since the current driveability of the switching transistor is insufficient.
As the L value is increased, the dissipation in the switching transistor due to I_{PK} decreases, and the efficiency reaches the maximum at a certain L value. As the L value is made even larger, the efficiency degrades since the dissipation due to the series resistance of the coil increases. I_{OUT} also decreases.
An inductance of 22 μH is recommended for the S-8533 Series.
When choosing an inductor, attention to its allowable current should be paid since the current exceeding the allowable value will cause magnetic saturation in the inductor, leading to a marked decline in efficiency and the breakdown of the IC due to large current.
An inductor should therefore be selected so that I_{PK} does not surpass its allowable current. I_{PK} is expressed by the following equation :

$$I_{PK} = I_{OUT} + \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{2 \times f_{OSC} \times L \times V_{IN}}$$

where f_{OSC} (= 300 kHz) is the oscillation frequency.

2. Capacitors (C_{IN}, C_{OUT})

The capacitor (C_{IN}) inserted on the input side serves to lower the power impedance, average input current, and suppress back-flow current to the power source. Select the C_{IN} value according to the impedance of the power supplied, and select a capacitor that has low ESR (Equivalent Series Resistance) and large capacitance. It should be approximately 47 to 100 μF, although the actual value depends on the impedance of the power source used and load current value. When the input voltage is low and the load is large, the output voltage may become unstable. In this case, increase the input capacitance.
For the output side capacitor (C_{OUT}), select a large capacitance with low ESR (Equivalent Series Resistance) to smoothen the ripple voltage. When the input voltage is extremely high or the load current is extremely large, the output voltage may become unstable. In this case, the unstable area will become narrow by selecting a large capacitance for an output side capacitor. A tantalum electrolytic capacitor is recommended since the unstable area widens when a capacitor with a large ESR, such as an aluminum electrolytic capacitor, or a capacitor with a small ESR, such as a ceramic capacitor, is chosen. The range of the capacitance should generally be approximately 47 to 100 μF.
Fully evaluate input and output capacitors under the actual operating conditions to determine the best value.

3. External Transistor

Enhancement (P-channel, N-channel) MOS FETs can be used as external switching transistors for the S-8533 Series.

3. 1 Enhancement (P-channel, N-channel) MOS FET

The PDRV/NDRV pin of the S-8533 Series is capable of directly driving a P-channel or N-channel MOS FET with a gate capacity around 1000 pF.
When P-channel/N-channel MOS FETs are chosen, efficiency will be 2 to 3% higher than that achieved by a PNP/NPN bipolar transistor since MOS FET switching speeds are higher than PNP/NPN bipolar transistors and power dissipation due to the base current is avoided.
The important parameters in selecting MOS FETs include the threshold voltage, breakdown voltage between gate and source, breakdown voltage between drain and source, total gate capacity, on-resistance, and the current ratings.
The PDRV and NDRV pins swing from voltage V_{IN} over to voltage V_{SS}. If the input voltage is low, a MOS FET with a low threshold voltage has to be used so that the MOS FET will turn on as required. If, conversely, the input voltage is high, select a MOS FET whose gate-source breakdown voltage is higher than the input voltage by at least several volts.
Immediately after the power is turned on, or when the power is turned off (that is, when the step-down operation is terminated), the input voltage will be imposed across the drain and the source of the MOS FET. The transistor therefore needs to have drain-source breakdown voltage that is also several volts higher than the input voltage.
The total gate capacity and the on-resistance affect the efficiency.
The power dissipation for charging and discharging the gate capacity by switching operation will affect the efficiency especially at low load current region when the total gate capacity becomes larger and the input voltage becomes higher. If the efficiency under light loads is a matter of particular concern, select a MOS FET with a small total gate capacity.
In regions where the load current is high, the efficiency is affected by power dissipation caused by the on-resistance of the MOS FET. If the efficiency under heavy loads is particularly important in the application, choose a MOS FET with as low an on-resistance as possible.
As for the current rating, select a MOS FET whose maximum continuous drain current rating is higher than I_{PK}.
If an external P-channel MOS FET has much different characteristics (input capacitance, threshold value, etc.) from an external N-channel MOS FET, they turn ON at the same time, flowing a through current and reducing efficiency.
If a MOS FET with a large input capacitance is used, switching dissipation increases and efficiency decreases. If it is used at several hundreds of mA or more, the dissipation at the MOS FET increases and may exceed the permissible dissipation of the MOS FET. To select P-channel and N-channel MOS FETs, evaluate the performance by testing under the actual condition.

Caution If the load current is large, the P-channel MOS FET dissipation increases and heat is generated. Pay attention to dissipate heat from the P-channel MOS FET.

Efficiency data using Sanyo Electric Co., Ltd. CPH6303, CPH6403, and Vishay Siliconix Si3441DV and Si3442DV for applications with an input voltage range of 6 to 8 V or less is included for reference. For applications with an input voltage range of 6 to 8 V or more, efficiency data using Sanyo Electric Co., Ltd. CPH6302, CHP6402, and Vishay Siliconix Si3454DV and Si3455DV is included. Refer to "■ **Reference Data**".

Current flow in the parasitic diode is not allowed in some MOS FETs. In this case, a Schottky diode must be connected in parallel to the MOS FET. The Schottky diode must have a low forward voltage, a high switching speed, a reverse-direction withstand voltage of V_{IN} or higher, and a current rating of I_{PK} or higher.

■ Standard Circuit

- **Using MOS FET**

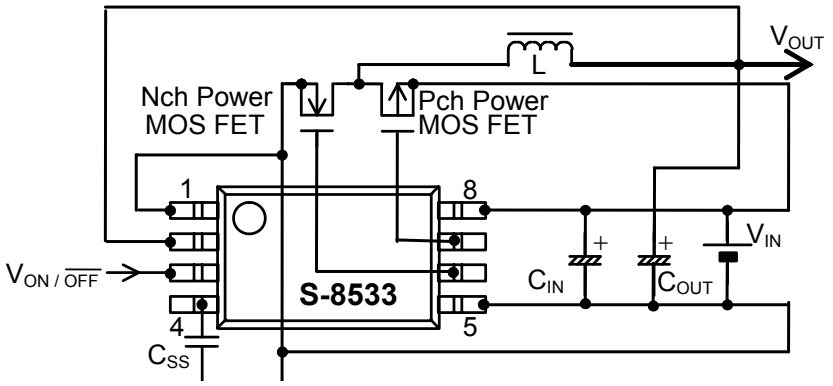


Figure 11

Caution The above connection diagram does not guarantee correct operation. Perform sufficient evaluation using the actual application to set the constants.

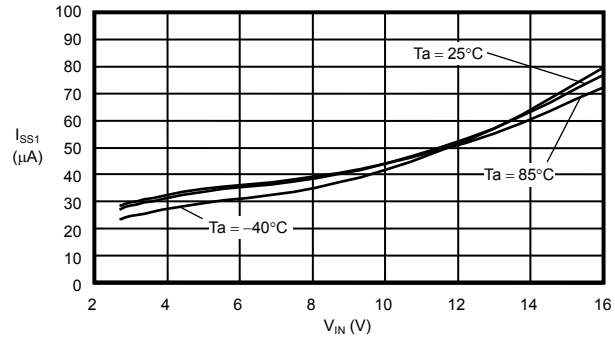
■ Precautions

- Install the external capacitors, diode, coil, and other peripheral parts as close to the IC as possible, and make a one-point grounding.
- Normally, the P-channel and N-channel MOS FETs do not turn ON at the same time. However, if the external P-channel MOS FET has much different characteristics (input capacitance, V_{th}, etc.) from the external N-channel MOS FET, they may turn ON at the same time, flowing a through current. Select P-channel and N-channel transistors with similar characteristics.
- Characteristics ripple voltage and spike noise occur in IC containing switching regulators. Moreover rush current flows at the time of a power supply injection. Because these largely depend on the coil, the capacitor and impedance of power supply used, fully check them using an actually mounted model.
- If the input voltage is high and output current is low, pulses with a low duty ratio may be output, and then the duty ratio may be 0% for several clocks.
- The PDRV and NDRV oscillation frequencies may be an integer fraction of 300 kHz at some input voltage and load conditions. In this case, the ripple voltage may increase.
- The through current prevention circuit reduces through current by shifting the P-channel and N-channel transistor on timing. It does not suppress the through current in the external transistors completely.
- Since PWM synchronous rectification is performed even when the load is light, current flows back to V_{IN}. Check whether the back-flow occurs and whether it affects the performance. (See "**5. Back-Flow Current**" in "■ **Operation**".)
- The PDRV or NDRV oscillation frequency may vary in a voltage range, depending on input voltage.
- When decreasing the power supply voltage slowly, the IC operation may be undefined if the voltage falls below the minimum operating voltage.
- Make sure that dissipation of the switching transistor especially at high temperature will not surpass the power dissipation of the package.
- Switching regulator performance varies depending on the design of PCB patterns, peripheral circuits and parts. Thoroughly evaluate the actual device when setting. When using parts other than those which are recommended, contact the ABLIC Inc. marketing department.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

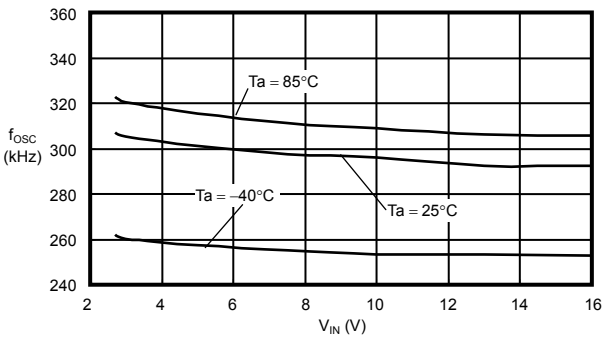
■ Characteristics (Typical Data)

1. Examples of Major Characteristics

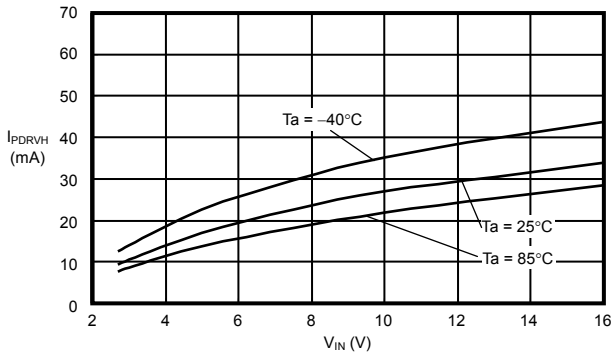
(1) Current Consumption 1 (I_{SS1}) vs. Input Voltage (V_{IN})



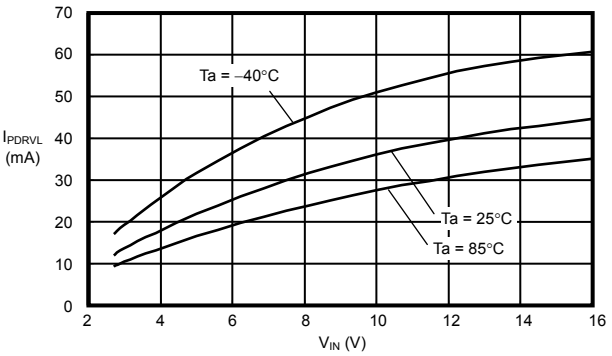
(2) Oscillation Frequency (f_{OSC}) vs. Input Voltage (V_{IN})



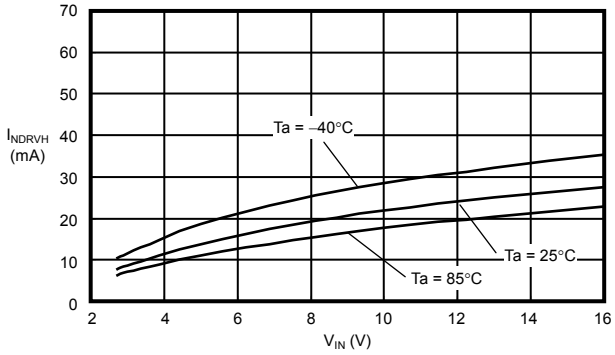
(3) PDRV Pin Output Current "H" (I_{PDRVH}) vs. Input Voltage (V_{IN})



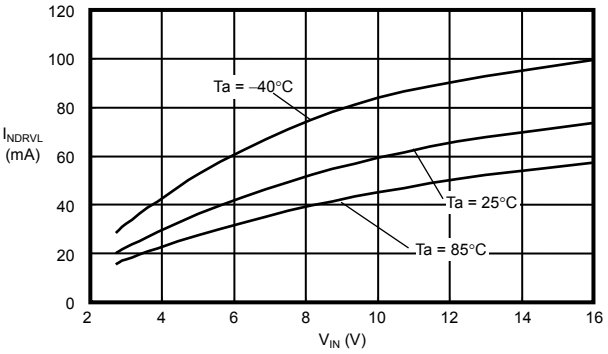
(4) PDRV Pin Output Current "L" (I_{PDRVL}) vs. Input Voltage (V_{IN})



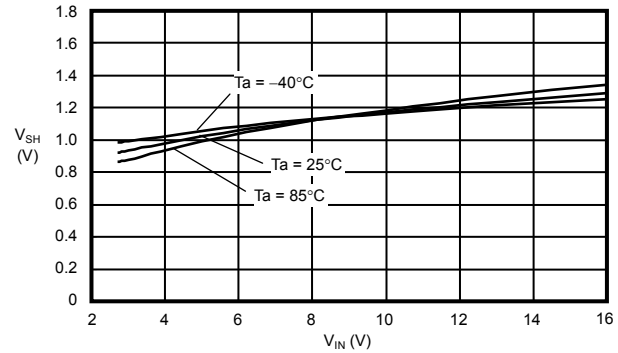
(5) NDRV Pin Output Current "H" (I_{NDRVH}) vs. Input Voltage (V_{IN})



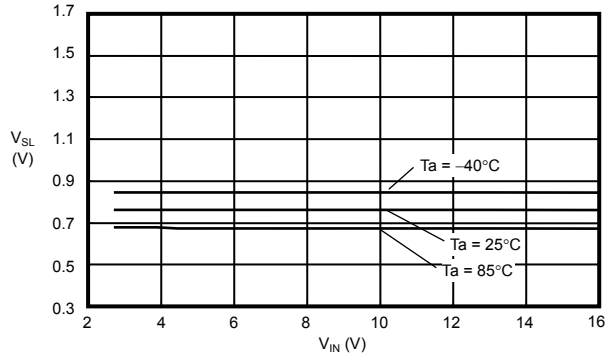
(6) NDRV Pin Output Current "L" (I_{NDRVL}) vs. Input Voltage (V_{IN})



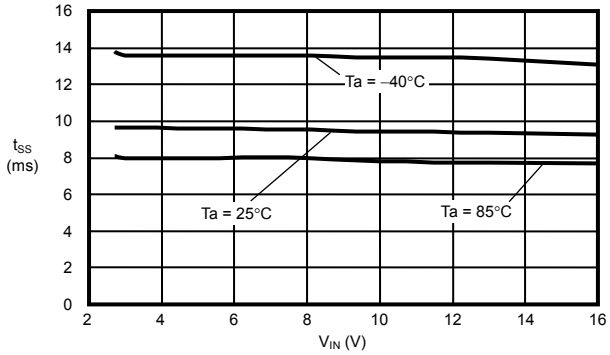
(7) ON/$\overline{\text{OFF}}$ Pin Input Voltage "H" (V_{SH}) vs. Input Voltage (V_{IN})



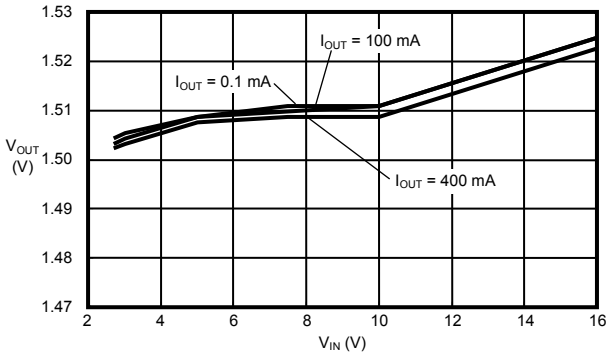
(8) ON/$\overline{\text{OFF}}$ Pin Input Voltage "L" (V_{SL}) vs. Input Voltage (V_{IN})



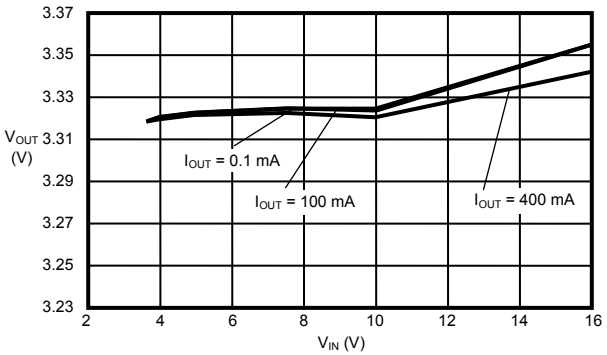
(9) Soft-Start Time (t_{SS}) vs. Input Voltage (V_{IN})



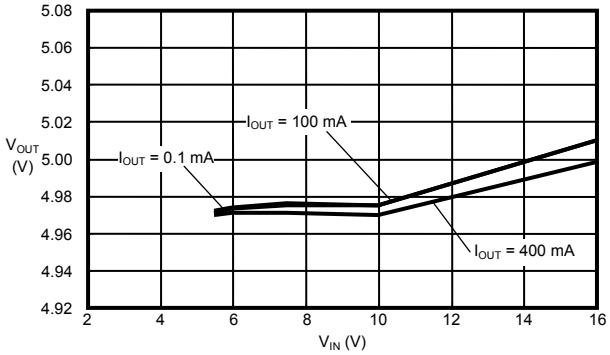
(10) Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) (1.5 V : S-8533A15AFT)



(11) Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) (3.3 V : S-8533A33AFT)



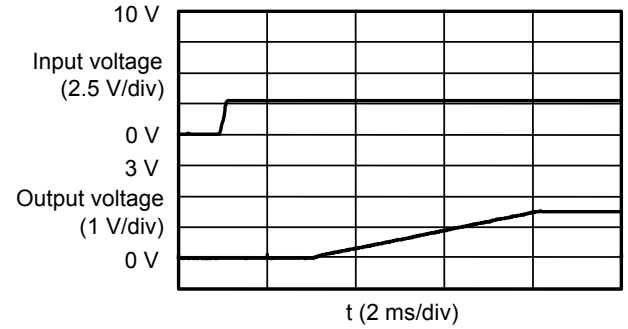
(12) Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) (5.0 V : S-8533A50AFT)



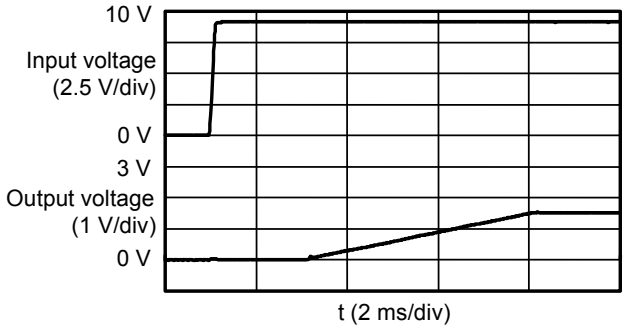
2. Examples of Transient Response Characteristics

(1) Power-on (V_{IN} : 0 V → 2.7 V or 5.0 V or 7.5 V, 0 V → 9.0 V, I_{OUT} : 10 mA)

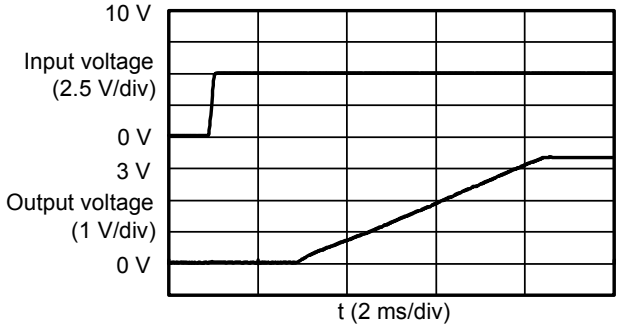
S-8533A15AFT (V_{IN} : 0 V → 2.7 V)



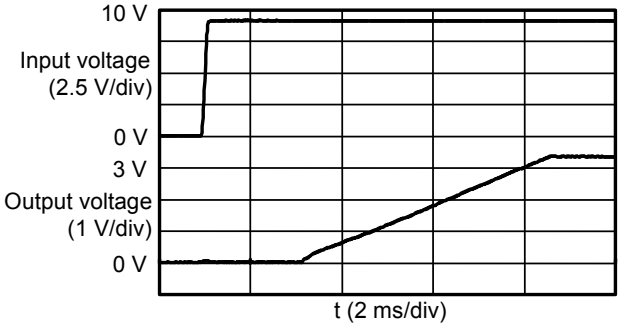
S-8533A15AFT (V_{IN} : 0 V → 9.0 V)



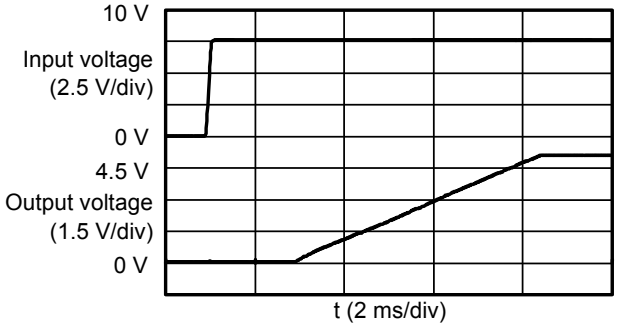
S-8533A33AFT (V_{IN} : 0 V → 5.0 V)



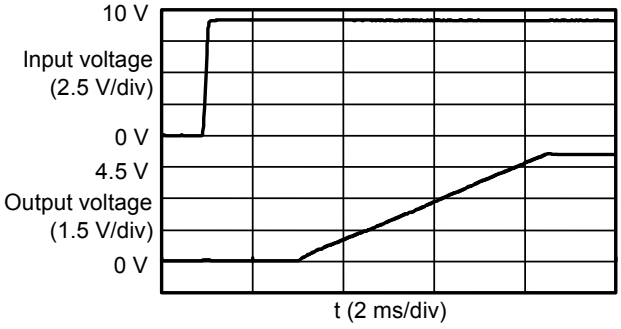
S-8533A33AFT (V_{IN} : 0 V → 9.0 V)



S-8533A50AFT (V_{IN} : 0 V → 7.5 V)

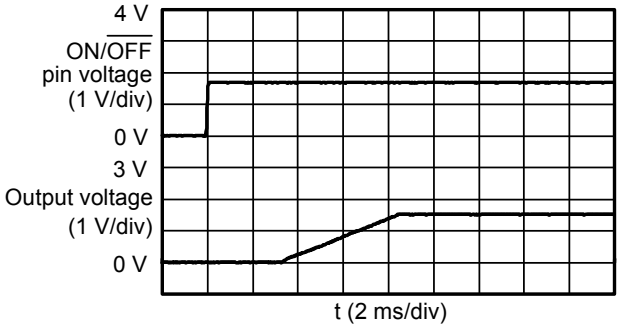


S-8533A50AFT (V_{IN} : 0 V → 9.0 V)

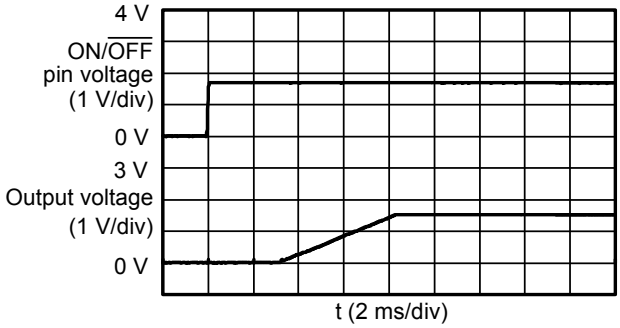


(2) ON/$\overline{\text{OFF}}$ Pin Response ($V_{ON/\overline{OFF}}$: 0 V → 1.8 V, I_{OUT} : 10 mA)

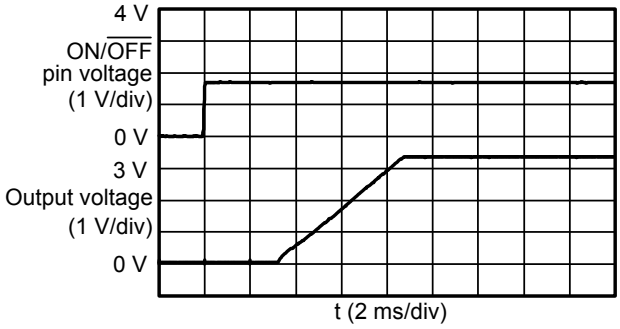
S-8533A15AFT (V_{IN} : 2.7 V)



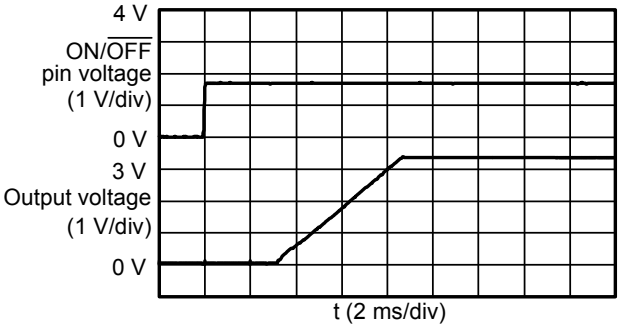
S-8533A15AFT (V_{IN} : 9.0 V)



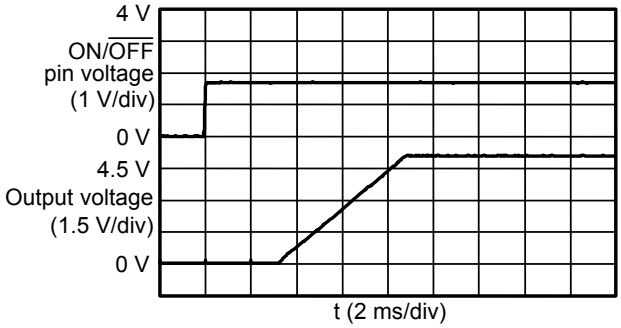
S-8533A33AFT (V_{IN} : 5.0 V)



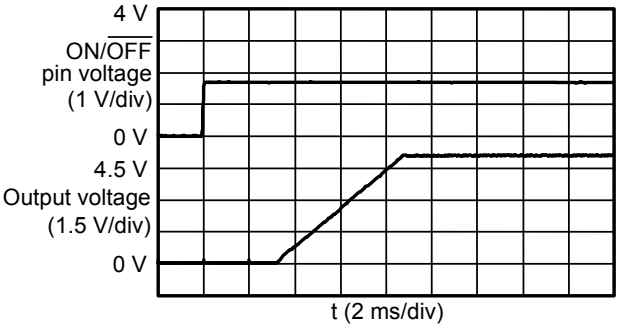
S-8533A33AFT (V_{IN} : 9.0 V)



S-8533A50AFT (V_{IN} : 7.5 V)

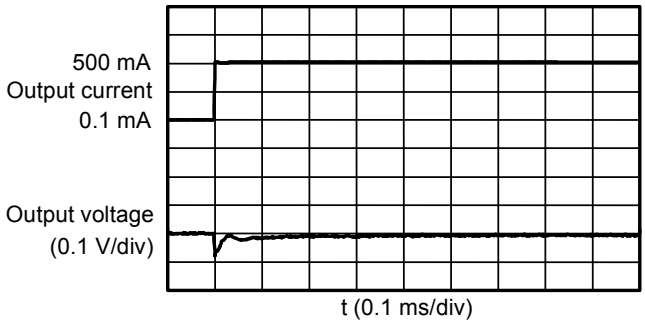


S-8533A50AFT (V_{IN} : 9.0 V)

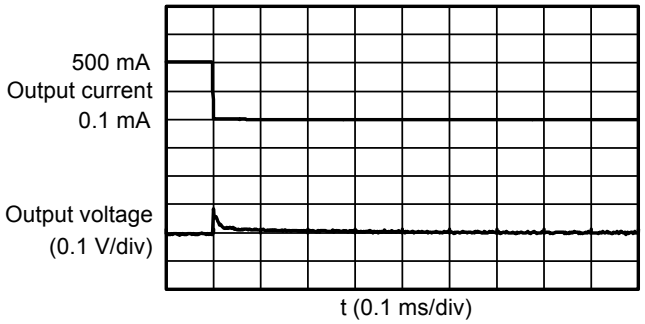


(3) Load Fluctuations (I_{OUT} : 0.1 mA → 500 mA, 500 mA → 0.1 mA, V_{IN} : 2.7 V or 5.0 V or 7.5 V)

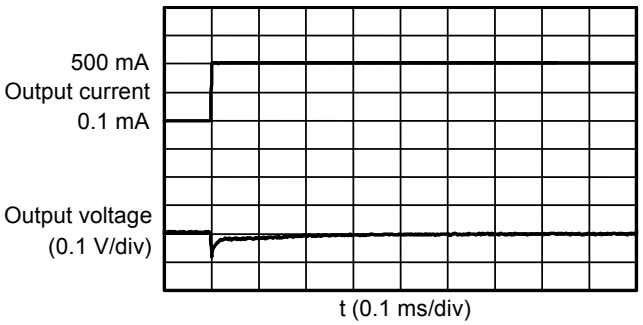
S-8533A15AFT (V_{IN} : 2.7 V)



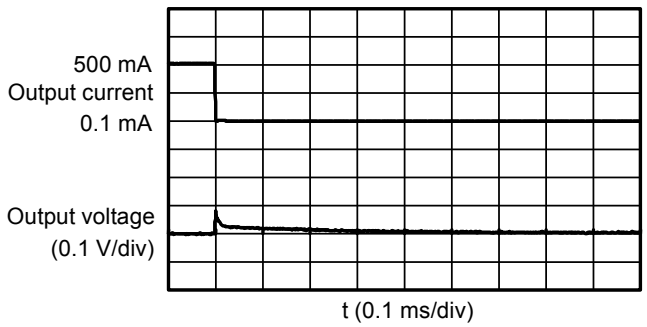
S-8533A15AFT (V_{IN} : 2.7 V)



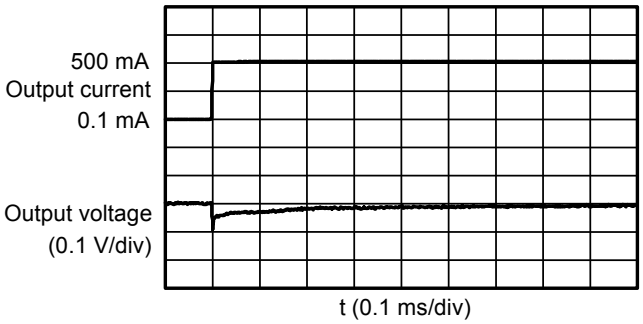
S-8533A33AFT (V_{IN} : 5.0 V)



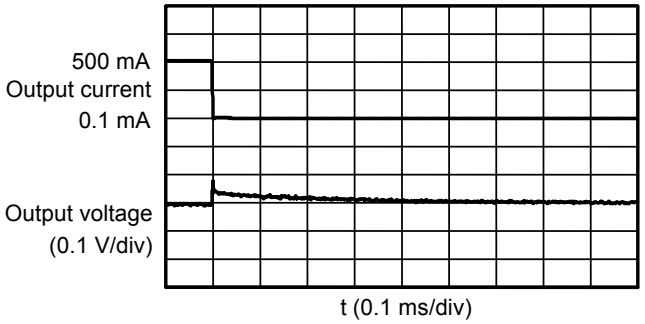
S-8533A33AFT (V_{IN} : 5.0 V)



S-8533A50AFT (V_{IN} : 7.5 V)

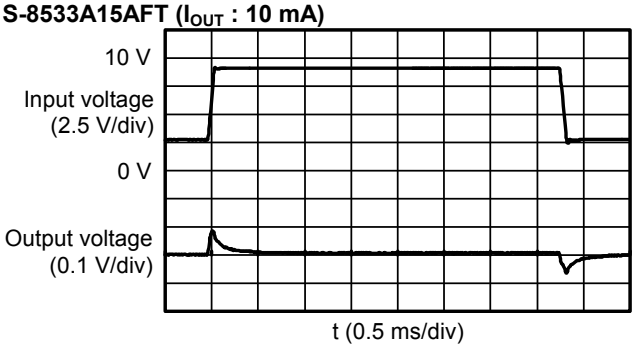


S-8533A50AFT (V_{IN} : 7.5 V)

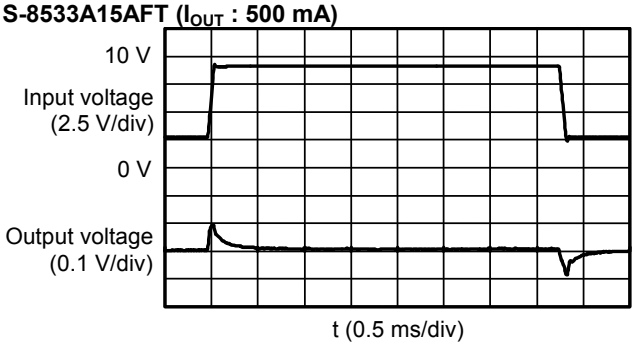


(4) Input Voltage Fluctuations (V_{IN} : 2.7 V → 9.0 V → 2.7 V, 5.0 V → 9.0 V → 5.0 V, 7.5 V → 9.0 V → 7.5 V)

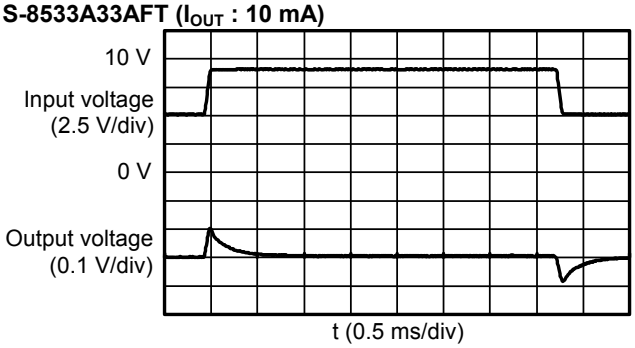
S-8533A15AFT (I_{OUT} : 10 mA)



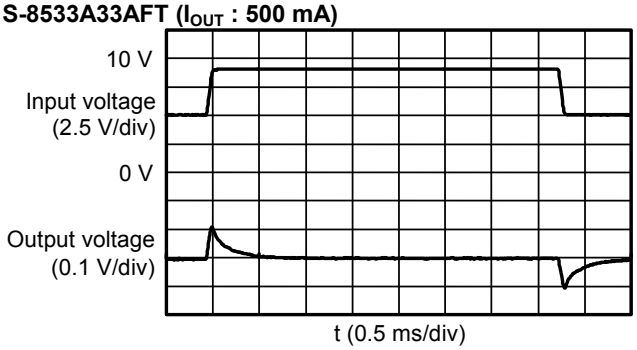
S-8533A15AFT (I_{OUT} : 500 mA)



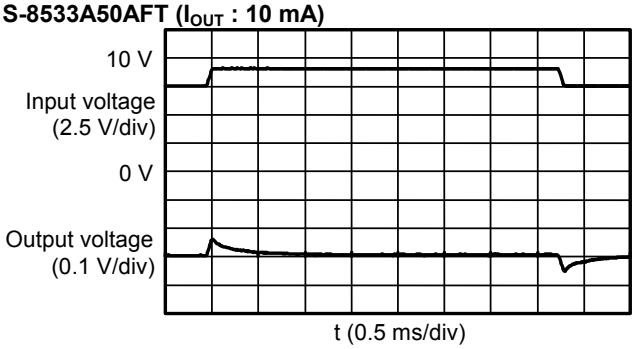
S-8533A33AFT (I_{OUT} : 10 mA)



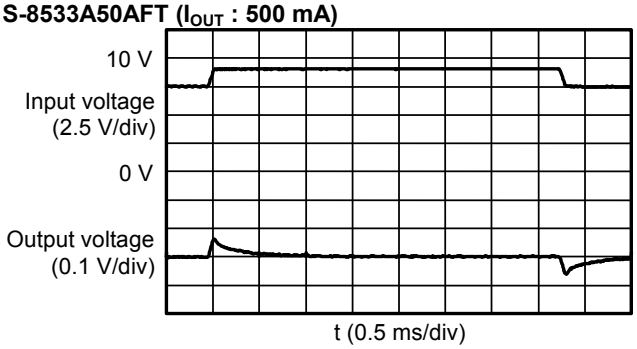
S-8533A33AFT (I_{OUT} : 500 mA)



S-8533A50AFT (I_{OUT} : 10 mA)



S-8533A50AFT (I_{OUT} : 500 mA)



■ Reference Data

Reference data are intended for use in selecting peripheral parts to the IC. The information therefore provides characteristic data in which external parts are selected with a view of wide variety of IC applications. All data show typical values.

1. External Parts for Reference Data

Table 4 External Parts List for Output Current vs. Efficiency Characteristics

No.	Product Name	Output Voltage	Inductor	Transistor P-channel	Transistor N-channel	Output Capacitor	Input Capacitor	Application Condition
(1)	S-8533A15AFT	1.5 V	CDRH104R/22 μH	CPH6303	CPH6403	47 μF × 2	47 μF, 0.1 μF	$I_{OUT} \leq 2$ A, $V_{IN} \leq 8$ V
(2)				Si3441DV	Si3442DV			$I_{OUT} \leq 1.4$ A, $V_{IN} \leq 6$ V
(3)	S-8533A33AFT	3.3 V		CPH6303	CPH6403			$I_{OUT} \leq 2$ A, $V_{IN} \leq 8$ V
(4)				Si3441DV	Si3442DV			$I_{OUT} \leq 1.4$ A, $V_{IN} \leq 6$ V
(5)				CPH6302	CPH6402			$I_{OUT} \leq 2$ A, $V_{IN} \leq 16$ V
(6)				Si3455DV	Si3454DV			$I_{OUT} \leq 1.6$ A, $V_{IN} \leq 16$ V
(7)	S-8533A50AFT	5.0 V		CPH6302	CPH6402			$I_{OUT} \leq 2$ A, $V_{IN} \leq 16$ V
(8)				Si3455DV	Si3454DV			$I_{OUT} \leq 1.6$ A, $V_{IN} \leq 16$ V
(9)	S-8533A15AFT	1.5 V	CDRH104R/47 μH	CPH6303	CPH6403			$I_{OUT} \leq 2$ A, $V_{IN} \leq 8$ V
(10)				Si3441DV	Si3442DV			$I_{OUT} \leq 1.4$ A, $V_{IN} \leq 6$ V
(11)	S-8533A33AFT	3.3 V		CPH6303	CPH6403			$I_{OUT} \leq 2$ A, $V_{IN} \leq 8$ V
(12)				Si3441DV	Si3442DV			$I_{OUT} \leq 1.4$ A, $V_{IN} \leq 6$ V
(13)				CPH6302	CPH6402			$I_{OUT} \leq 2$ A, $V_{IN} \leq 16$ V
(14)				Si3455DV	Si3454DV			$I_{OUT} \leq 1.6$ A, $V_{IN} \leq 16$ V
(15)	S-8533A50AFT	5.0 V		CPH6302	CPH6402			$I_{OUT} \leq 2$ A, $V_{IN} \leq 16$ V
(16)				Si3455DV	Si3454DV			$I_{OUT} \leq 1.6$ A, $V_{IN} \leq 16$ V
(17)	S-8533A15AFT	1.5 V	CDRH104R/10 μH	CPH6303	CPH6403			$I_{OUT} \leq 2$ A, $V_{IN} \leq 8$ V
(18)				Si3441DV	Si3442DV			$I_{OUT} \leq 1.4$ A, $V_{IN} \leq 6$ V
(19)	S-8533A33AFT	3.3 V		CPH6303	CPH6403			$I_{OUT} \leq 2$ A, $V_{IN} \leq 8$ V
(20)				Si3441DV	Si3442DV			$I_{OUT} \leq 1.4$ A, $V_{IN} \leq 6$ V
(21)				CPH6302	CPH6402			$I_{OUT} \leq 2$ A, $V_{IN} \leq 16$ V
(22)				Si3455DV	Si3454DV			$I_{OUT} \leq 1.6$ A, $V_{IN} \leq 16$ V
(23)	S-8533A50AFT	5.0 V		CPH6302	CPH6402			$I_{OUT} \leq 2$ A, $V_{IN} \leq 16$ V
(24)				Si3455DV	Si3454DV			$I_{OUT} \leq 1.6$ A, $V_{IN} \leq 16$ V
(25)	S-8533A33AFT	3.3 V	CDRH125/10 μH	CPH6303	CPH6403			$I_{OUT} \leq 3$ A, $V_{IN} \leq 8$ V
(26)				CPH6302	CPH6402			$I_{OUT} \leq 3$ A, $V_{IN} \leq 16$ V

External Parts List for Ripple Data

Table 5 External Parts for Input Voltage vs. Ripple Voltage Characteristics Data

No.	Product Name	Output Voltage	Inductor	Transistor P-channel	Transistor N-channel	Output Capacitor	Input Capacitor	Application Condition
(27)	S-8533A15AFT	1.5 V	CDRH104R/22 μH	CPH6303	CPH6403	47 μF × 2	47 μF, 0.1 μF	$I_{OUT} \leq 2$ A, $V_{IN} \leq 8$ V
(28)				Si3441DV	Si3442DV			$I_{OUT} \leq 1.4$ A, $V_{IN} \leq 6$ V
(29)	S-8533A33AFT	3.3 V		CPH6303	CPH6403			$I_{OUT} \leq 2$ A, $V_{IN} \leq 8$ V
(30)				Si3441DV	Si3442DV			$I_{OUT} \leq 1.4$ A, $V_{IN} \leq 6$ V
(31)				CPH6302	CPH6402			$I_{OUT} \leq 2$ A, $V_{IN} \leq 16$ V
(32)				Si3455DV	Si3454DV			$I_{OUT} \leq 1.6$ A, $V_{IN} \leq 16$ V
(33)	S-8533A50AFT	5.0 V		CPH6302	CPH6402			$I_{OUT} \leq 2$ A, $V_{IN} \leq 16$ V
(34)				Si3455DV	Si3454DV			$I_{OUT} \leq 1.6$ A, $V_{IN} \leq 16$ V

Performance Data for Parts

The following shows the performance of external parts.

Table 6 Performance of External Parts

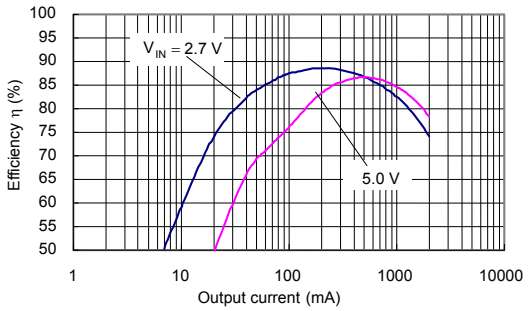
Parts	Product Name	Manufacturer	Characteristics				
Inductor	CDRH125	Sumida Corporation	L Value	DC Resistance	Maximum Current	Diameter	Height
			10 μH	0.019 Ω	4.0 A	12.0 mm typ. 12.3 mm max.	8.0 mm max.
	CDRH104R		47 μH	0.095 Ω	1.9 A	10.2 mm typ. 10.5 mm max.	4.0 mm max.
			22 μH	0.054 Ω	2.5 A		
			10 μH	0.026 Ω	3.8 A		
Diode	MA737	Matsushita Electric Industrial Co., Ltd	Forward current 1.5 A (@V_F = 0.5 V)				
Output Capacity	F93	Nichicon Corporation					
External transistor (P-channel FET)	CPH6303	Sanyo Electric Co., Ltd	V_{GS} = 10 V max., I_D = −4 A max., V_{th} = −0.4 V min., C_{iss} = 820 pF typ., $R_{DS(ON)}$ = 0.090 Ω max. (V_{GS} = −4 V), CPH6 package				
	CPH6302		V_{GS} = 20 V max., I_D = −3 A max., V_{th} = −1.0 V min., C_{iss} = 300 pF typ., $R_{DS(ON)}$ = 0.145 Ω max. (V_{GS} = −10 V), CPH6 package				
	Si3441DV	Vishay Silliconix	V_{GS} = 8 V max., I_D = −3.3 A max., V_{th} = −0.45 V min., $R_{DS(ON)}$ = 0.10 Ω max. (V_{GS} = −4.5 V), TSOP-6 package				
	Si3455DV		V_{GS} = 20 V max., I_D = −3.5 A max., V_{th} = −1.0 V min., $R_{DS(ON)}$ = 0.100 Ω max. (V_{GS} = −10 V), TSOP-6 package				
External transistor (N-channel FET)	CPH6403	Sanyo Electric Co., Ltd	V_{GS} = 10 V max., I_D = 6 A max., V_{th} = 0.4 V min., C_{iss} = 700 pF typ., $R_{DS(ON)}$ = 0.038 Ω max. (V_{GS}= 4 V), CPH6 package				
	CPH6402		V_{GS} = 24 V max., I_D = 4 A max., V_{th} = 1.0 V min., C_{iss} = 240 pF typ., $R_{DS(ON)}$ = 0.75 Ω max. (V_{GS}= 10 V), CPH6 package				
	Si3442DV	Vishay Silliconix	V_{GS} = 8 V max., I_D = 4.0 A max., V_{th} = 0.6 V min., $R_{DS(ON)}$ = 0.07 Ω max. (V_{GS} = 4.5 V), TSOP-6 package				
	Si3454DV		V_{GS} = 20 V max., I_D = 4.2 A max., V_{th} = 1.0 V min., $R_{DS(ON)}$ = 0.065 Ω max. (V_{GS} = 10 V), TSOP-6 package				

Caution The value of each characteristic in Table 6 depends on the materials prepared by each manufacturer, however, confirm the specifications by referring to respective materials when using any of the above.

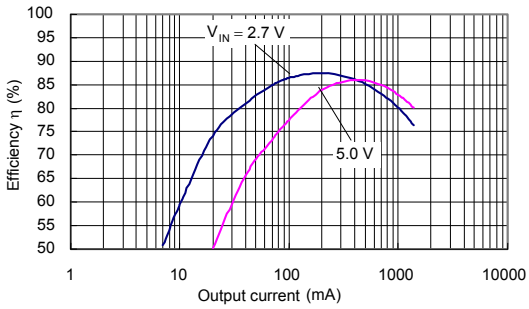
2. Output Current (I_{OUT}) vs. Efficiency (η) Characteristics

The following shows the actual output current (I_{OUT}) vs. efficiency (η) characteristics when the S-8533 Series is used under conditions (1) to (26) in **Table 4**.

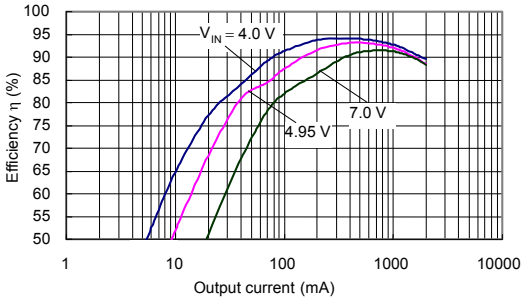
(1) S-8533A15AFT (CPH6303/CPH6403)



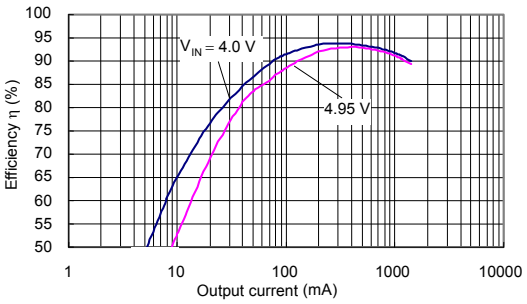
(2) S-8533A15AFT (Si3441DV/Si3442DV)



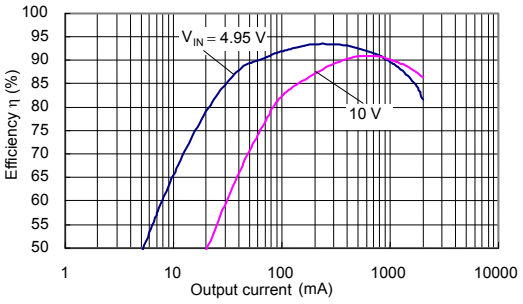
(3) S-8533A33AFT (CPH6303/CPH6403)



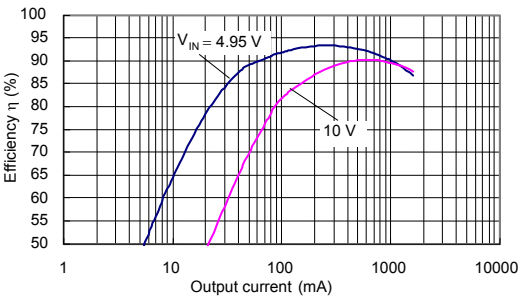
(4) S-8533A33AFT (Si3441DV/Si3442DV)



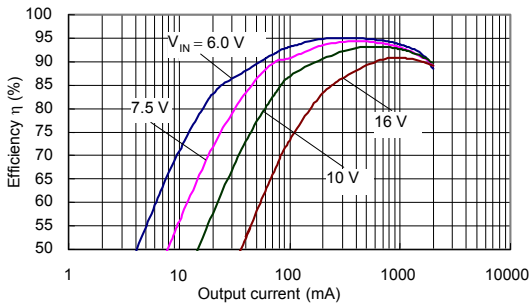
(5) S-8533A33AFT (CPH6302/CPH6402)



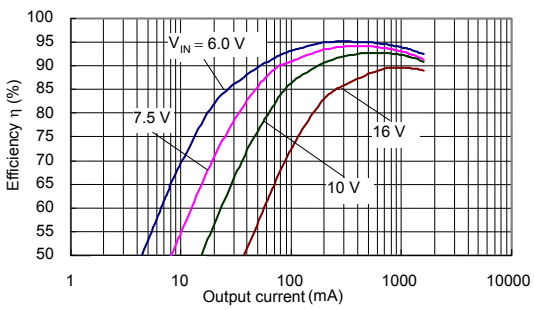
(6) S-8533A33AFT (Si3454DV/Si3455DV)



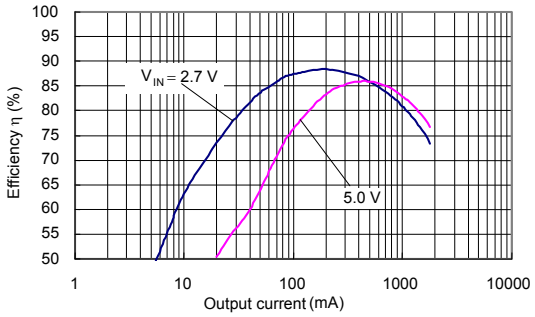
(7) S-8533A50AFT (CPH6302/CPH6402)



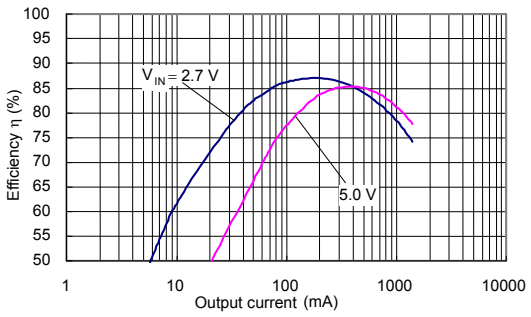
(8) S-8533A50AFT (Si3454DV/Si3455DV)



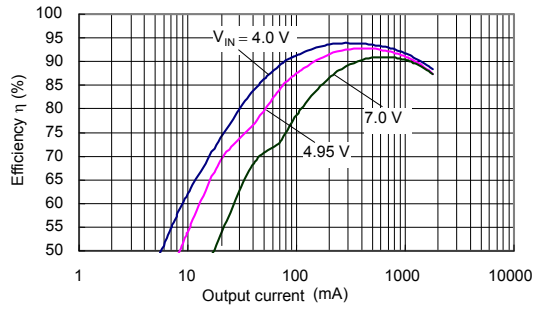
(9) S-8533A15AFT (CPH6303/CPH6403)



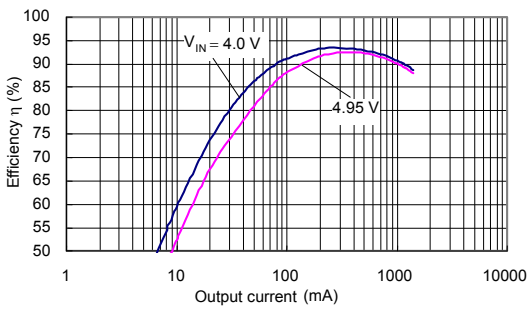
(10) S-8533A15AFT (Si3441DV/Si3442DV)



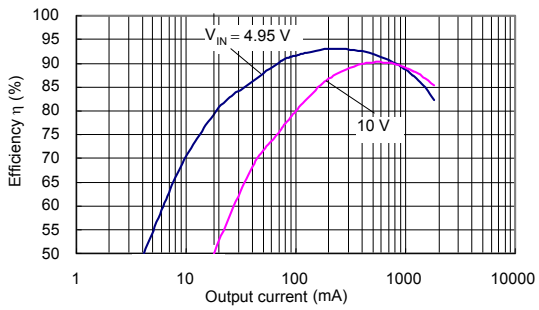
(11) S-8533A33AFT (CPH6303/CPH6403)



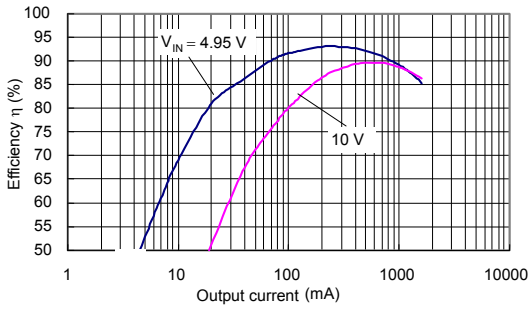
(12) S-8533A33AFT (Si3441DV/Si3442DV)



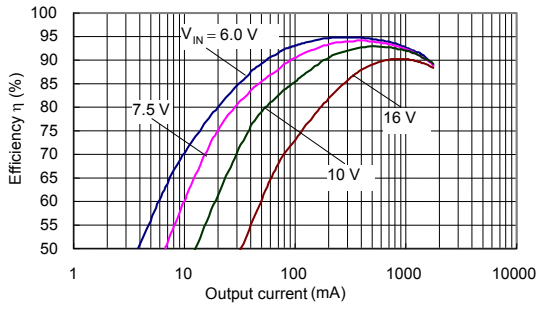
(13) S-8533A33AFT (CPH6302/CPH6402)



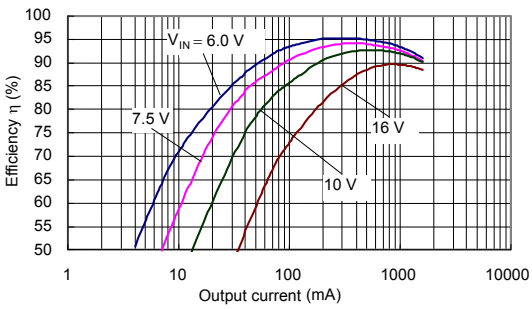
(14) S-8533A33AFT (Si3454DV/Si3455DV)



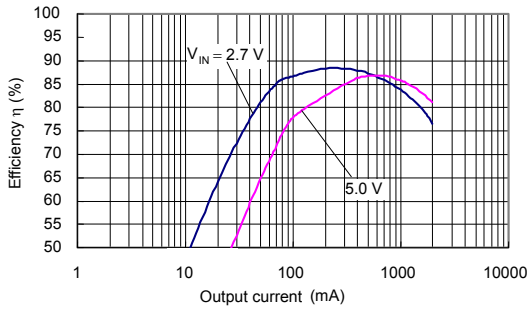
(15) S-8533A50AFT (CPH6302/CPH6402)



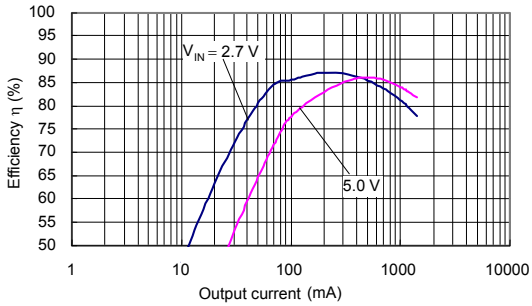
(16) S-8533A50AFT (Si3454DV/Si3455DV)



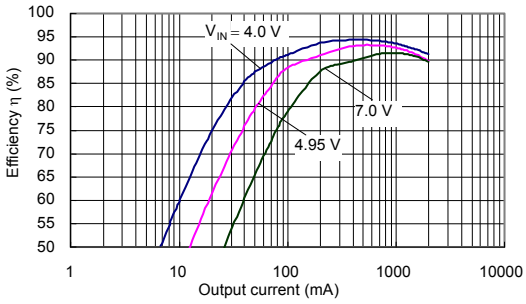
(17) S-8533A15AFT (CPH6303/CPH6403)



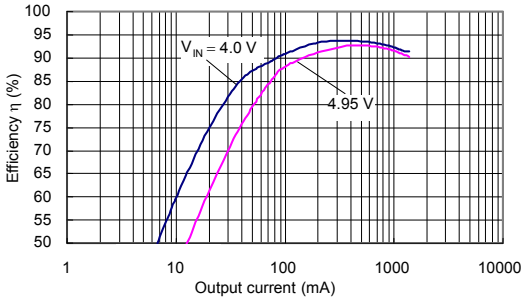
(18) S-8533A15AFT (Si3441DV/Si3442DV)



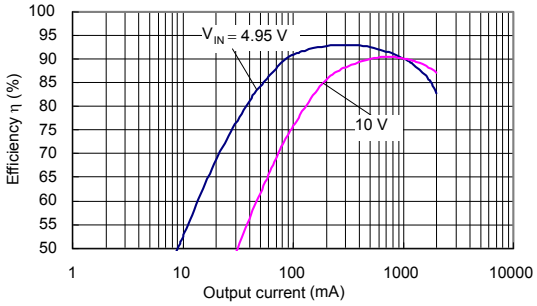
(19) S-8533A33AFT (CPH6303/CPH6403)



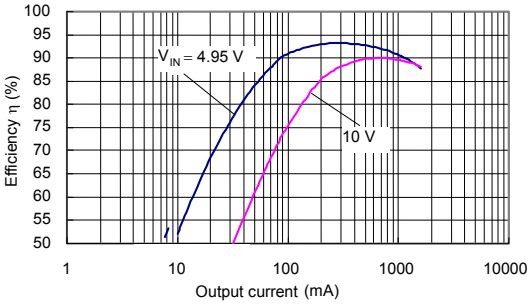
(20) S-8533A33AFT (Si3441DV/Si3442DV)



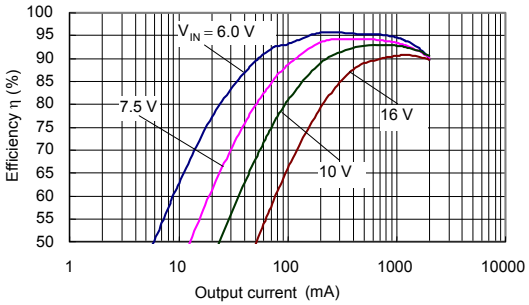
(21) S-8533A33AFT (CPH6302/CPH6402)



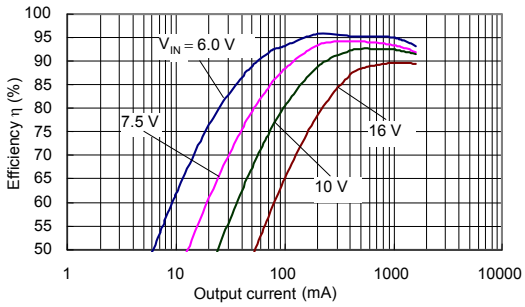
(22) S-8533A33AFT (Si3454DV/Si3455DV)



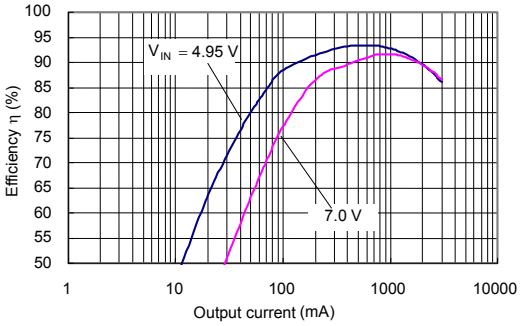
(23) S-8533A50AFT (CPH6302/CPH6402)



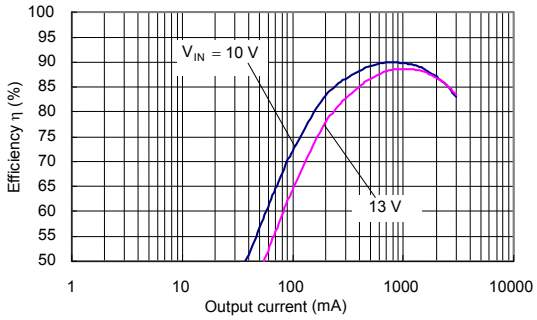
(24) S-8533A50AFT (Si3454DV/Si3455DV)



(25) S-8533A33AFT (CPH6303/CPH6403)



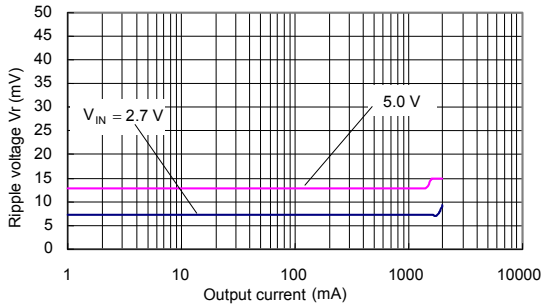
(26) S-8533A33AFT (CPH6302/CPH6402)



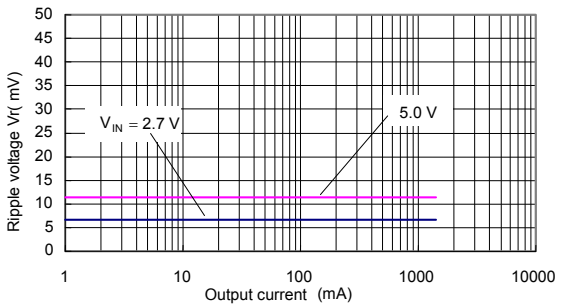
3. Output Current (I_{OUT}) vs. Ripple Voltage (V_r) Characteristics

The following shows the actual output current (I_{OUT}) vs. ripple voltage (V_r) characteristics when the S-8533 Series is used under conditions (27) to (34) in **Table 5**.

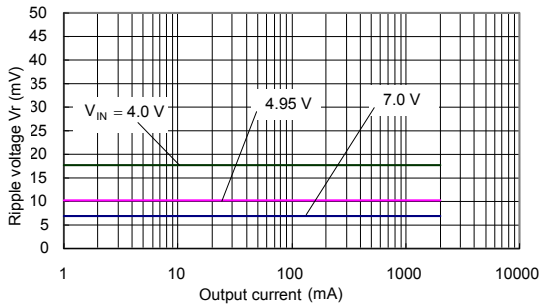
(27) S-8533A15AFT (CPH6303/CPH6403)



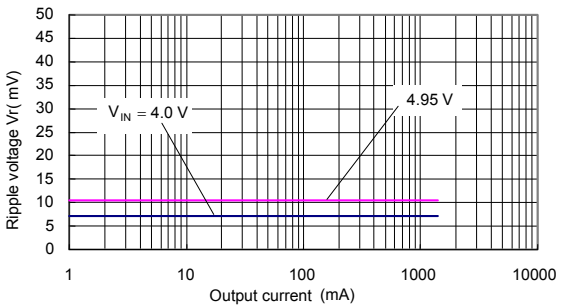
(28) S-8533A15AFT (Si3441DV/Si3442DV)



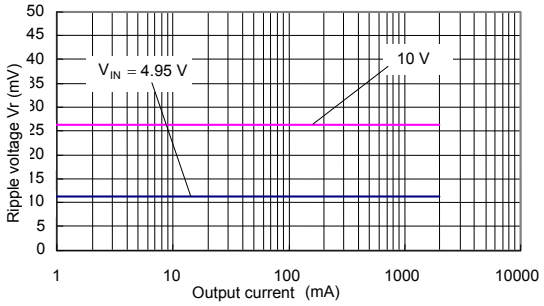
(29) S-8533A33AFT (CPH6303/CPH6403)



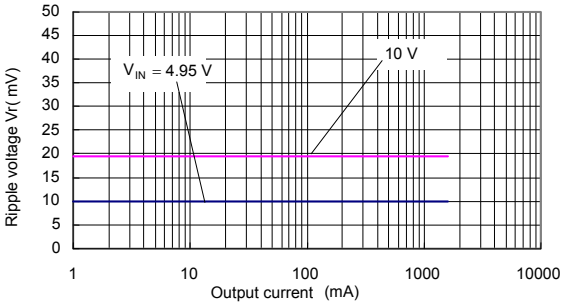
(30) S-8533A33AFT (Si3441DV/Si3442DV)



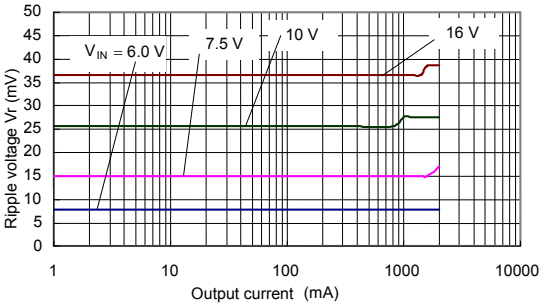
(31) S-8533A33AFT (CPH6302/CPH6402)



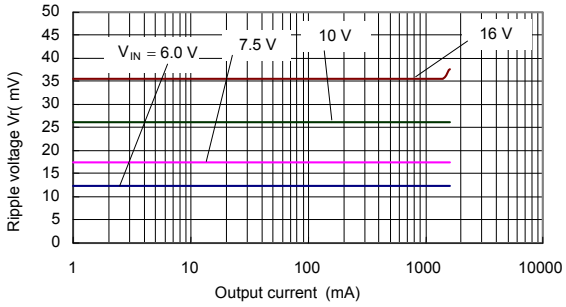
(32) S-8533A33AFT (Si3454DV/Si3455DV)

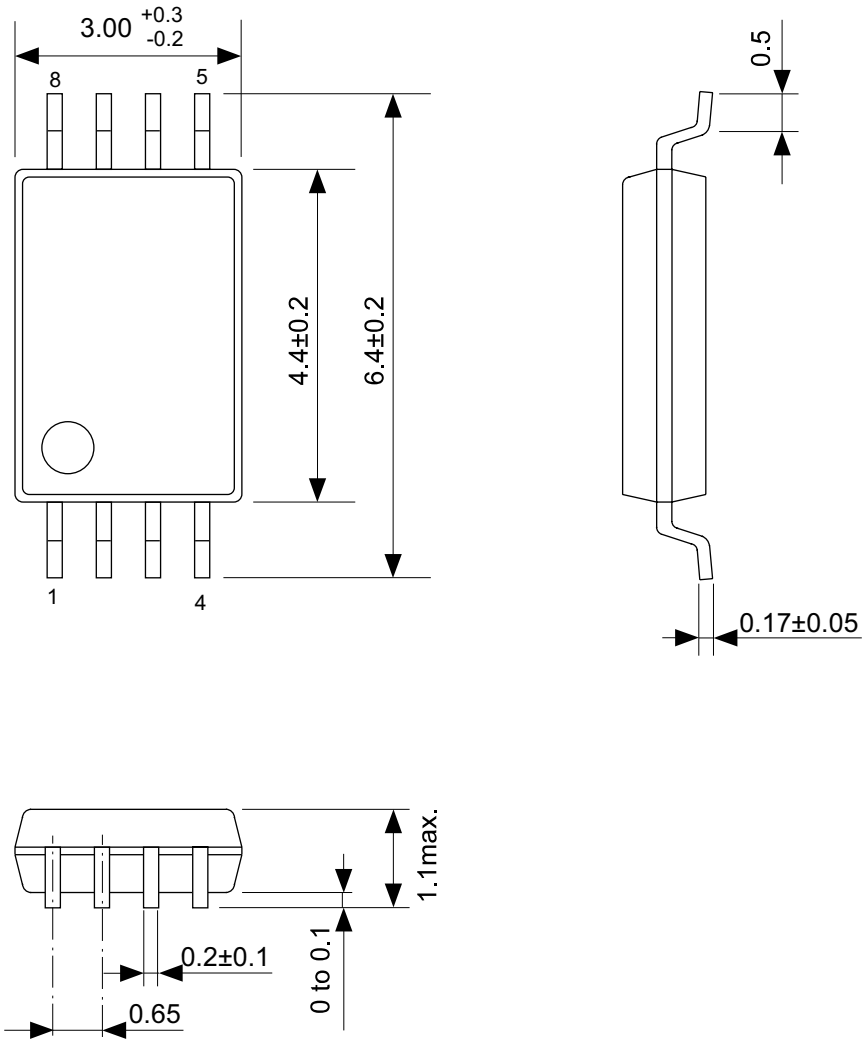


(33) S-8533A50AFT (CPH6302/CPH6402)



(34) S-8533A50AFT (Si3454DV/Si3455DV)

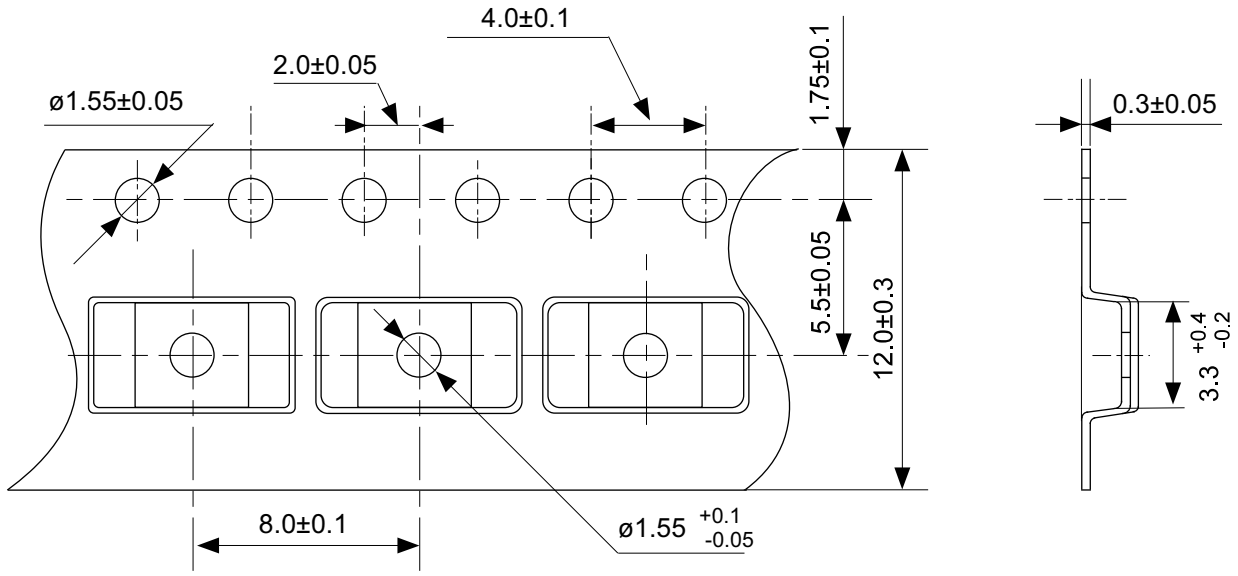


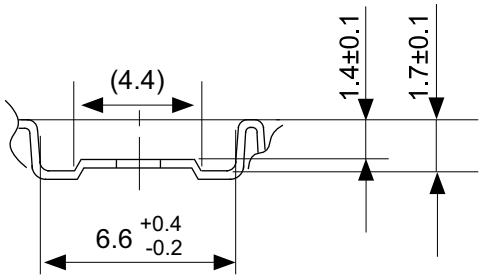


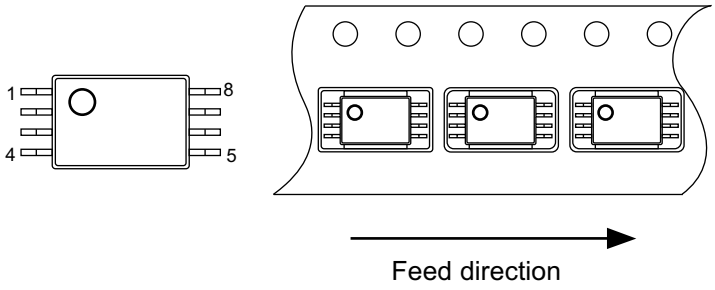
No. FT008-A-P-SD-1.2

TITLE	TSSOP8-E-PKG Dimensions
No.	FT008-A-P-SD-1.2
ANGLE	
UNIT	mm

ABLIC Inc.

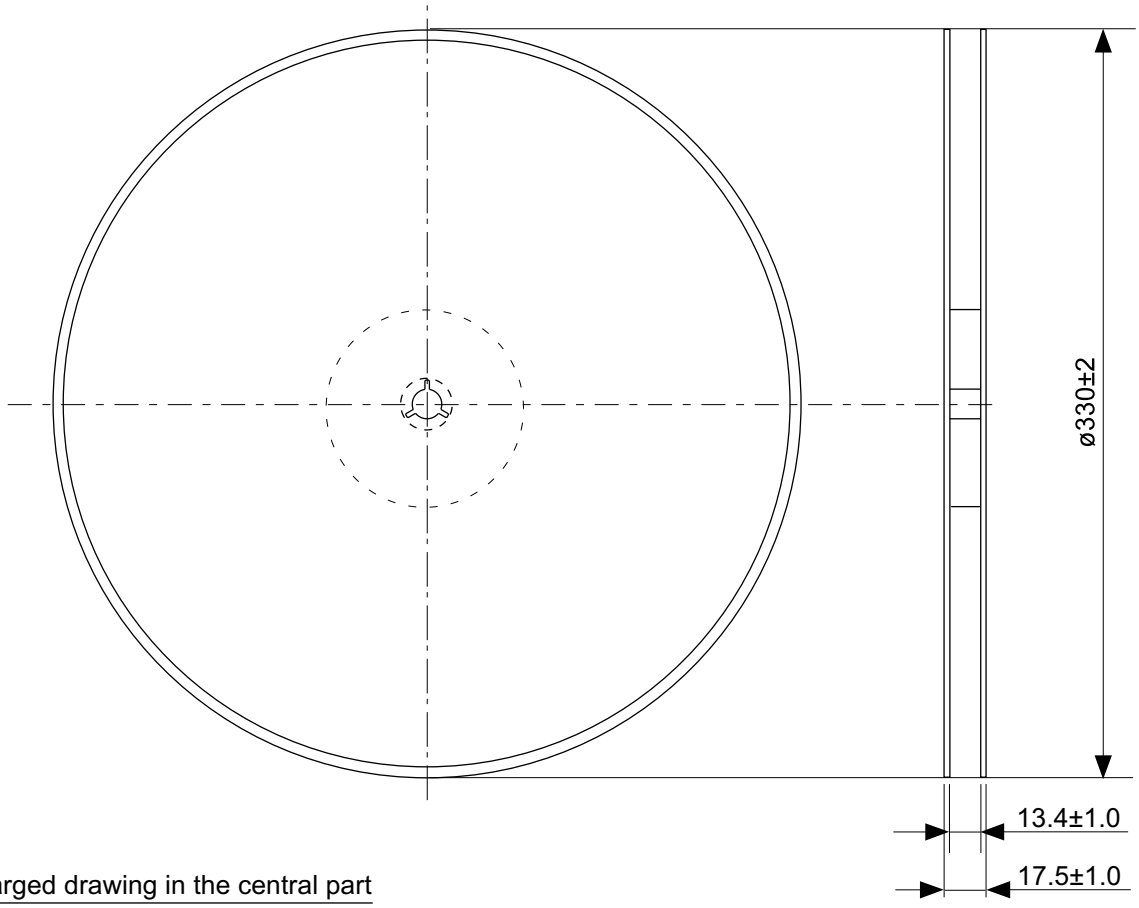




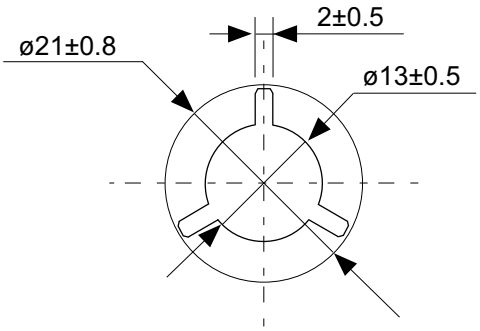


No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

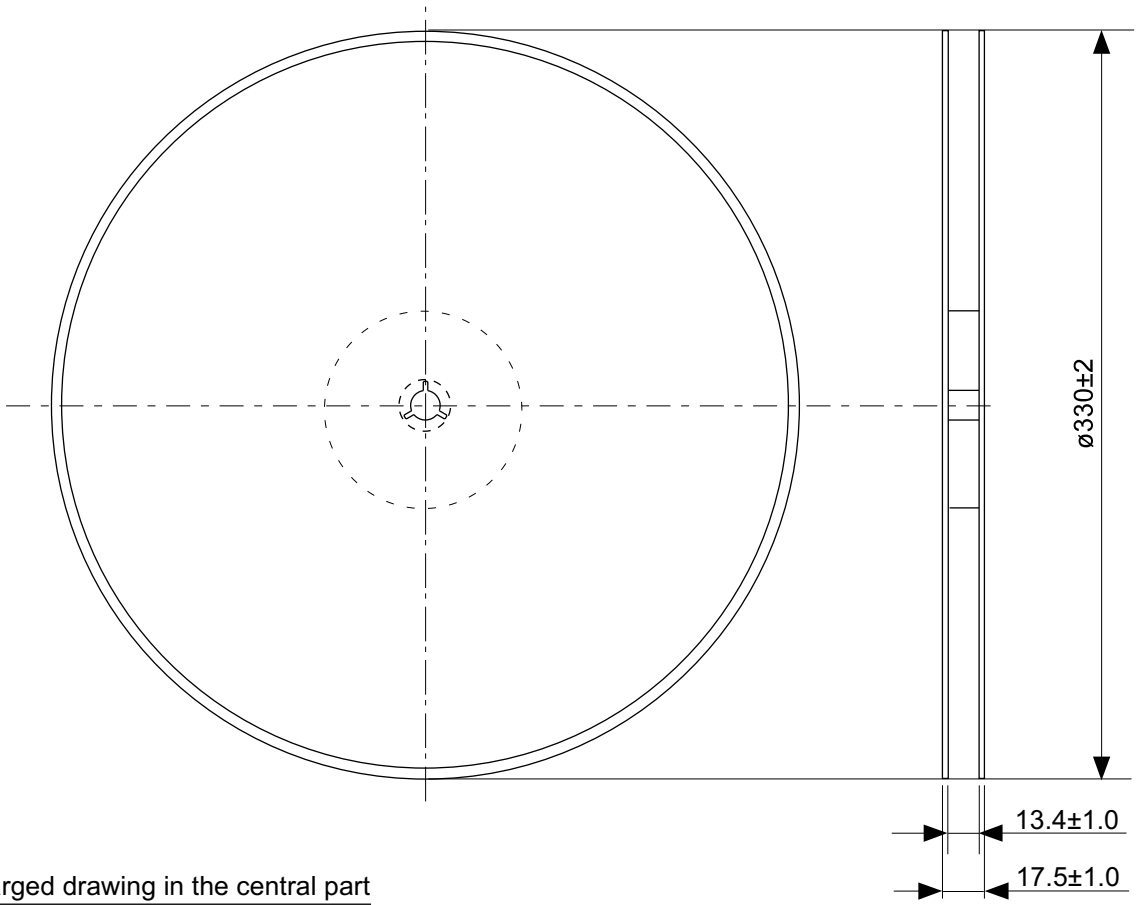


Enlarged drawing in the central part

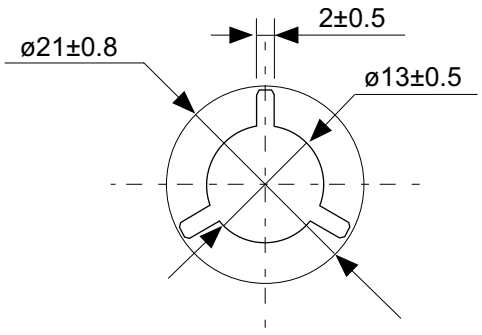


No. FT008-E-R-SD-1.0

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-SD-1.0		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			



Enlarged drawing in the central part



No. FT008-E-R-S1-1.0

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-S1-1.0		
ANGLE		QTY.	4,000
UNIT	mm		
ABLIC Inc.			

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1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
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   Prior consultation with our sales office is required when considering the above uses.
   ABLIC Inc. is not responsible for damages caused by unauthorized or unspecified use of our products.
9. Semiconductor products may fail or malfunction with some probability.
   The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system must be sufficiently evaluated and applied on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc.
    The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party without the express permission of ABLIC Inc. is strictly prohibited.
14. For more details on the information described herein, contact our sales office.

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