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BATTERY BACKUP IC FOR 1-CHIP CPU

S-8420 Series

The S-8420 Series is a CMOS IC designed for use in the switching circuits of main and backup power supplies. It consists of a voltage regulator, three voltage detectors, a power alteration switch, and a control circuit.

In addition to being able to switch from main to backup power supplies, the S-8420 Series has three types of voltage detection output signal corresponding to the power supply voltage. The special sequence for switch control prevents unnecessary exhaustion of the backup power supply; this feature is suitable for structuring backup systems.

■ Features

- Low power consumption
  Normal operation: 32 μA max. (V_{IN} = 6 V)
  Backup: 3.6 μA max.
- Low input/output voltage differences
  Voltage regulator: 0.35 V max. (I_{RO} = 50 mA)
  Switch: 0.3 V max. (I_{OUT} = 50 mA)
- Output voltage accuracy: ±3%
- Three built-in voltage detectors (CS, $\overline{\text{PREEND}}$, $\overline{\text{RESET}}$)
  Detection voltage accuracy: ±3%
- Special sequence
  Backup voltage is not output, if the main power supply voltage does not reach the initial threshold voltage that activates the switch.

■ Applications

- Video camera recorder
- Still video camera
- Memory card
- SRAM Backup equipment

■ Selection Guide

Table 1

Ta = 25°C

Item / Product	Output voltage*			CS detection voltage			CS release voltage			$\overline{\text{RESET}}$ detection voltage		
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.
S-8420AF	4.86	5.0	5.14	4.36	4.49	4.62	4.44	4.59	4.74	2.42	2.5	2.58
S-8420BF	4.85	5.0	5.15	4.07	4.2	4.33	—	—	4.67	2.42	2.5	2.58
S-8420CF	5.06	5.25	5.44	4.07	4.2	4.33	—	—	4.67	2.23	2.3	2.37
S-8420DF	4.85	5.0	5.15	4.07	4.2	4.33	—	—	4.67	2.23	2.3	2.37

[Unit : V]

* S-8420AF/BF/DF : Regulated at the V_{RO} pin (output pin of the voltage regulator)
S-8420CF: Regulated at the V_{OUT} pin (output pin of the switch)

■ Block Diagram

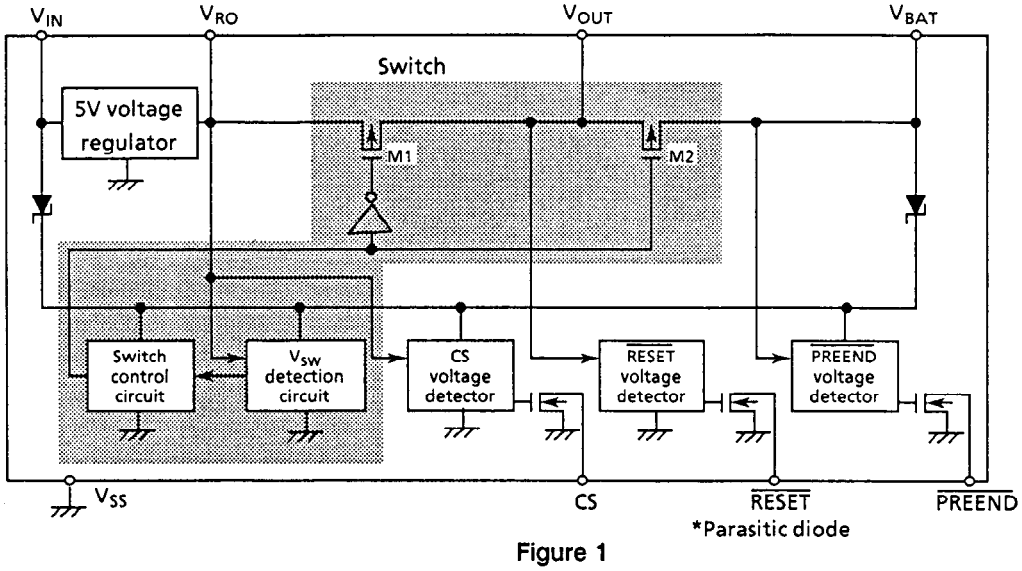
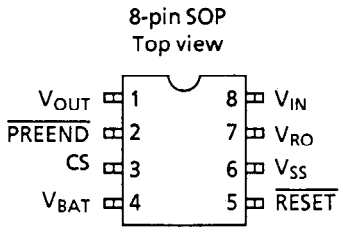


Figure 1

■ Pin Assignment



Pin name	Description
CS	Output pin of CS voltage detector
$\overline{\text{RESET}}$	Output pin of $\overline{\text{RESET}}$ voltage detector
$\overline{\text{PREEND}}$	Output pin of $\overline{\text{PREEND}}$ voltage detector
V_{IN}*	Main power supply input pin
V_{BAT}*	Backup power supply input pin
V_{OUT}*	Output pin of switch
V_{RO}*	Output pin of voltage regulator
V_{SS}	Ground

* Mount capacitors between V_{SS} (GND) and the V_{IN}, V_{BAT}, V_{OUT}, and V_{RO} pins. In particular, mount a capacitor to the V_{RO} pin even when it is not used. (See "■ Standard Circuit")

Figure 2

■ Absolute Maximum Ratings

Table 2

(Unless otherwise specified : Ta = 25°C)

Parameter	Symbol	Ratings	Unit
Main power supply input voltage	V_{IN}	18	V
Backup power supply input voltage	V_{BAT}	18	V
Output voltage of voltage regulator	V_{RO}	V_{SS}-0.3 to V_{IN} + 0.3	V
Output voltage of switch	V_{OUT}	V_{SS}-0.3 to 18	V
Output voltage of CS / $\overline{\text{RESET}}$ / $\overline{\text{PREEND}}$	V_{CS} / V_{RESET} / V_{PRE}	V_{SS}-0.3 to 18	V
Power dissipation	P_D	300	mW
Operating temperature	T_{opr}	-30 to + 80	°C
Storage temperature	T_{stg}	-40 to + 125	°C

■ Electrical Characteristics

1. S-8420AF / BF / DF

Table 3

(Unless otherwise specified : Ta = 25°C)

	Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test cir.
Voltage regulator	Output voltage	V_{RO}	V_{IN} = 6 V, I_{RO} = 50 mA	S-8420AF	4.86	5.00	5.14	V	1
				S-8420BF	4.85	5.00	5.15	V	
				S-8420DF	4.85	5.00	5.15	V	
	I/O voltage difference	V_{dif1}	I_{RO} = 50 mA		—	0.2	0.35	V	
	Load regulation	$\triangle V_{RO}$	V_{IN} = 6 V, I_{RO} = 100 μA to 60 mA		—	50	110	mV	
	Line regulation	$\frac{\triangle V_{RO}}{\triangle V_{IN} \cdot V_{RO}}$	V_{IN} = 6 to 15 V, I_{RO} = 50 mA		—	0.1	0.3	%/V	
	Input voltage of main power supply	V_{IN}			—	—	15	V	
	Temperature coefficient of V_{RO}	$\frac{\triangle V_{RO}}{\triangle Ta}$	V_{IN} = 6 V, I_{RO} = 50 mA, Ta = -30°C to 80°C		—	± 0.71	—	mV/°C	
Switch	Switch voltage	$-V_{SW}$	V_{BAT} = 3 V		3.20	3.30	3.40	V	3
	Hysteresis width 1	V_{HYSSW}	V_{BAT} = 3 V		0.12	0.16	0.20	V	
	I/O voltage difference	V_{dif2}	V_{IN} = 6 V, I_{OUT} = 50 mA, V_{BAT} = 3 V		—	—	0.3	V	2
		V_{dif3}	V_{IN} = open, I_{OUT} = 200 μA, V_{BAT} = 3 V		—	—	0.1	V	
	Leakage current	I_{LEK}	V_{IN} = 6 V, I_{OUT} = 50 mA, V_{BAT} = 0 V		—	—	100	nA	
Voltage detector	CS detection voltage	$-V_{DET1}$	V_{BAT} = open	S-8420AF	4.36	4.49	4.62	V	4
				S-8420BF	4.07	4.20	4.33	V	
				S-8420DF	4.07	4.20	4.33	V	
	CS release voltage	$+V_{DET1}$	V_{BAT} = open	S-8420AF	4.44	4.59	4.74	V	
				S-8420BF	—	—	4.67	V	
				S-8420DF	—	—	4.67	V	
	$\overline{RESET}$ detection voltage	$-V_{DET2}$	V_{IN} = open	S-8420AF	2.42	2.50	2.58	V	8
				S-8420BF	2.42	2.50	2.58	V	
				S-8420DF	2.23	2.30	2.37	V	
	Hysteresis width 2	V_{HYS2}	V_{IN} = open	S-8420AF	0.09	0.12	0.16	V	4
				S-8420BF	0.09	0.12	0.16	V	
				S-8420DF	0.08	0.11	0.15	V	
	$\overline{PREEND}$ detection voltage	$-V_{DET3}$	V_{IN} = open		$-V_{DET2}$ + 0.15	$-V_{DET2}$ + 0.20	$-V_{DET2}$ + 0.25	V	8
	Hysteresis width 3	V_{HYS3}	V_{IN} = open	S-8420AF	0.10	0.14	0.18	V	4
				S-8420BF	0.10	0.14	0.18	V	
				S-8420DF	0.09	0.13	0.17	V	
	Operating voltage	V_{opr}	V_{IN}		1.5	—	15	V	4, 8
	Temperature coefficient of detection voltage	$\frac{\triangle -V_{DET1}}{\triangle Ta}$	Ta = -30°C to 80°C		—	± 0.5	—	mV/°C	4
		$\frac{\triangle -V_{DET2,3}}{\triangle Ta}$	Ta = -30°C to 80°C		—	± 0.34	—	mV/°C	8
		$\frac{\triangle -V_{SW}}{\triangle Ta}$	Ta = -30°C to 80°C		—	± 0.39	—	mV/°C	3
	Output current	I_{SINK}	V_{DS} = 0.5 V	$\overline{RESET}$: V_{IN} or V_{BAT} = 2.0 V	2.50	4.00	—	mA	5
				$\overline{PREEND}$: V_{IN} or V_{BAT} = 2.0 V	2.00	2.80	—	mA	
				CS : V_{IN} or V_{BAT} = 2.0 V	2.00	2.80	—	mA	
				CS : V_{IN} or V_{BAT} = 3.6 V	4.10	6.50	—	mA	

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit	Test cir.
Current consumption	I_{SS1}	V_{IN} = 6 V, Unloaded V_{BAT} = 3 V		—	12	32	μA	6
	I_{BAT1}*			—	0.27	0.52	μA	
	I_{SS2}	V_{IN} = 15 V, Unloaded V_{BAT} = 3 V		—	14	35	μA	
	I_{BAT2}*			—	0.27	0.52	μA	
	I_{BAT3}*	V_{IN} = open V_{BAT} = 3 V, Unloaded	Ta = 25°C	—	1.6	3.6	μA	
			Ta = 80°C	—	—	5.0	μA	
Initial threshold V_{IN} voltage to start switch operation	V_{INI}	V_{BAT} = 3 V		4.45	4.70	4.95	V	7
Temperature coefficient of V_{INI}	$\frac{\triangle V_{INI}}{\triangle Ta}$	Ta = -30°C to 80°C		—	-2.4	—	mV/°C	
Input voltage of backup power supply**	V_{BAT}			1.5	—	4.0	V	8

* I_{BAT1}, I_{BAT2}, and I_{BAT3} show the currents consumed by the backup power supply.

** Applying over 4.0 V to the V_{BAT} pin does not destroy the IC. However, to ensure normal operation, keep the V_{BAT} voltage below 4.0 V.

2. S-8420CF

Table 4

(Unless otherwise specified : Ta = 25°C)

	Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test cir.
	Output voltage*	V_{OUT}	V_{IN} = 8.5 V I_{OUT} = 20 mA	5.06	5.25	5.44	V	1
V regulator	I/O voltage difference	V_{dif1}	I_{RO} = 50 mA	—	0.2	0.35	V	
	Load regulation	$\triangle V_{RO}$	V_{IN} = 8.5 V I_{RO} = 100 μA to 60 mA	—	50	110	mV	
	Line regulation	$\frac{\triangle V_{RO}}{\triangle V_{IN} \cdot V_{RO}}$	V_{IN} = 6 to 15 V I_{RO} = 20 mA	—	0.1	0.3	%/V	
	Input voltage of main power supply	V_{IN}		—	—	15	V	
	Temperature coefficient of V_{OUT}	$\frac{\triangle V_{RO}}{\triangle Ta}$	V_{IN} = 8.5 V, I_{RO} = 20 mA Ta = -30°C to 80°C	—	± 0.71	—	mV/°C	
Switch	Switch voltage	$-V_{SW}$	V_{BAT} = 3 V	3.20	3.30	3.40	V	3
	Hysteresis width 1	V_{HYSSW}	V_{BAT} = 3 V	0.12	0.16	0.20	V	
	I/O voltage difference	V_{dif2}	V_{IN} = 8.5 V, I_{OUT} = 20 mA V_{BAT} = 3 V	—	0.12	0.15	V	2
		V_{dif3}	V_{IN} = open, I_{OUT} = 200 μA, V_{BAT} = 3 V	—	—	0.1	V	
	Leakage current	I_{LEK}	V_{IN} = 8.5 V, I_{OUT} = 20 mA V_{BAT} = 0 V	—	—	100	nA	
Voltage detector	CS detection voltage	$-V_{DET1}$	V_{BAT} = open	4.07	4.20	4.33	V	4
	CS release voltage	$+V_{DET1}$	V_{BAT} = open	—	—	4.67	V	
	$\overline{\text{RESET}}$ detection voltage	$-V_{DET2}$	V_{IN} = open	2.23	2.30	2.37	V	8
	Hysteresis width 2	V_{HYS2}	V_{IN} = open	0.08	0.11	0.15	V	
	$\overline{\text{PREEND}}$ detection voltage	$-V_{DET3}$	V_{IN} = open	$-V_{DET2}$ + 0.15	$-V_{DET2}$ + 0.20	$-V_{DET2}$ + 0.25	V	
	Hysteresis width 3	V_{HYS3}	V_{IN} = open	0.09	0.13	0.17	V	
	Operating voltage	V_{opr}	V_{IN}	1.5	—	15	V	4, 8
	Temperature coefficient of detection voltage	$\frac{\triangle -V_{DET1}}{\triangle Ta}$	Ta = -30°C to 80°C	—	± 0.5	—	mV/°C	4
		$\frac{\triangle -V_{DET2,3}}{\triangle Ta}$	Ta = -30°C to 80°C	—	± 0.34	—	mV/°C	8
		$\frac{\triangle -V_{SW}}{\triangle Ta}$	Ta = -30°C to 80°C	—	± 0.39	—	mV/°C	3

* Output voltage is regulated at the V_{OUT} pin.

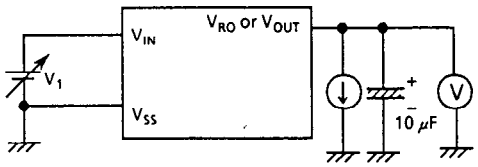
	Parameter	Symbol	Conditions			Min.	Typ.	Max.	Unit	Test cir.
V·detector	Output current	I_{SINK}	V_{DS} = 0.5 V	$\overline{RESET}$	V_{IN} or V_{BAT} = 2.0 V	2.50	4.00	—	mA	5
				$\overline{PREEND}$	V_{IN} or V_{BAT} = 2.0 V	2.00	2.80	—	mA	
				CS	V_{IN} or V_{BAT} = 2.0 V	2.00	2.80	—	mA	
					V_{IN} or V_{BAT} = 3.6 V	4.10	6.50	—	mA	
Current consumption		I_{SS1}	V_{IN} = 8.5 V, Unloaded V_{BAT} = 3 V			—	13	33	μA	6
		I_{BAT1}*				—	0.27	0.52	μA	
		I_{SS2}	V_{IN} = 15 V, Unloaded V_{BAT} = 3 V			—	14	35	μA	
		I_{BAT2}*				—	0.27	0.52	μA	
		I_{BAT3}*	V_{IN} = open V_{BAT} = 3 V Unloaded		Ta = 25°C	—	1.6	3.6	μA	
					Ta = 80°C	—	—	5.0	μA	
Initial threshold V_{IN} voltage to start switch operation		V_{INI}	V_{BAT} = 3 V			4.45	4.70	4.95	V	7
Temperature coefficient of V_{INI}		$\frac{\triangle V_{INI}}{\triangle Ta}$	Ta = -30°C to 80°C			—	-2.4	—	mV/°C	
Input voltage of backup power supply**		V_{BAT}				1.5	—	4.0	V	8

* I_{BAT1}, I_{BAT2}, and I_{BAT3} show the currents consumed by the backup power supply.

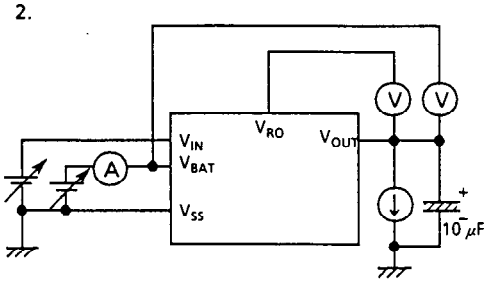
** Applying over 4.0 V to the V_{BAT} pin does not destroy the IC. However, to ensure normal operation, keep the V_{BAT} voltage below 4.0 V.

■ Test Circuit

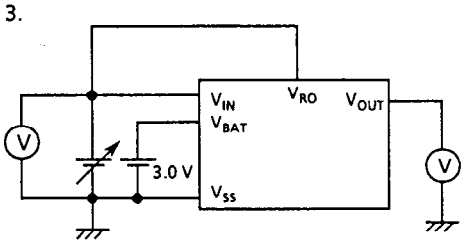
1.



2.

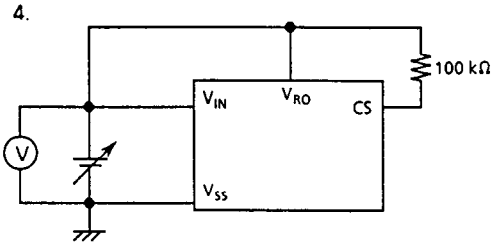


3.

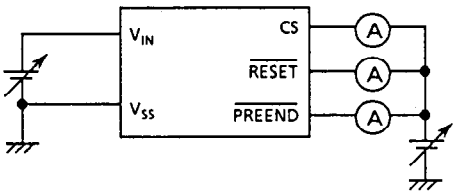


Measure the value after applying 6 V or more to V_{IN}.

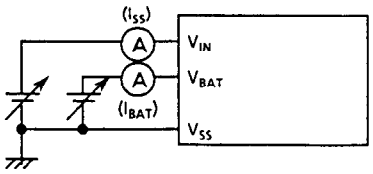
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5.

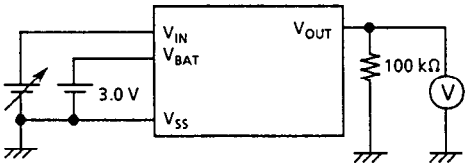


6.



To measure I_{BAT3}, first apply 3 V to V_{BAT} and 6 V or more to V_{IN}. Then open these pins and measure the current when V_{BAT} is 3 V.

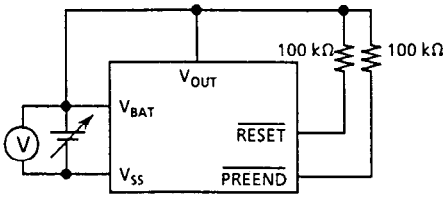
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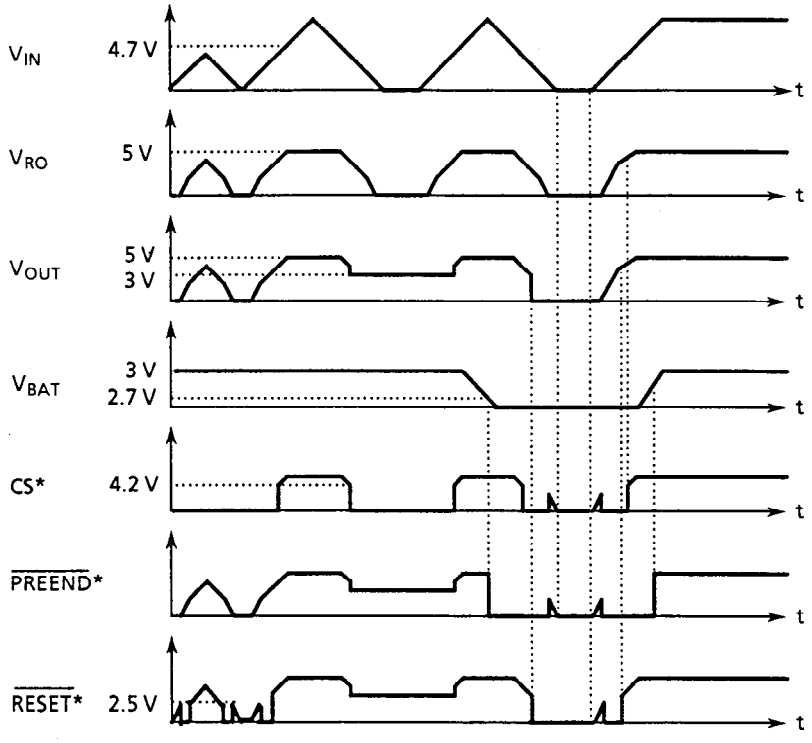
Condition:

After applying 4.44 V to V_{IN} and then setting it to 0 V, V_{OUT} must be equal to or lower than 0.5 V.
After applying 4.96 V to V_{IN} and then setting it to 0 V, V_{OUT} must be equal to or higher than 2.5 V.

8.



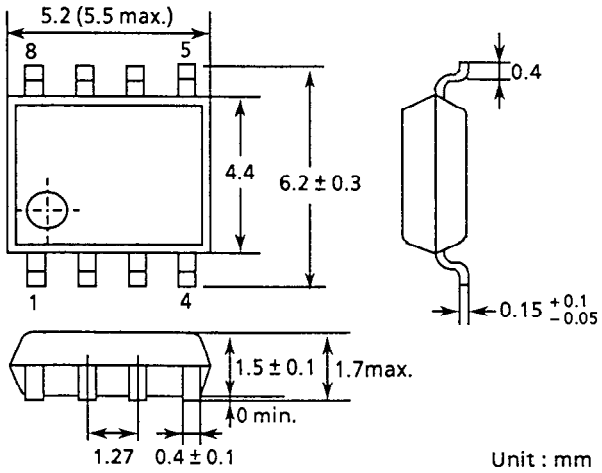
■ Operation Timing Chart



* CS is pulled up to V_{RO}, and $\overline{PREEND}$ and $\overline{RESET}$ are pulled up to V_{OUT}.

Figure 3 In case of the S-8420BF

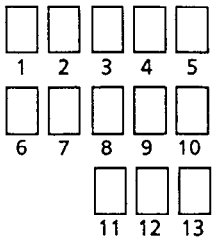
■ Dimensions



Unit : mm

Figure 4

■ Markings



1 to 7 : Product name
8 : Assembly code
9 : Year of assembly (last digit)
10 : Month of assembly; Jan. = 1, Feb. = 2, Mar. = 3, Apr. = 4, May = 5, June = 6, July = 7, Aug. = 8, Sept. = 9, Oct. = X, Nov. = Y, Dec. = Z
11 to 13: Lot No.

Figure 5

■ Taping

1. Tape specifications

T1 and T2 types are available depending upon the direction of ICs on the tape.

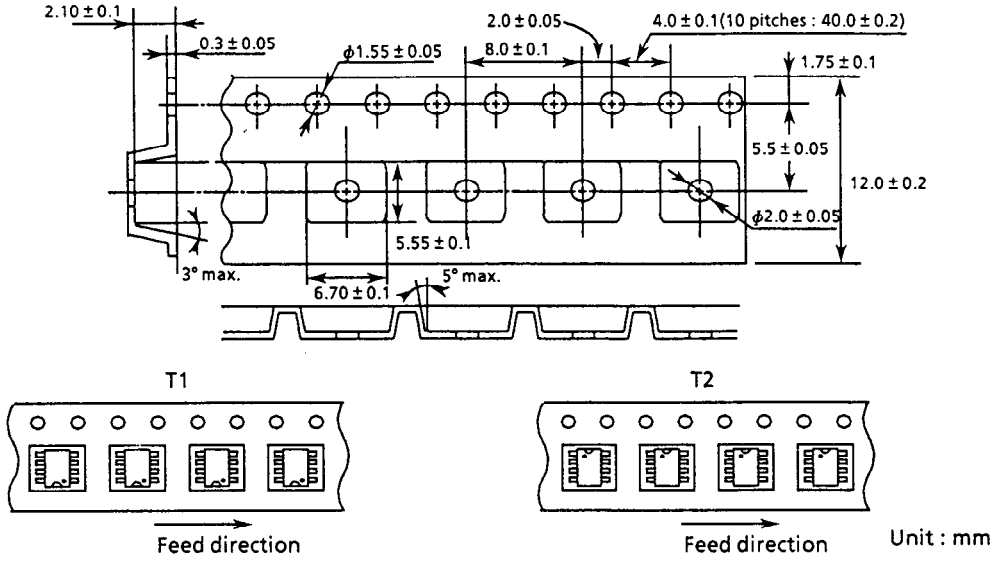


Figure 6

2. Reel specifcations

1 reel holds 2000 products.

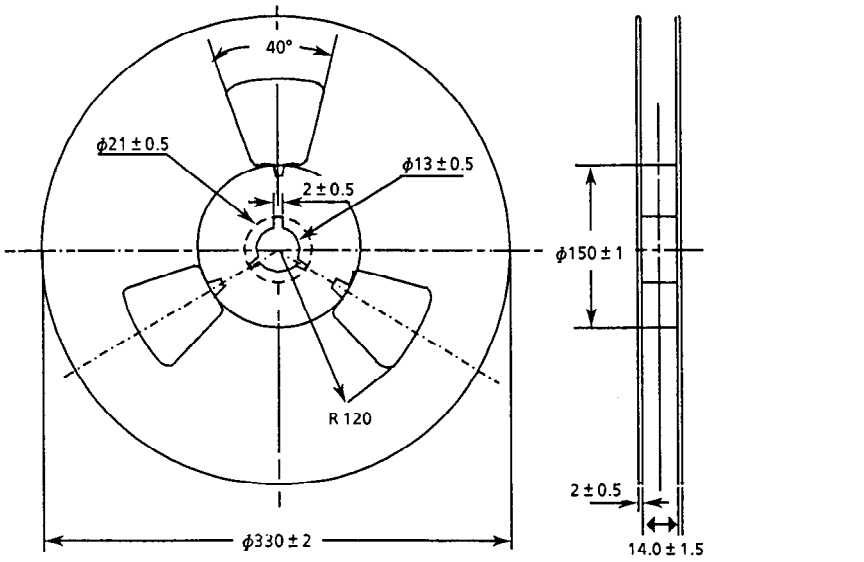


Figure 7

■ Operation

An S-8420 Series IC chip consists of a voltage regulator, a switch, and three voltage detectors. The voltage regulator rectifies input voltage V_{IN} and outputs to V_{RO}. The switch alters the output to V_{OUT} to V_{RO} or V_{BAT}. This section describes the functions and operations of each part.

1. Voltage regulator

The built-in regulator has a very small I/O voltage difference (V_{dif1} = 0.2 V typ. at I_{RO} = 50 mA). When V_{IN} is 6 V and I_{RO} is 50 mA, 5 V ± 3% (in case of the S-8420BF and CF) is output to the V_{RO} pin (output pin of the voltage regulator).

I/O voltage difference V_{dif1}

Assume that the V_{RO} voltage when V_{IN} is 6 V and I_{RO} is 50 mA is Vinitial. When the amount voltage of I/O voltage difference V_{dif1} and Vinitial is applied to the V_{IN} pin, 95% of the Vinitial voltage is output at the V_{RO} pin.

2. Switch

The switch consists of the switch control circuit, V_{SW} detection circuit, and switch transistors M1 and M2.

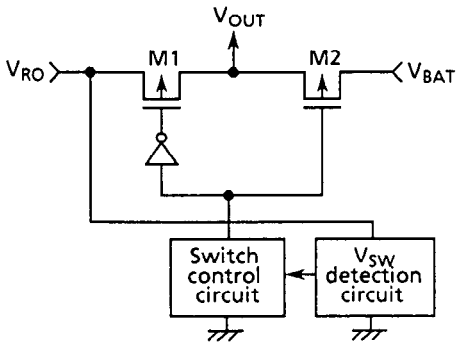


Figure 8 Switch

2.1 V_{SW} detection circuit

The V_{SW} detection circuit monitors the V_{RO} voltage (output of the voltage regulator) and sends the results of detection to the switch control circuit. The detection voltage ($-V_{SW}$) is specified as 3.30 ± 0.1 V and the release voltage ($+V_{SW}$) as 3.46 V typ. Between $-V_{SW}$ and $+V_{SW}$ means hysteresis; during hysteresis, the output is kept in the immediately preceding status.

2.2 Switch control circuit

The switch control circuit receives the signal from the V_{SW} detection circuit and controls M1 and M2. The switch control circuit operates in two statuses: the special and normal sequences. In the special sequence status, the circuit does not receive nor control according to the V_{IN} (or V_{BAT}) voltage sequence. In the normal sequence status, the circuit receives and controls within the range of the operating voltages. Initially, the circuit is kept in the special sequence status. When V_{IN} exceeds V_{INI} (initializing voltage: 4.7 ± 0.25 V) even once, the circuit enters the normal sequence status.

(1) Special sequence status

When the V_{IN} (or V_{BAT}) voltage rises from under 0.5 V, the switch control circuit is kept in the special sequence status until V_{IN} reaches V_{INI}.

At that time, the switch control circuit turns M1 on and turns M2 off regardless of the status of the V_{SW} detection circuit. Therefore, the voltage output at V_{OUT} is V_{RO} minus voltage reduction due to M1.

(2) Normal sequence status

When V_{IN} voltage exceeds V_{INI} (V_{BAT} is 4.0 V or less and does not exceed V_{INI}), the switch control circuit enters the normal sequence. The normal sequence is valid while V_{IN} or V_{BAT} is at the minimum operating voltage (1.5 V) or higher.

Once the circuit enters the normal sequence, it turns M1 and M2 on and off according to the V_{RO} voltage as shown in Table 5.

To return the circuit to the special sequence status, lower the V_{IN} or V_{BAT} to below 0.5 V.

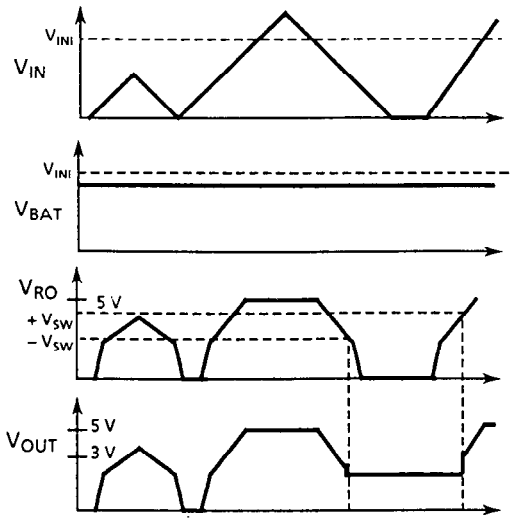


Figure 9

Table 5

V_{RO} voltage	M1	M2	V_{OUT}
$V_{RO} \geqq +V_{SW}$	ON	OFF	$V_{RO}-V_{dif2}$
$V_{RO} \leqq -V_{SW}$	OFF	ON	$V_{BAT}-V_{dif3}$

2.3 Switch transistors M1 and M2

M1 and M2 are turned on and off by the switch control circuit as described in Table 5.

The ON resistance of M1 is 6 Ω or less and has characteristics equivalent to a Shottky diode. Therefore, if M1 is turned on to connect V_{OUT} to V_{RO}, the maximum voltage drop V_{dif2} due to M1 is $6 \times I_{OUT}$ (output current). The minimum output at the V_{OUT} pin is V_{RO} -V_{dif2} (max.).

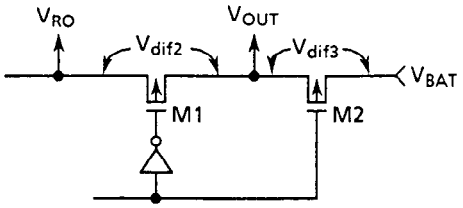


Figure 10 Definitions of V_{dif2} and V_{dif3}

The ON resistance of M2 is 500 Ω or less. Therefore, when M2 is turned on to connect V_{OUT} to V_{BAT}, the maximum voltage drop V_{dif3} due to M2 is 500 × I_{OUT} (output current). The minimum output at the V_{OUT} pin is V_{BAT}-V_{dif3} (max.).

When M1 is on and M2 is off, the leakage current of M2 is kept below 100 nA (V_{IN} = 6 V, I_{OUT} = 50 mA, Ta = 25°C) with the V_{BAT} pin connected to the ground (V_{SS}).

3. Voltage detector

The S-8420 Series has three voltage detectors featuring high precision and low power consumption with hysteresis characteristics. The CS and $\overline{\text{PREEND}}$ detectors receive power from the V_{IN} and V_{BAT} pins. Therefore, the output is stable as long as the main or backup power supplies are within the operating voltage range (1.5 to 15 V). All outputs are Nch open-drains.

(1) CS voltage detector

CS monitors V_{RO} (output of voltage regulator). The detection voltage is about 4 V, but varies with the model (see Table 1). The result of detection is output at the CS pin: "L" for lower voltages than the detection level and "H" for higher voltages than the release level.

(2) $\overline{\text{PREEND}}$ voltage detector

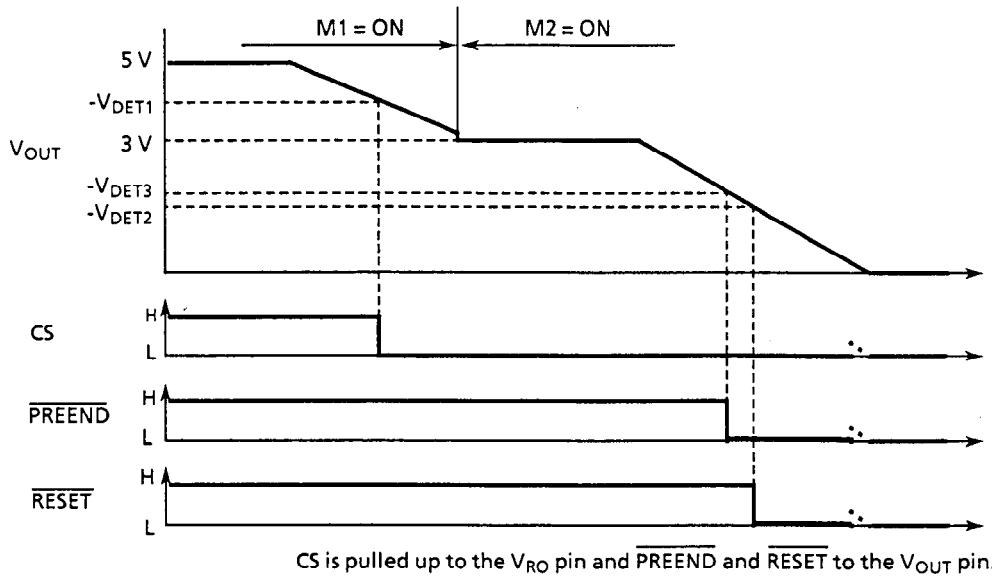
$\overline{\text{PREEND}}$ monitors the V_{BAT} pin. The detection voltage is 0.2 V higher typically than $\overline{\text{RESET}}$, indicating that the backup power supply is running out. The result of detection is output at the $\overline{\text{PREEND}}$ pin: "L" for lower voltages than the detection level and "H" for higher voltages than the release level.

(3) $\overline{\text{RESET}}$ voltage detector

$\overline{\text{RESET}}$ monitors the V_{OUT} pin. The detection voltage is 2.3 V or 2.5 V, but varies with the model (see Table 1). The result of detection is output at the $\overline{\text{RESET}}$ pin: "L" for lower voltages than the detection level and "H" for higher voltages than the release level.

NOTE $\overline{\text{PREEND}}$ and $\overline{\text{RESET}}$ are detected at different pins. In practice, current is taken from the V_{BAT} side, so consider the I/O voltage difference (V_{dif3}) of M2 when M2 is turned on.

Figure 11 shows the detecting positions of each voltage detector.



CS is pulled up to the V_{RO} pin and $\overline{PREEND}$ and $\overline{RESET}$ to the V_{OUT} pin.

Figure 11 Detection potentials of voltage detectors

■ Transient Response

1. Line transient response against input voltage fluctuation

Input voltage fluctuation differs with the types of the signal applied: type Ⅰ (square wave between 6.0 V and 10 V) and type Ⅱ (square wave from 0 V to 10 V) (see Figure 12). This section describes the ringing waveforms and parameter dependency of each type. For reference, Figure 13 describes the measuring circuit.

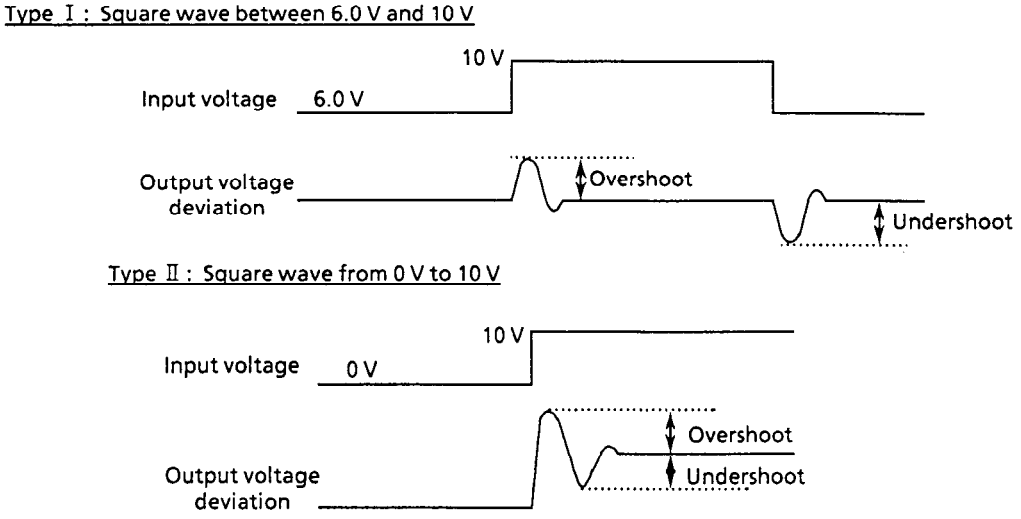


Figure 12

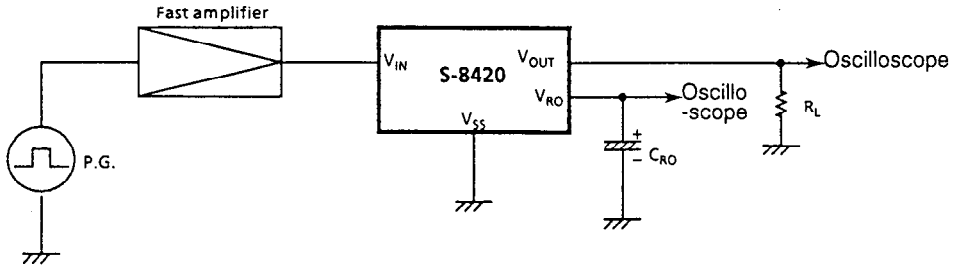
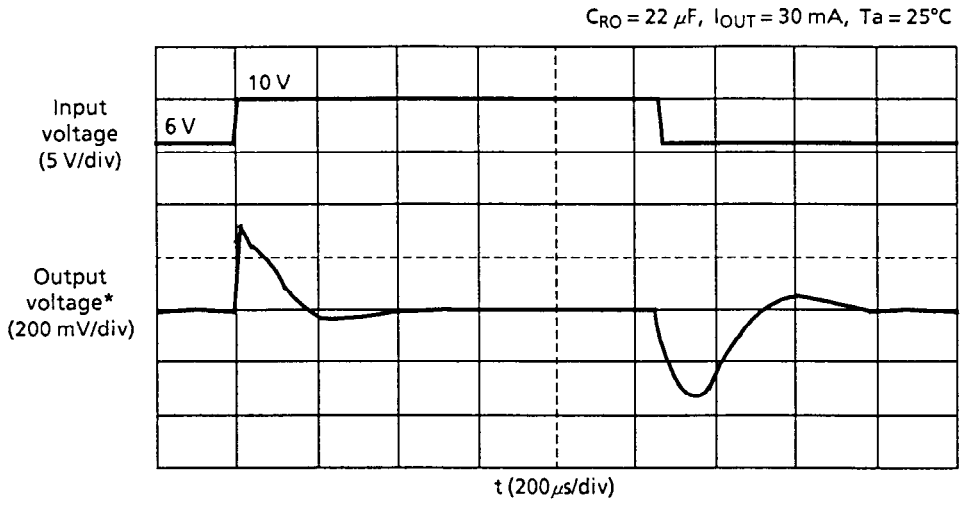


Figure 13 Measuring circuit

Type I



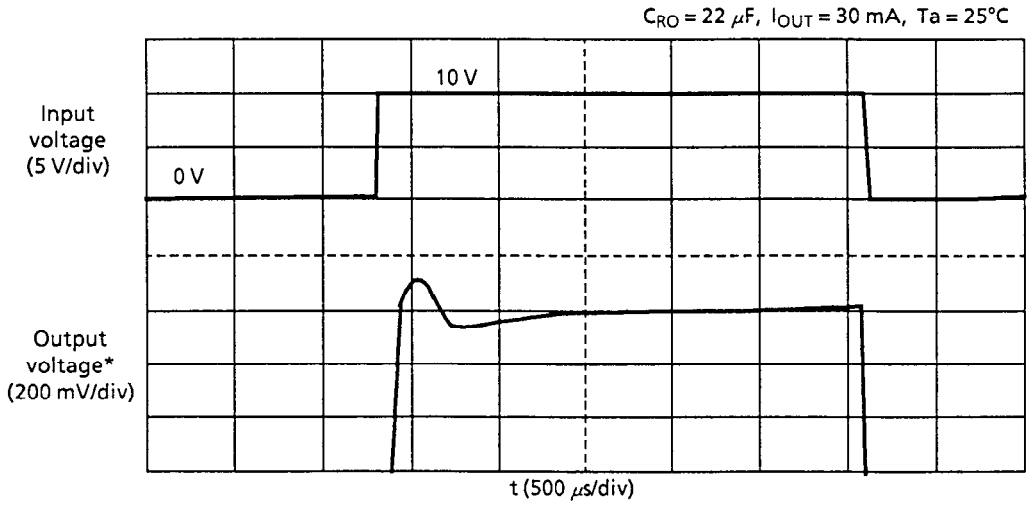
* The output waveforms at V_{RO} and V_{OUT} pins are almost the same.

Figure 14 Type I ringing waveform

Table 6 Type I parameter dependency

Parameter		Conditions	Method to decrease overshoot	Method to decrease undershoot
Output current	I_{OUT}	5 to 50 mA	Decrease	Decrease
Load capacitance	C_{RO}	5 to 47 μF	Increase	Increase
Input fluctuation	$\triangle V_{IN}$	1 to 4 V	Decrease	Decrease
Temperature	Ta	-30°C to + 80°C	High temperature	High temperature

Type II



* The output waveforms at V_{RO} and V_{OUT} pins are almost the same.

Figure 15 Type II ringing waveform

Table 7 Type II parameter dependency

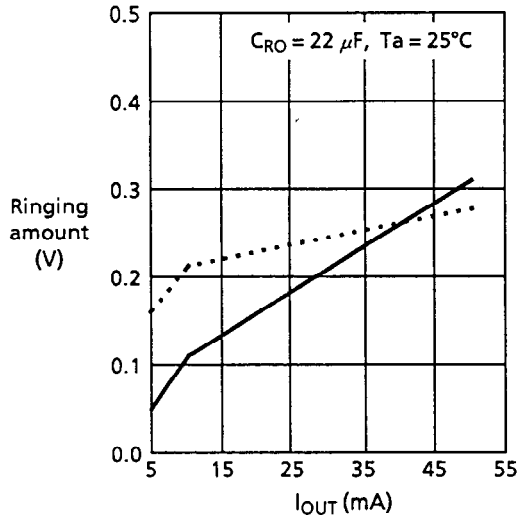
Parameter		Conditions	Method to decrease overshoot	Method to decrease undershoot
Output current	I_{OUT}	5 to 50 mA	Increase	Increase
Load capacitance	C_{RO}	5 to 47 μF	Decrease	Decrease
Temperature	Ta	-30°C to + 80°C	Low temperature	Low temperature

For reference, the following pages describe the results of measuring the ringing amounts at the V_{OUT} and V_{RO} pins using the output current (I_{OUT}), load capacitance (C_{RO}), input fluctuation width ($\triangle V_{IN}$), and temperature as parameters.

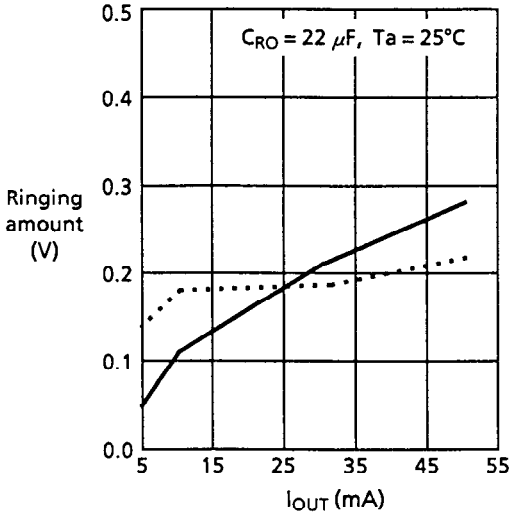
Reference data: Type I

1. I_{OUT} dependency

1.1 V_{OUT} pin

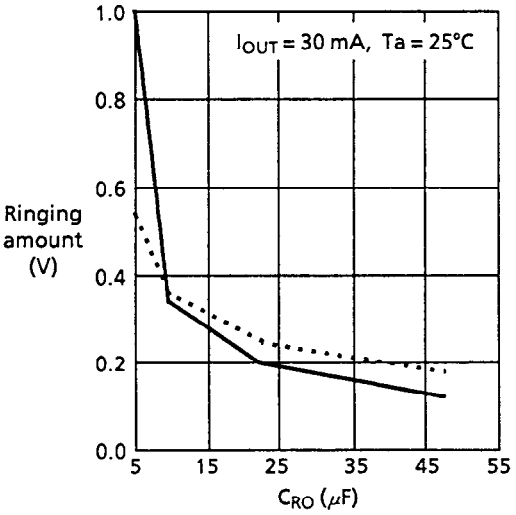


1.2 V_{RO} pin

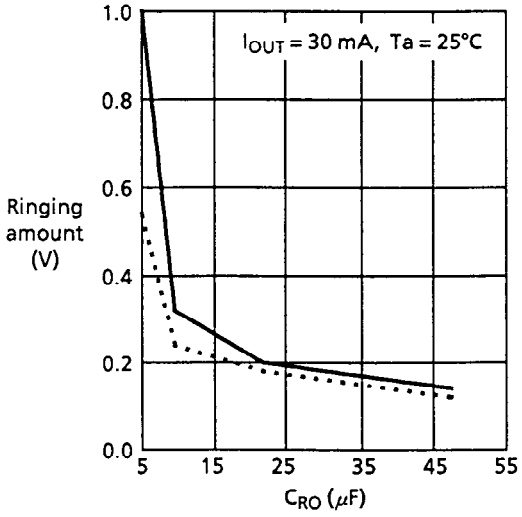


2. C_{RO} dependency

2.1 V_{OUT} pin



2.2 V_{RO} pin

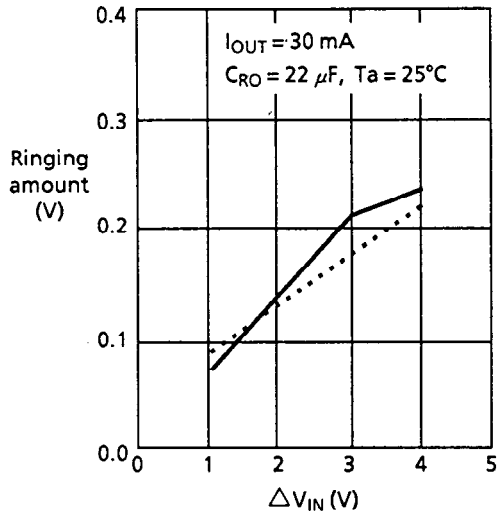


——— Undershoot
· · · · · Overshoot

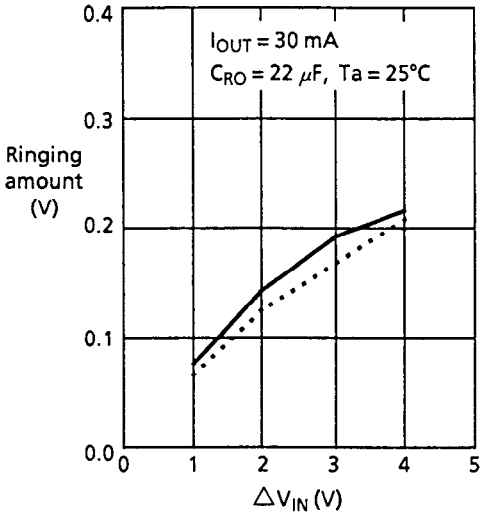
3. $\triangle V_{IN}$ dependency

$\triangle V_{IN}$ shows the difference between the low voltage fixed to 6 V and the high voltage. For example, $\triangle V_{IN} = 2$ V means the difference between 6 V and 8 V.

3.1 V_{OUT} pin

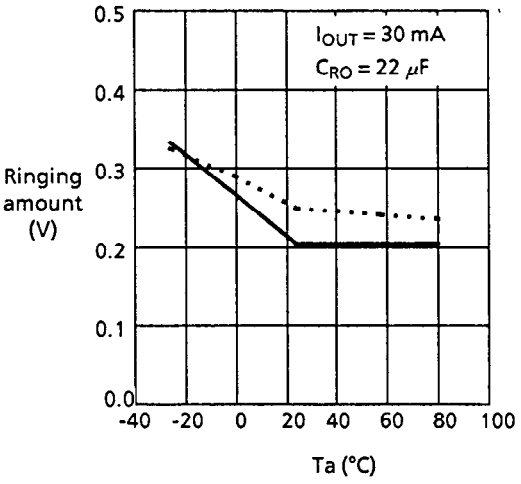


3.2 V_{RO} pin

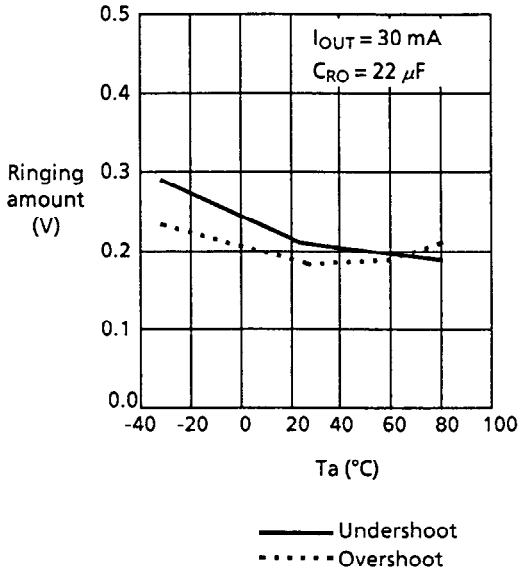


4. Temperature dependency

4.1 V_{OUT} pin



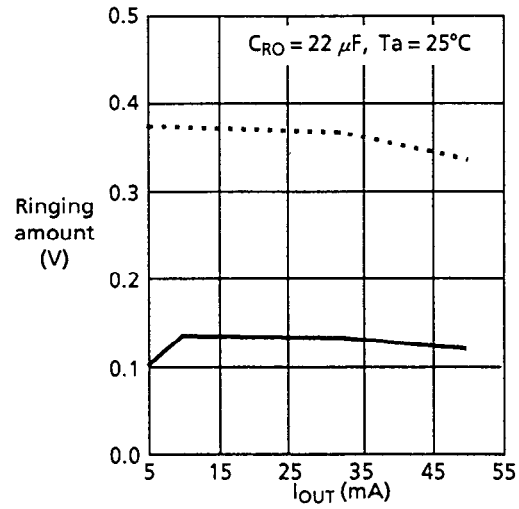
4.2 V_{RO} pin



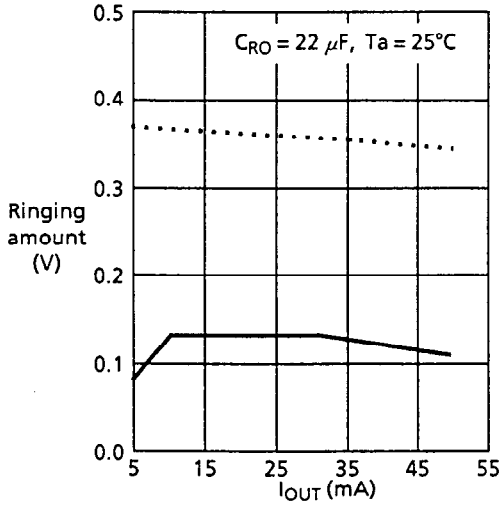
Reference data: Type II

1. I_{OUT} dependency

1.1 V_{OUT} pin

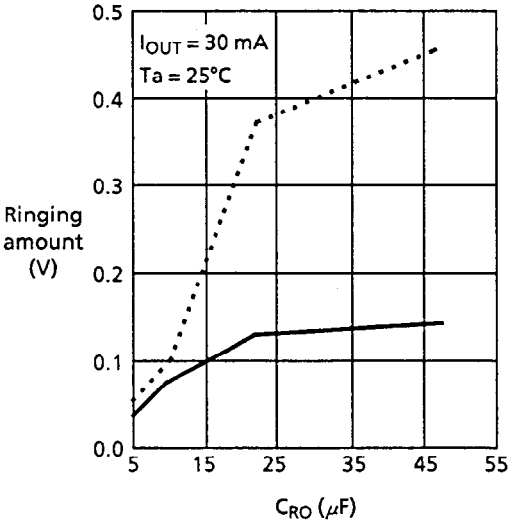


1.2 V_{RO} pin

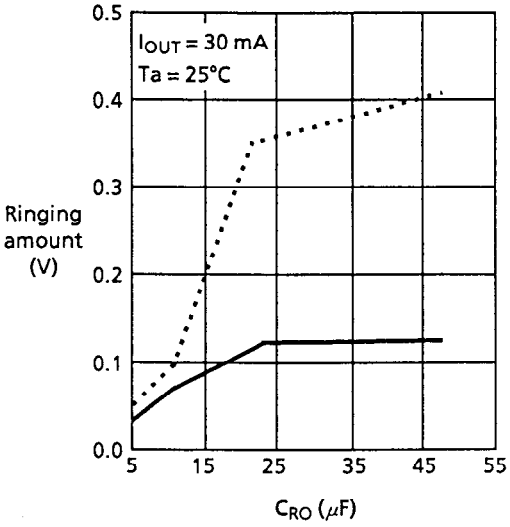


2. C_{RO} dependency

2.1 V_{OUT} pin

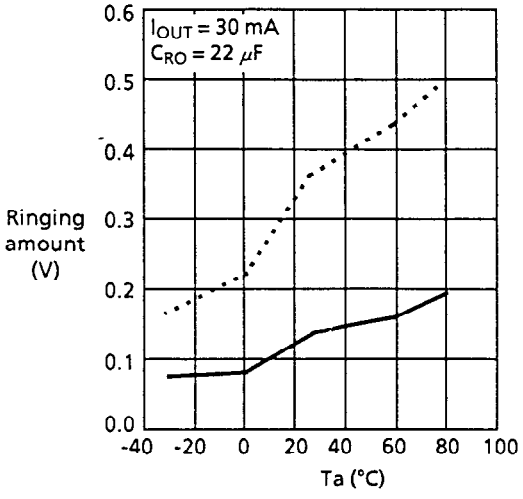


2.2 V_{RO} pin

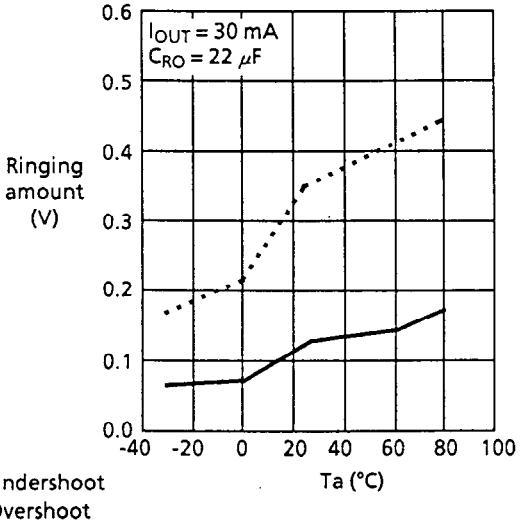


3. Temperature dependency

3.1 V_{OUT} pin



3.2 V_{RO} pin



——— Undershoot
- - - - - Overshoot

2. Load transient response based on output current fluctuation

The overshoot and undershoot is caused in the output voltage if the output current fluctuates between 10 μA and 30 mA while the input voltage is costant. Figure 16 shows the output voltage fluctuation due to change of output current. Figure 17 shows the measuring circuit for reference. The latter half of this section describes ringing waveform and parameter dependency.

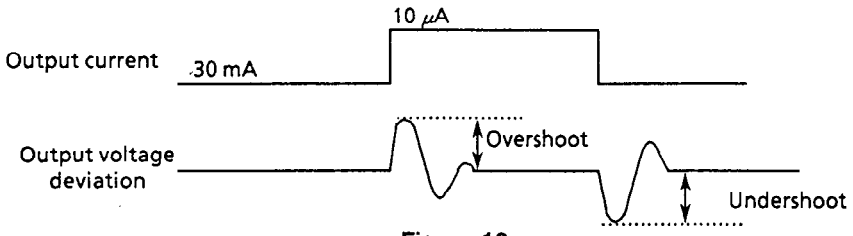


Figure 16

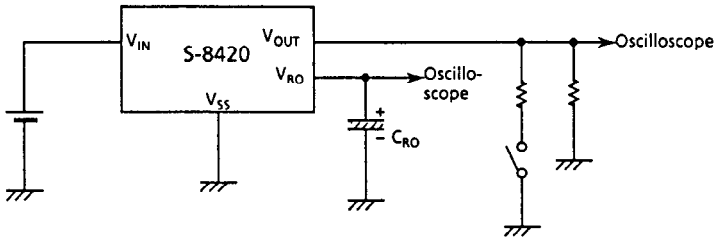
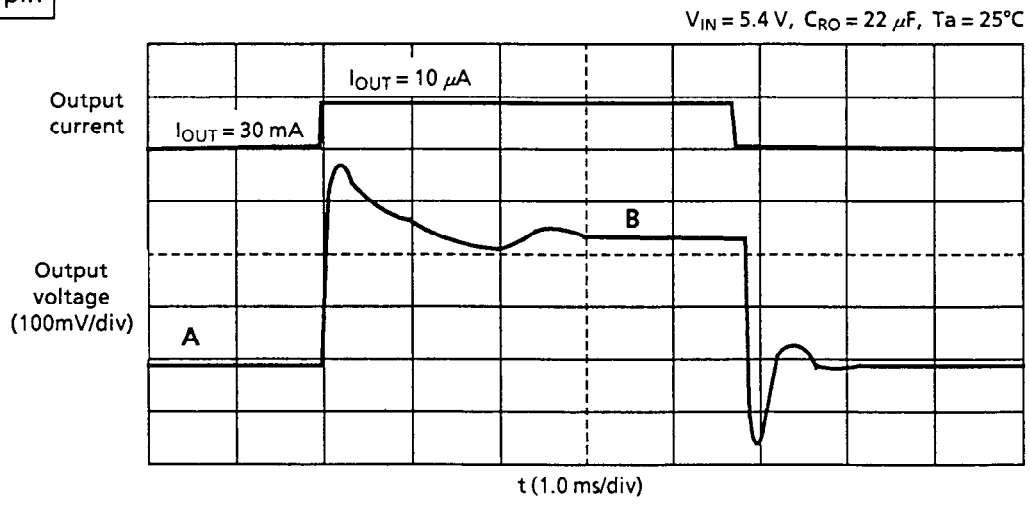


Figure 17 Measuring circuit

Output current fluctuation causes ringing. Figure 18 shows the ringing waveform at the V_{OUT} pin and Figure 19 shows that waveform at the V_{RO} pin.

V_{OUT} pin



The voltage drop of M1 causes a large difference between the ringing amounts of **A** and **B**.

Figure 18 Ringing waveform due to output current fluctuation (V_{OUT} pin)

V_{RO} pin

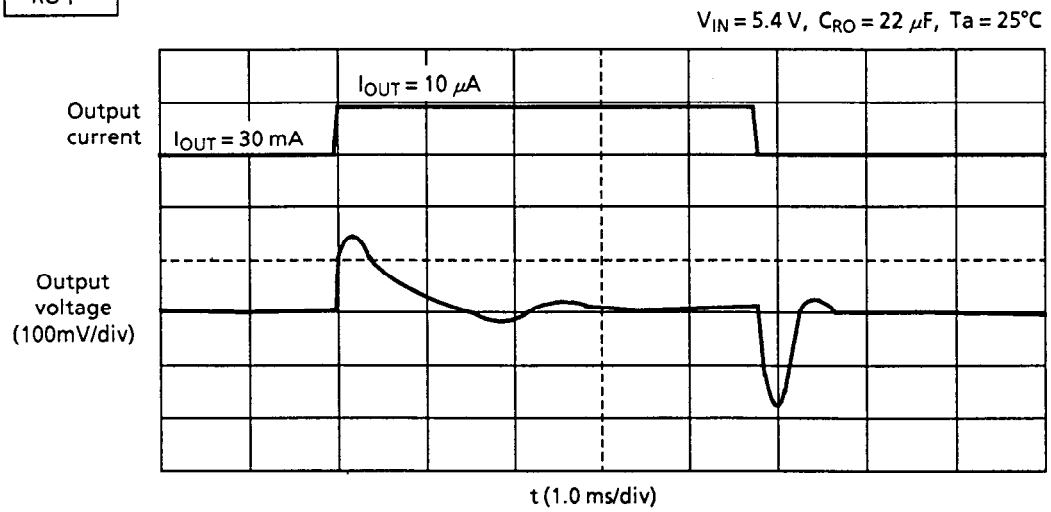


Figure 19 Ringing waveform due to output current fluctuation (V_{RO} pin)

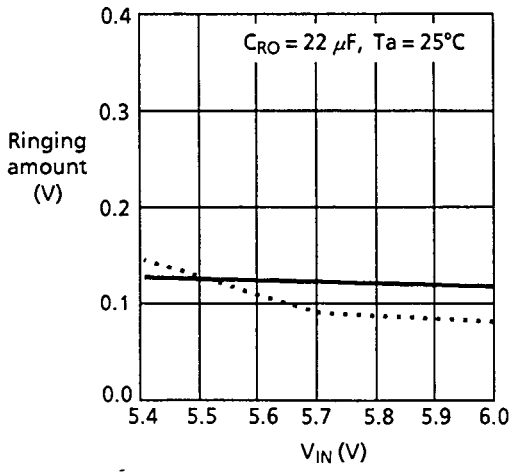
Table 8 Parameter dependency due to output current fluctuation

Parameter		Method to decrease overshoot	Method to decrease undershoot
Input voltage	V_{IN}	Increase	Increase
Load capacitance	C_{RO}	Increase	Increase
Temperature	Ta	No change	High temperature

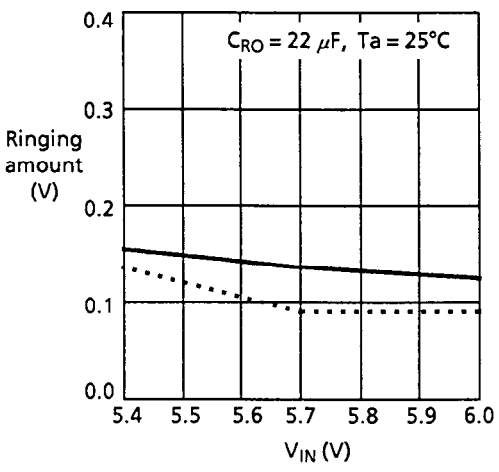
Reference data

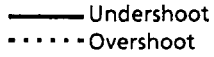
1. V_{IN} dependency

1.1 V_{OUT} pin



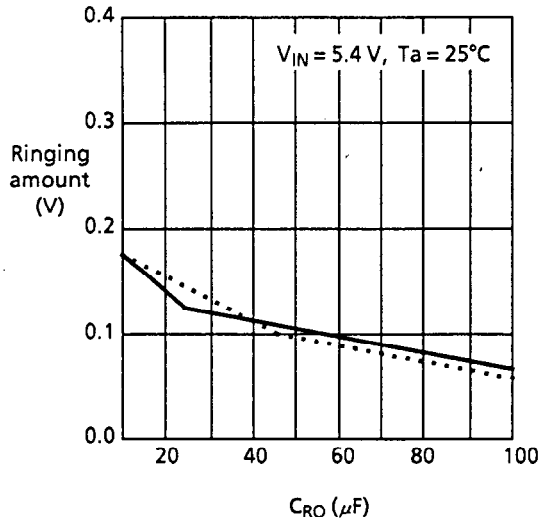
1.2 V_{RO} pin



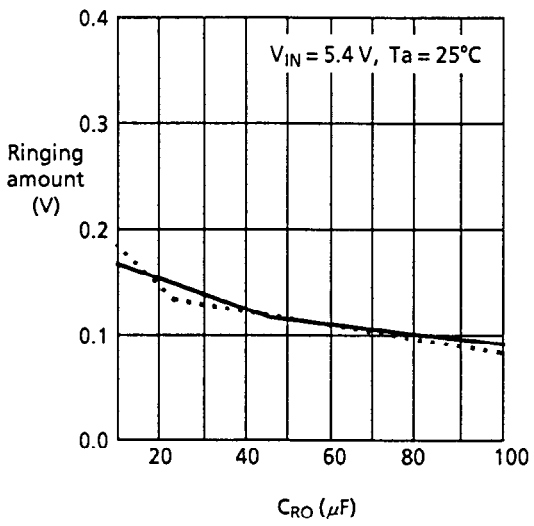


2. C_{RO} dependency

2.1 V_{OUT} pin

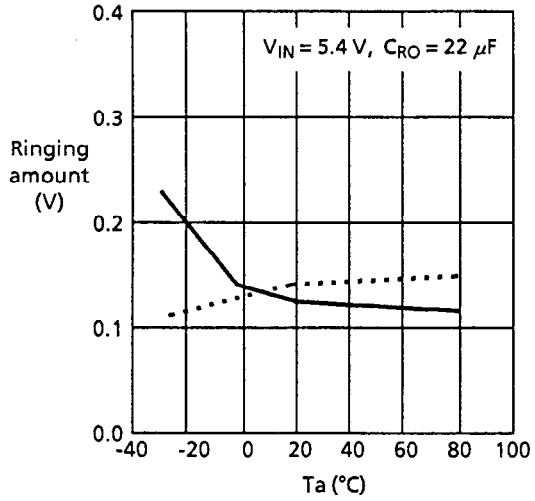


2.2 V_{RO} pin

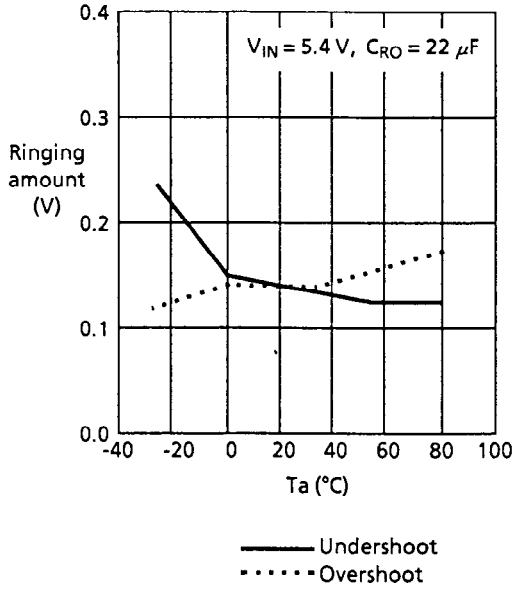


3. Temperature dependecy

3.1 V_{OUT} pin



3.2 V_{RO} pin



3. Selecting load capacitance

Results of 1 and 2 demonstrate that:

- The parameter dependencies of type I of input voltage fluctuation and output current fluctuation have the same tendency. However, the ringing amount is larger in type I.
- The parameter dependency of type II of input voltage fluctuation has the reverse tendency to that of type I and output current fluctuation.

Therefore, proper load capacitance is determined by types I and II of input voltage fluctuation.
For example, Figure 20 shows the type I undershoot amount and type II overshoot amount in the C_{RO} dependency at the V_{RO} pin. The type I undershoot crosses the type II overshoot where C_{RO} is 18 μF. Therefore, a load capacitor of 18 μF will keep both undrershoot and overshoot low. However, if the load capacitance is 10 μF or less, type I undershoot will increase. So, add a capacitor of at least 10 μF. The dependency of the ringing amount is the same for both the V_{OUT} and V_{RO} pins. (In this example, the V_{OUT} pin has no load capacitor attached, and has a little larger dependency than that at the V_{RO} pin.) Two 10μF capacitors at the V_{OUT} and V_{RO} pins suppress the ringing amount better than a 20μF capacitor at the V_{RO} pin.

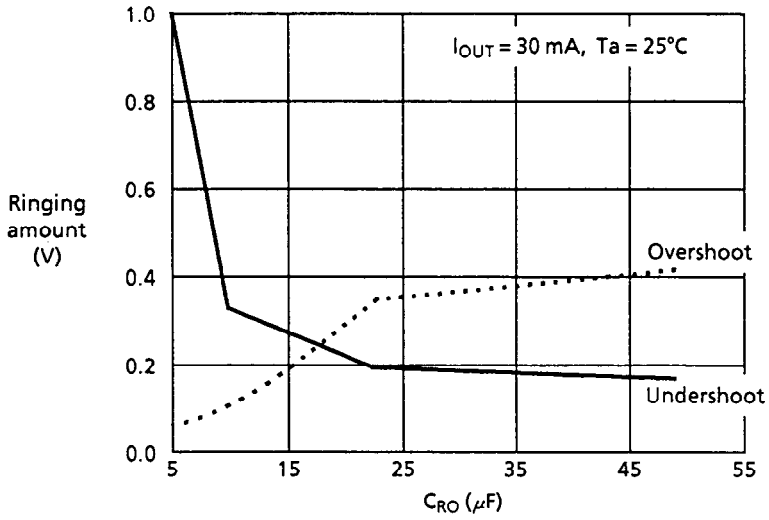


Figure 20

If IC chips or capacitors connected to the V_{RO} and V_{OUT} pins have sufficient room for overshoot and little room for undershoot (the V_{RO} output voltage is close to the detection voltage of the CS voltage detector), use of capacitors of 18 μF or more is recommended. In either case, check the temperature characteristics.

■ Standard Circuit

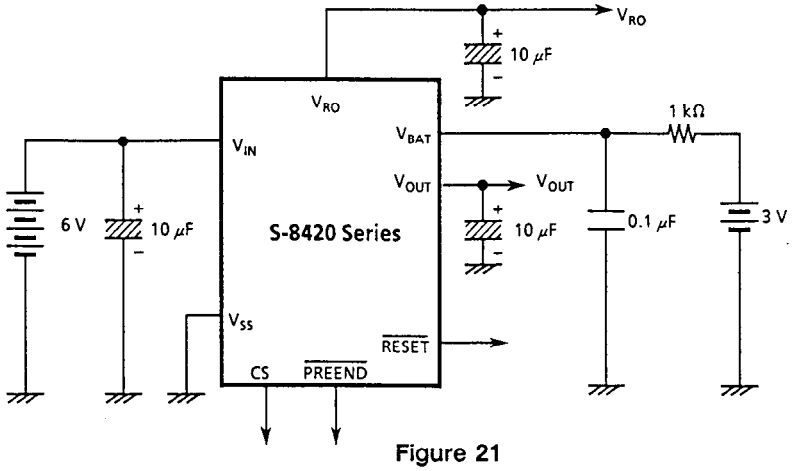


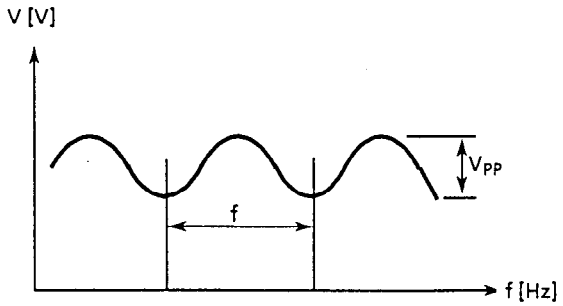
Figure 21

■ Merits In Designing

1. A switching circuit for main and backup power supplies is usually configured with discrete components. The S-8420 Series enables you to configure the circuit with a single chip.
   Some microcomputers can enter standby mode (or low clock mode) from normal mode (or high clock mode) only, and need about 5 V each time they are used. If a low voltage (such as the backup voltage) is applied to these microcomputers initially, they may run away and vast current consumption may flow. The S-8420 Series are designed to have a *special sequence* that stops the backup voltage until the main power supply voltage reaches the initial voltage that trips the switch.
2. Systems can be structured easily.
   Three types of built-in voltage detectors (CS, $\overline{\text{PREEND}}$, and $\overline{\text{RESET}}$) send three types of voltage detection signal to microcomputers.
3. Battery service life are prolonged.
   - The I/O voltage difference in the switch is very small (as small as that of a Schottky diode), and allows the batteries to be used until just before they are completely discharged.
   - The current consumption during backup operation is very small (3.6 μA max.), and allows the backup power supply to have a long service life.

■ Notes on Design

- In applications with small I_{RO} or I_{OUT}, output voltage (V_{RO}) may rise to cause the load stability to violate standards. Set I_{RO} and I_{OUT} to 10 μA or more.
- Attach the proper capacitor to the V_{RO} pin to prevent the CS voltage detector (which monitors the V_{RO} pin) from being active due to undershoot.
- Watch for overshoot and ensure it does not exceed the ratings of the IC chips and/or capacitors attached to the V_{RO} and V_{OUT} pins.
- Do not apply a ripple voltage of the conditions below to V_{IN} terminal.



$V_{PP} \geq 0.5V$
$f \geq 1000Hz$

Figure 22

- Consider the tolerable loss of the output transistor, particularly at high temperature.

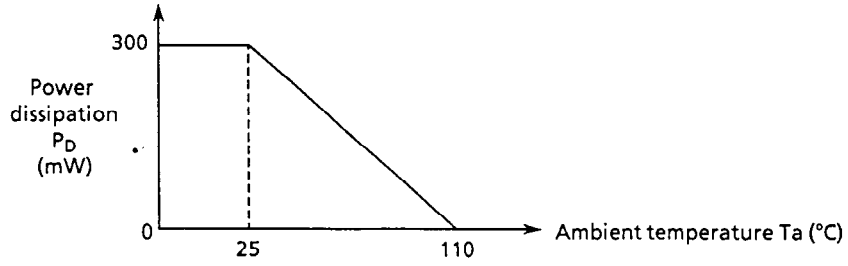


Figure 23 Power dissipation of 8-pin SOP

■ Application Circuits

1. When using a timer microcomputer for backup and displaying $\overline{\text{PREEND}}$ on the main CPU

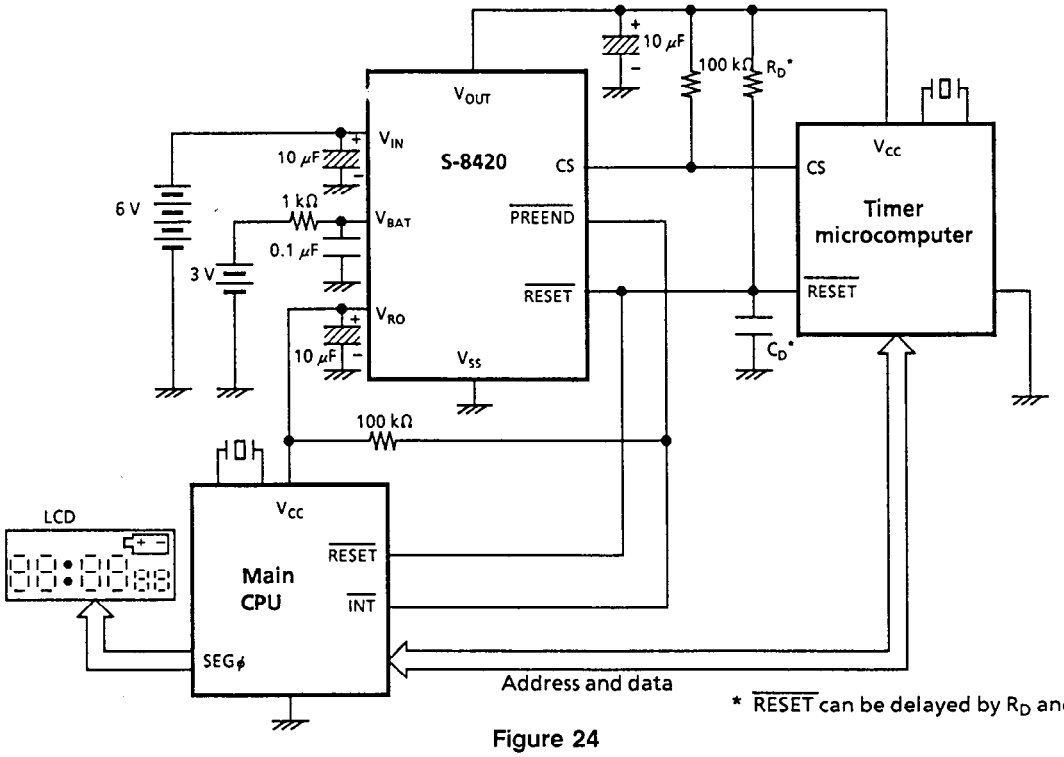


Figure 24

2. When adding delays to $\overline{\text{RESET}}$ to make it a RESET signal

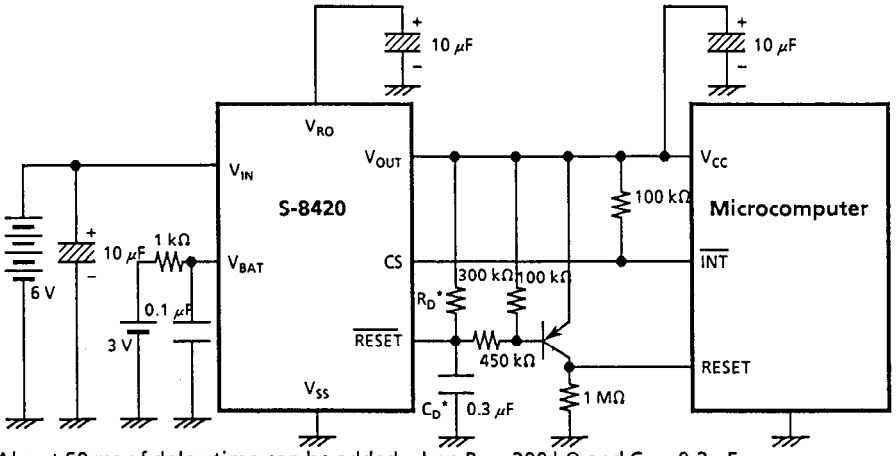


Figure 25

3. Memory card (when a voltage regulator is not used.)

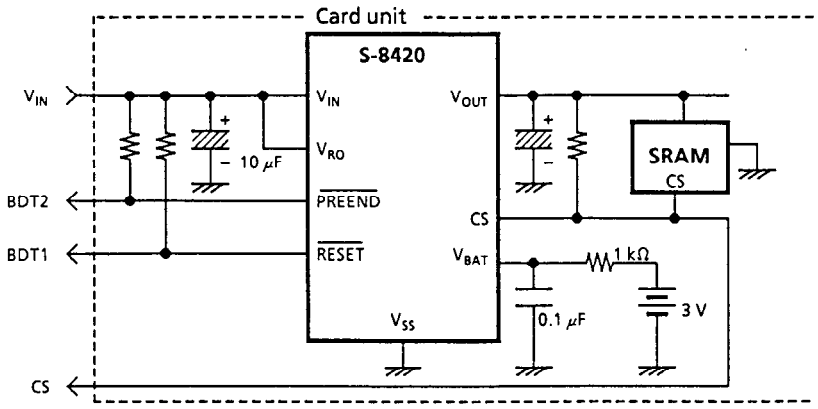


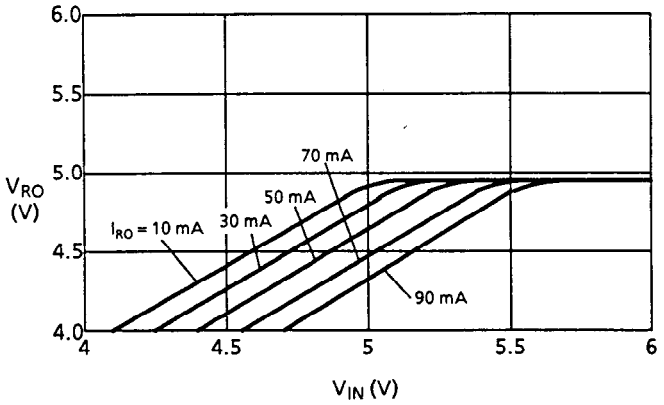
Figure 26

■ Characteristics

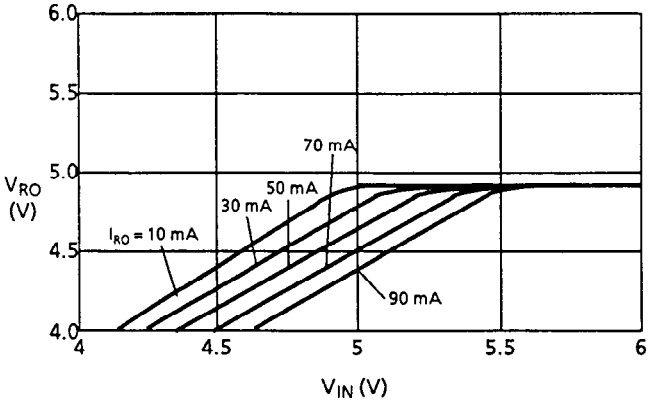
1. Voltage regulator

1.1 Input voltage – Output voltage

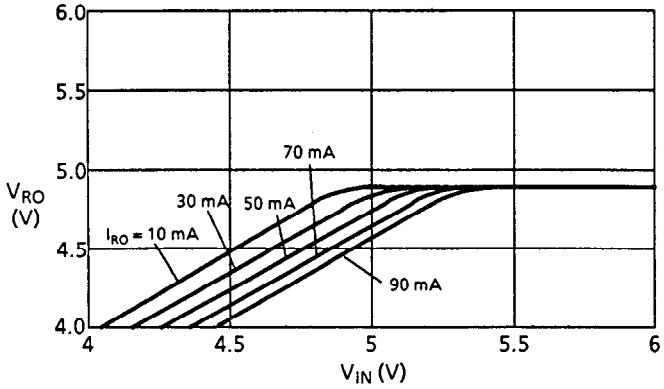
(1) Ta = 80°C



(2) Ta = 25°C

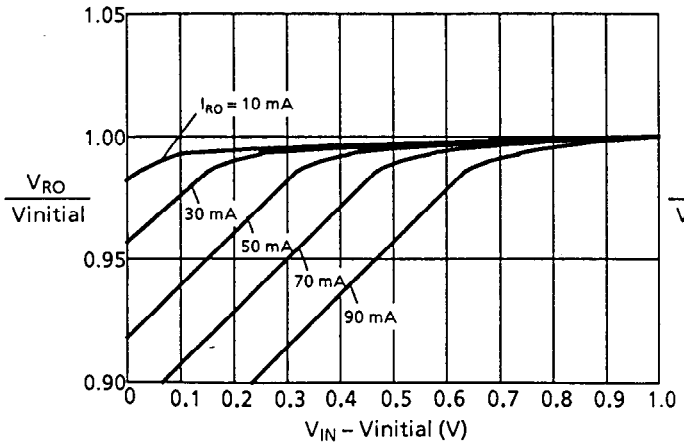


(3) Ta = -30°C

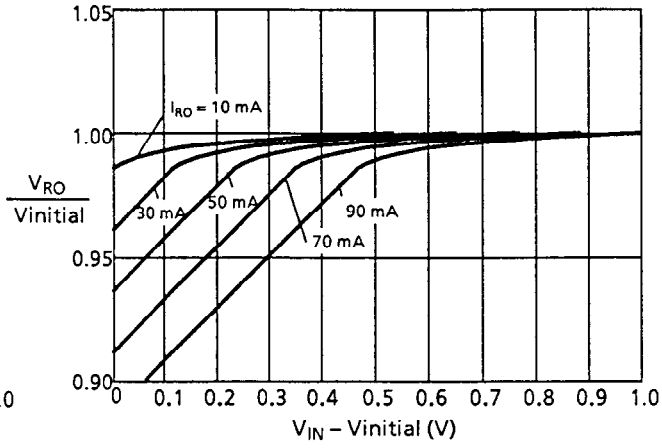


1.2 Input/output voltage difference – Output voltage

(1) Ta = 80°C

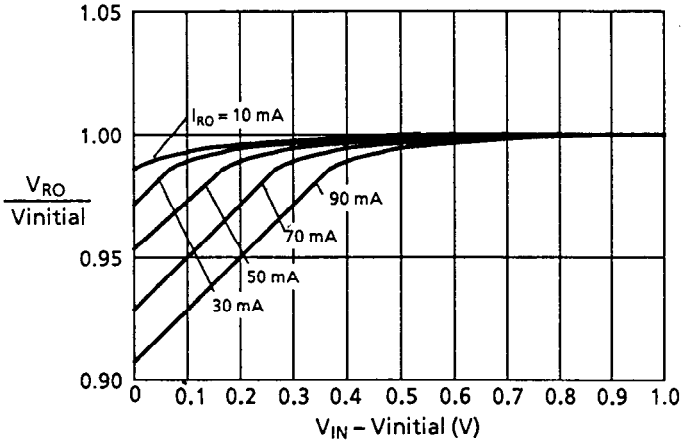


(2) Ta = 25°C



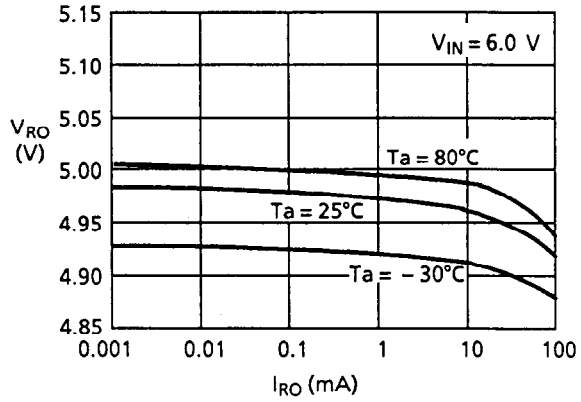
Vinitial : V_{RO} value when input voltage is 6 V.

(3) Ta = -30°C

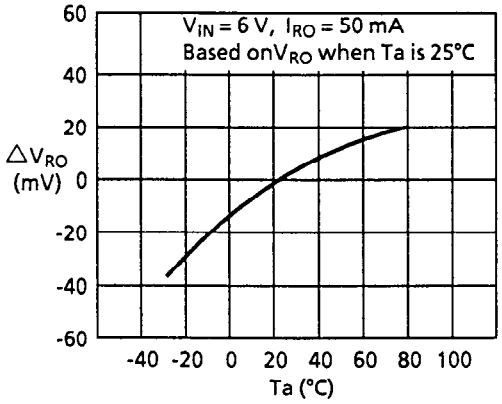


Vinitial : V_{RO} value when input voltage is 6 V.

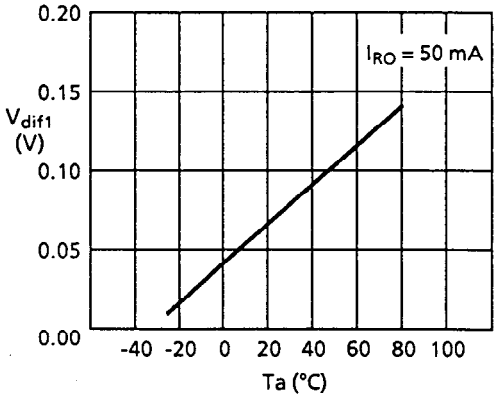
1.3 Output current – Output voltage



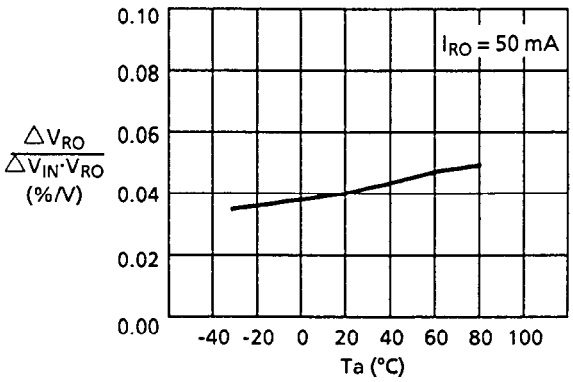
1.4 Output voltage – Temperature



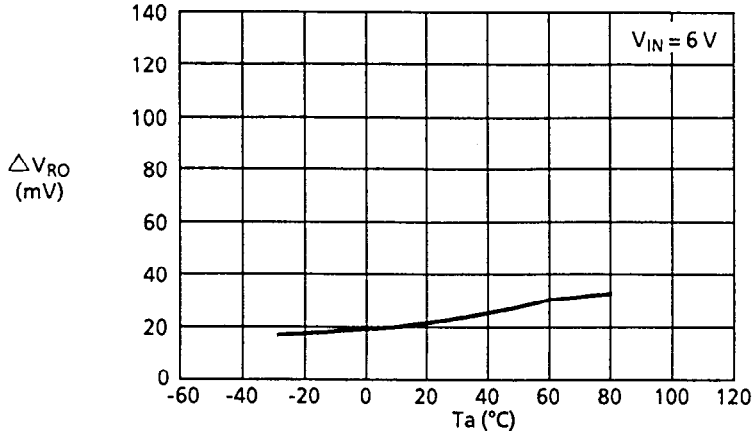
1.5 I/O voltage difference – Temperature



1.6 Line regulation – Temperature



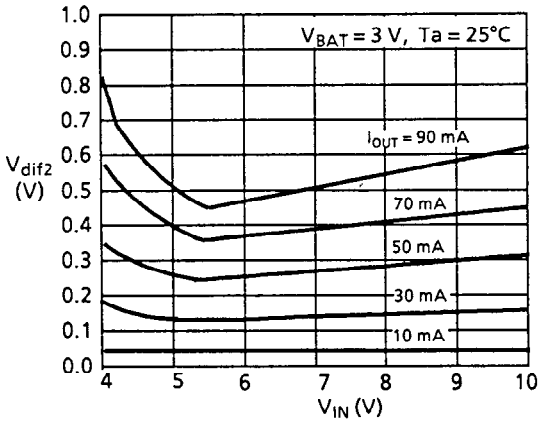
1.7 Load regulation – Temperature



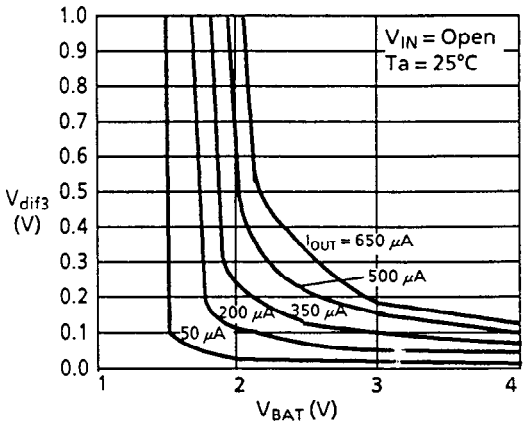
2. Switch

2.1 Input/output voltage difference

(1) V_{dif2}

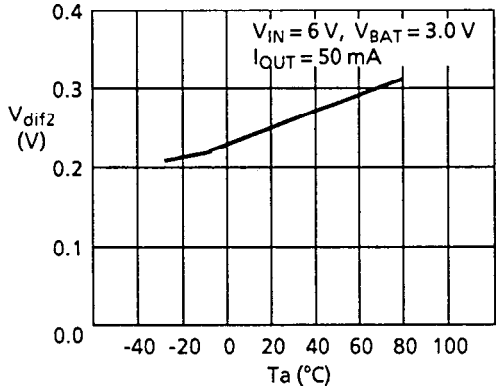


(2) V_{dif3}

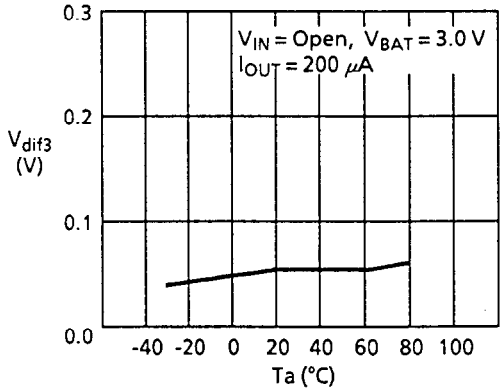


2.2 Input/output voltage difference – Temperature

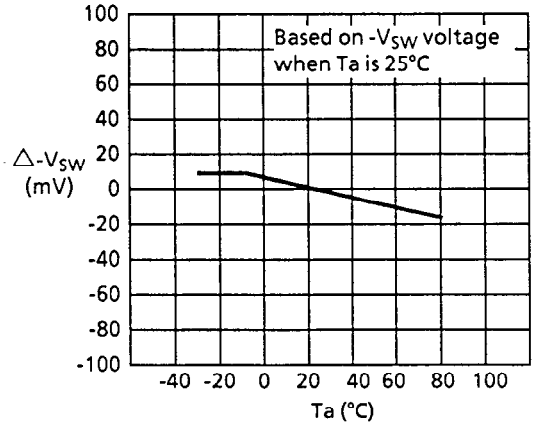
(1) V_{dif2}



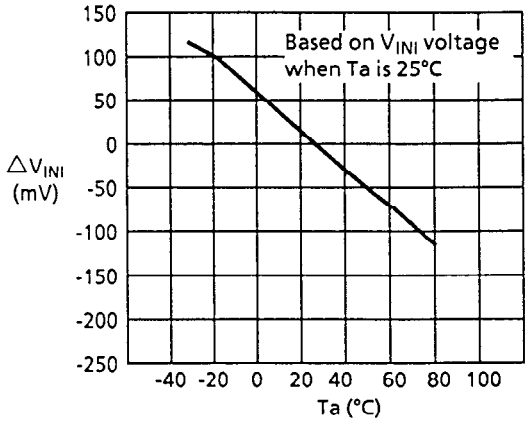
(2) V_{dif3}



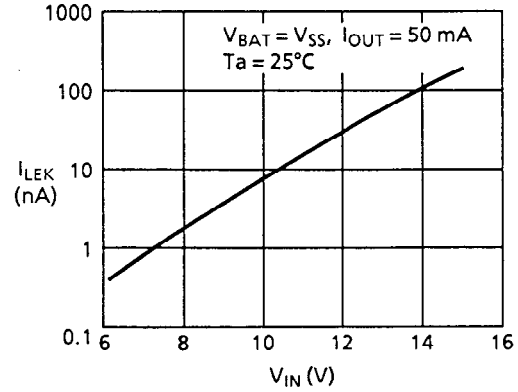
2.3 Switch voltage ($-V_{SW}$) – Temperature



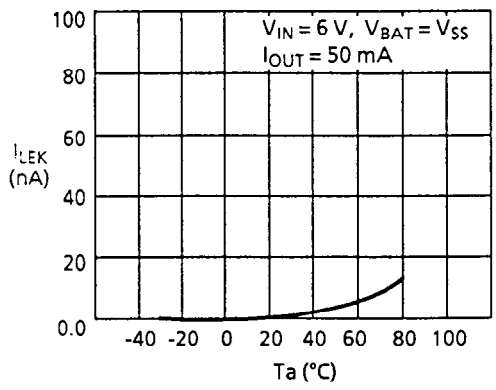
2.4 V_{INI} voltage – Temperature



2.5 Leakage current – Input voltage



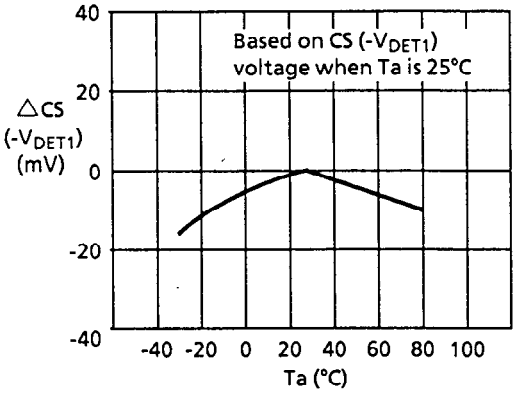
2.6 Leakage current – Temperature



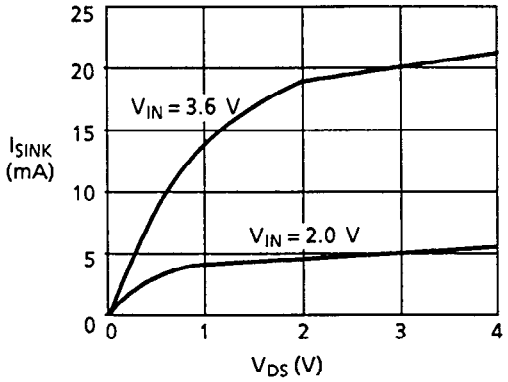
3. Voltage detectors

3.1 CS voltage detector

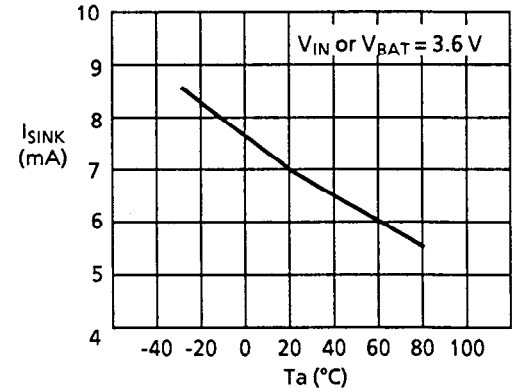
(1) Detection voltage – Temperature



(2) Output current

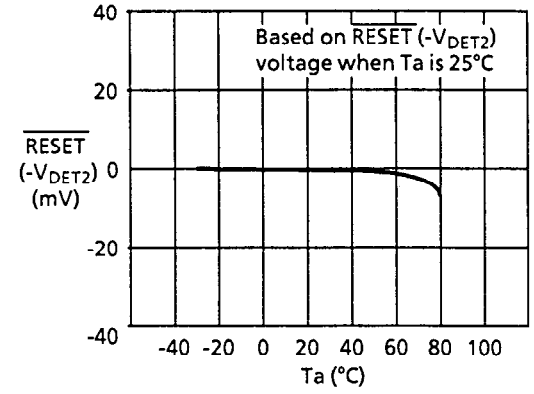


(3) Output current – Temperature

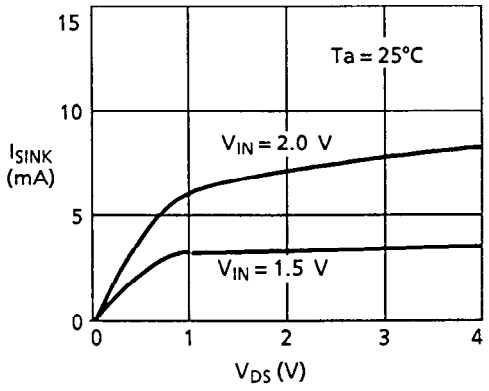


3.2 $\overline{\text{RESET}}$ voltage detector

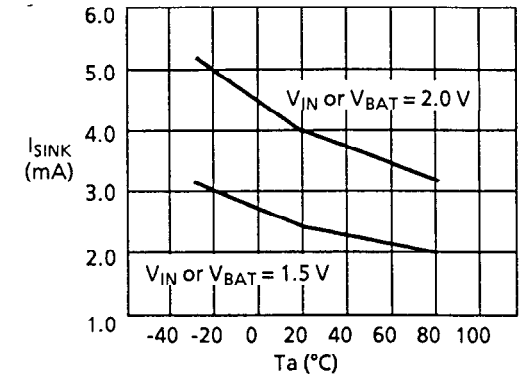
(1) Detection voltage – Temperature



(2) Output current

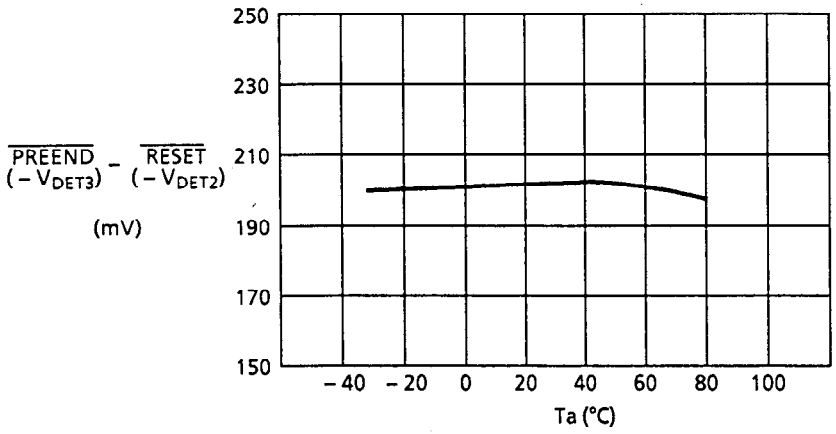


(3) Output current – Temperature

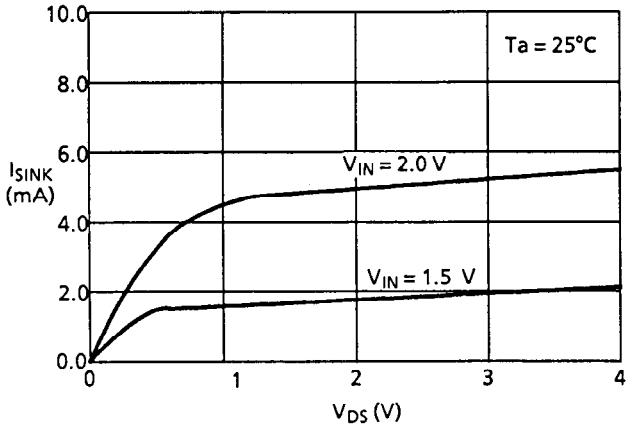


3.3 $\overline{\text{PREEND}}$ voltage detector

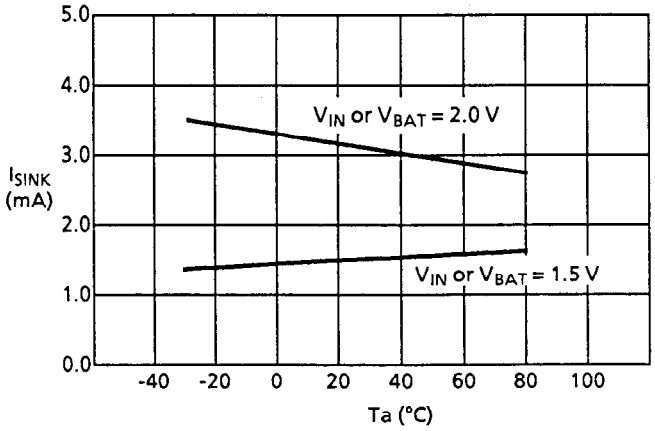
(1) Temperature characteristic of difference between $\overline{\text{PREEND}}$ and $\overline{\text{RESET}}$ detection voltages



(2) Output current

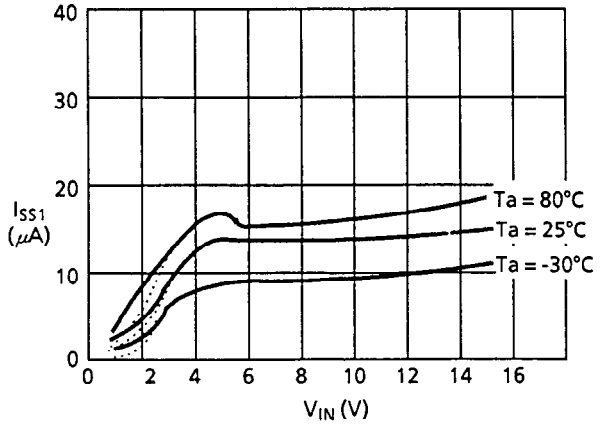


(3) Output current – Temperature

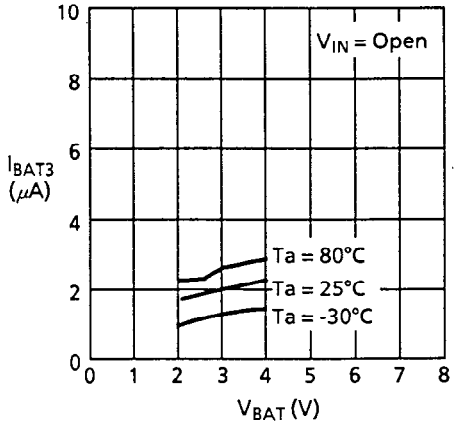


4. Current consumption

4.1 V_{IN} – I_{SS1}



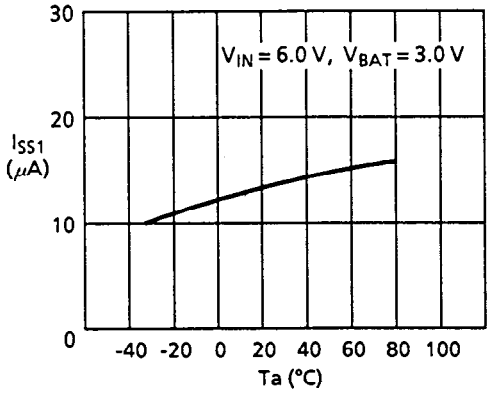
4.2 V_{BAT} – I_{BAT3}



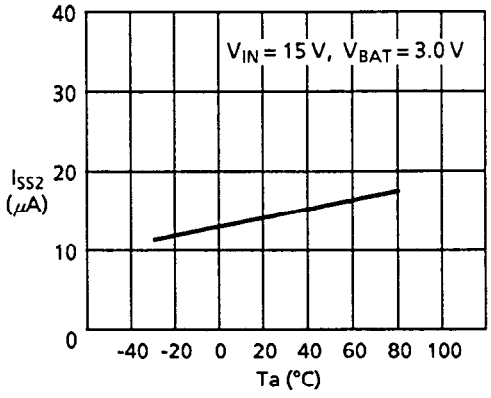
——— V_{BAT} = Open
------ V_{BAT} = 3 V applied

4.3 Temperature

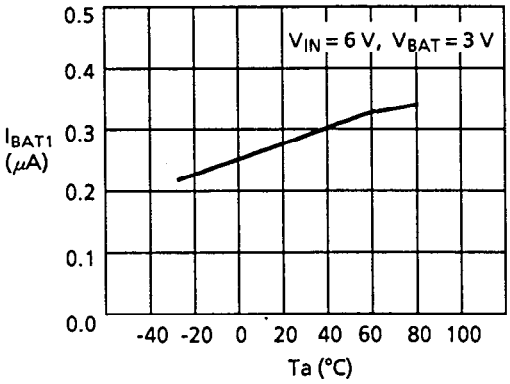
(1) I_{SS1}



(2) I_{SS2}



(3) I_{BAT1}



(4) I_{BAT3}

