

## LOW CURRENT CONSUMPTION WATCHDOG TIMER WITH RESET FUNCTION

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The S-1410/1411 Series is a watchdog timer developed using CMOS technology, which can operate with low current consumption of 3.8  $\mu$ A typ. The reset function and the low voltage detection function are available.

### ■ Features

- Detection voltage: 2.0 V to 5.0 V, selectable in 0.1 V step
- Detection voltage accuracy:  $\pm 1.5\%$
- Input voltage:  $V_{DD} = 0.9$  V to 6.0 V
- Hysteresis width: 5% typ.
- Current consumption: 3.8  $\mu$ A typ.
- Reset time-out period: 14.5 ms typ. ( $C_{POR} = 2200$  pF)
- Watchdog operation is switchable: Enable, Disable
- Watchdog operation voltage range: 2.5 V to 6.0 V
- Watchdog mode switching function\*1: Time-out mode, window mode
- Watchdog input edge is selectable: Rising edge, falling edge, both rising and falling edges
- Product type is selectable: S-1410 Series  
(Product with  $\overline{W}$  / T pin (Output:  $\overline{WDO}$  pin))  
S-1411 Series  
(Product without  $\overline{W}$  / T pin (Output:  $\overline{RST}$  pin,  $\overline{WDO}$  pin))
- Operation temperature range:  $T_a = -40^\circ\text{C}$  to  $+105^\circ\text{C}$
- Lead-free (Sn 100%), halogen-free

\*1. The S-1411 Series is fixed to the window mode.

### ■ Applications

- Power supply monitoring of microcontroller mounted apparatus and system monitoring

### ■ Packages

- TMSOP-8
- HSNT-8(2030)

## ■ Block Diagrams

### 1. S-1410 Series (Product with $\overline{W}$ / T pin)

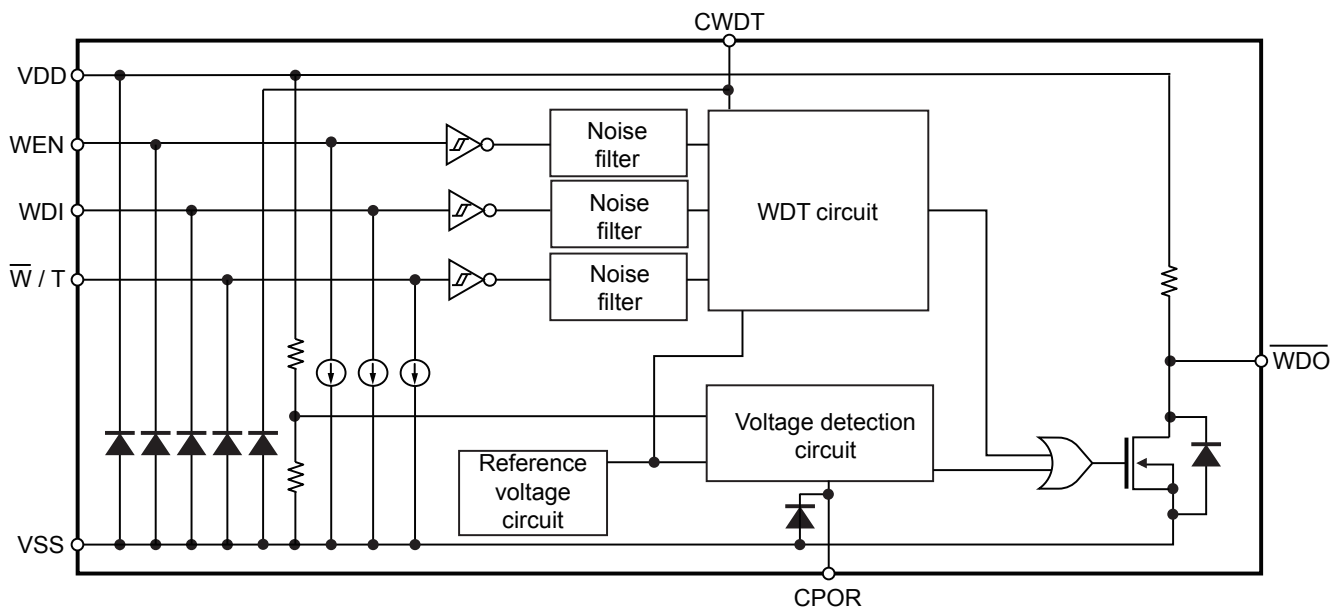


Figure 1

### 2. S-1411 Series (Product without $\overline{W}$ / T pin)

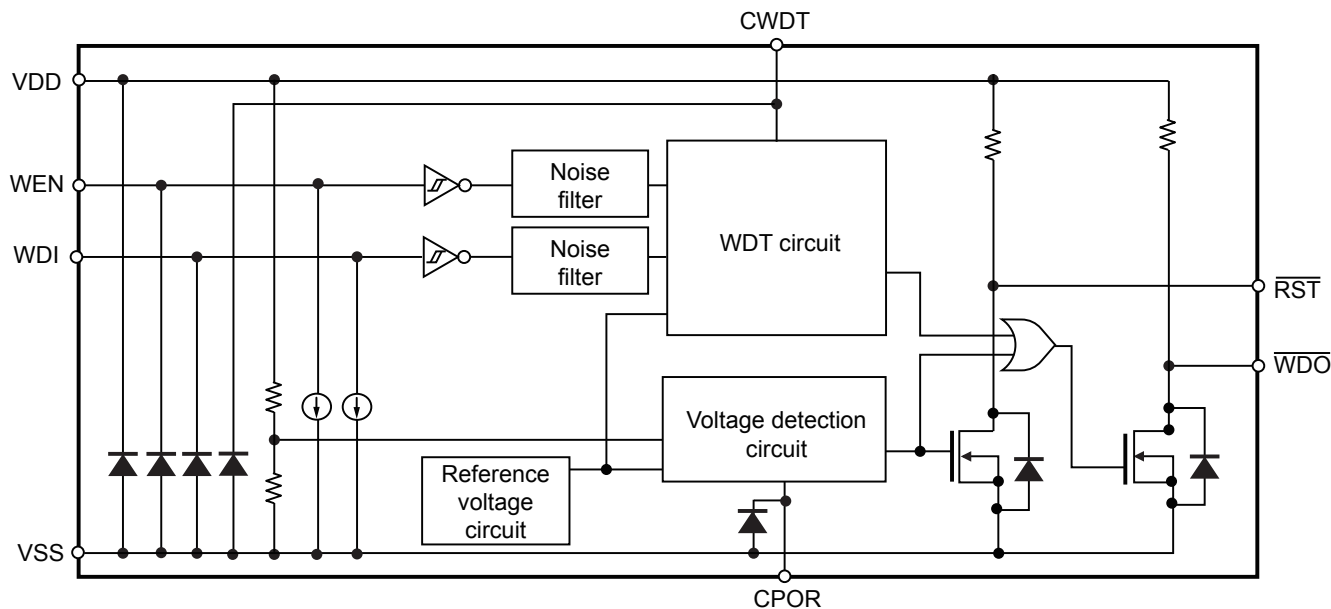
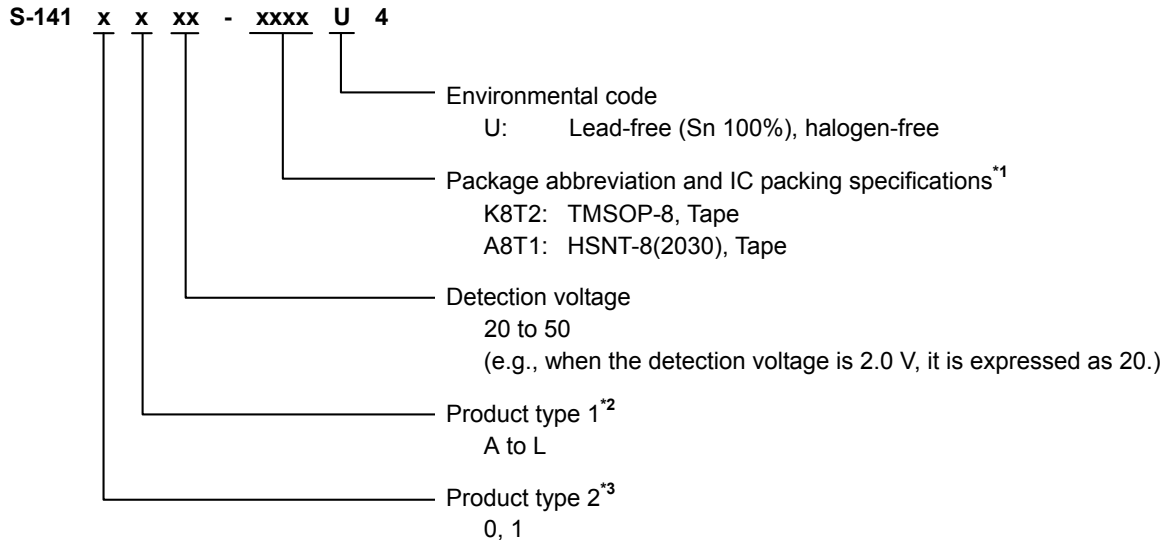


Figure 2

## ■ Product Name Structure

Users can select the product type, detection voltage, and package type for the S-1410/1411 Series. Refer to "1. **Product name**" regarding the contents of product name, "2. **Product type list**" regarding the product types, "3. **Packages**" regarding the package drawings.

### 1. Product name



\*1. Refer to the tape drawing.

\*2. Refer to "2. **Product type list**".

\*3. 0: S-1410 Series (Product with  $\overline{W}$  / T pin)

The  $\overline{WDO}$  pin outputs the signals which are from the watchdog timer circuit and the voltage detection circuit.

1: S-1411 Series (Product without  $\overline{W}$  / T pin)

The  $\overline{WDO}$  pin outputs the signals which are from the watchdog timer circuit and the voltage detection circuit.

The  $\overline{RST}$  pin outputs the signal which is from the voltage detection circuit.

The watchdog mode is fixed to the window mode.

## 2. Product type list

**Table 1**

| Product Type | WEN Pin Logic | Input Edge                    | Output Pull-up Resistor |
|--------------|---------------|-------------------------------|-------------------------|
| A            | Active "H"    | Rising edge                   | Available               |
| B            | Active "H"    | Falling edge                  | Available               |
| C            | Active "H"    | Both rising and falling edges | Available               |
| D            | Active "L"    | Rising edge                   | Available               |
| E            | Active "L"    | Falling edge                  | Available               |
| F            | Active "L"    | Both rising and falling edges | Available               |
| G            | Active "H"    | Rising edge                   | Unavailable             |
| H            | Active "H"    | Falling edge                  | Unavailable             |
| I            | Active "H"    | Both rising and falling edges | Unavailable             |
| J            | Active "L"    | Rising edge                   | Unavailable             |
| K            | Active "L"    | Falling edge                  | Unavailable             |
| L            | Active "L"    | Both rising and falling edges | Unavailable             |

## 3. Packages

**Table 2 Package Drawing Codes**

| Package Name | Dimension    | Tape         | Reel         | Land         |
|--------------|--------------|--------------|--------------|--------------|
| TMSOP-8      | FM008-A-P-SD | FM008-A-C-SD | FM008-A-R-SD | –            |
| HSNT-8(2030) | PP008-A-P-SD | PP008-A-C-SD | PP008-A-R-SD | PP008-A-L-SD |

## ■ Pin Configuration

### 1. TMSOP-8

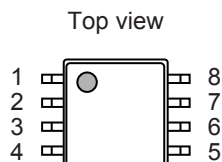


Figure 3

Table 3 S-1410 Series (Product with  $\overline{W}$  / T pin)

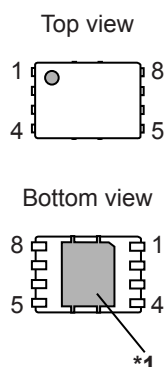
| Pin No. | Symbol                           | Description                          |
|---------|----------------------------------|--------------------------------------|
| 1       | $\overline{W}$ / T <sup>*1</sup> | Watchdog mode switching pin          |
| 2       | CPOR                             | Reset time-out period adjustment pin |
| 3       | CWDT                             | Watchdog time adjustment pin         |
| 4       | VSS                              | GND pin                              |
| 5       | WEN                              | Watchdog enable pin                  |
| 6       | $\overline{WDO}$                 | Watchdog output pin                  |
| 7       | WDI                              | Watchdog input pin                   |
| 8       | VDD                              | Voltage input pin                    |

Table 4 S-1411 Series (Product without  $\overline{W}$  / T pin)

| Pin No. | Symbol            | Description                          |
|---------|-------------------|--------------------------------------|
| 1       | RST $\overline{}$ | Reset output pin                     |
| 2       | CPOR              | Reset time-out period adjustment pin |
| 3       | CWDT              | Watchdog time adjustment pin         |
| 4       | VSS               | GND pin                              |
| 5       | WEN               | Watchdog enable pin                  |
| 6       | $\overline{WDO}$  | Watchdog output pin                  |
| 7       | WDI               | Watchdog input pin                   |
| 8       | VDD               | Voltage input pin                    |

- \*1.  $\overline{W}$  / T pin = "H": Time-out mode  
 $\overline{W}$  / T pin = "L": Window mode

**2. HSNT-8(2030)**



**Figure 4**

**Table 5 S-1410 Series (Product with  $\overline{W}$  / T pin)**

| Pin No. | Symbol                          | Description                          |
|---------|---------------------------------|--------------------------------------|
| 1       | $\overline{W}$ / T <sup>2</sup> | Watchdog mode switching pin          |
| 2       | CPOR                            | Reset time-out period adjustment pin |
| 3       | CWDT                            | Watchdog time adjustment pin         |
| 4       | VSS                             | GND pin                              |
| 5       | WEN                             | Watchdog enable pin                  |
| 6       | $\overline{WDO}$                | Watchdog output pin                  |
| 7       | WDI                             | Watchdog input pin                   |
| 8       | VDD                             | Voltage input pin                    |

**Table 6 S-1411 Series (Product without  $\overline{W}$  / T pin)**

| Pin No. | Symbol           | Description                          |
|---------|------------------|--------------------------------------|
| 1       | $\overline{RST}$ | Reset output pin                     |
| 2       | CPOR             | Reset time-out period adjustment pin |
| 3       | CWDT             | Watchdog time adjustment pin         |
| 4       | VSS              | GND pin                              |
| 5       | WEN              | Watchdog enable pin                  |
| 6       | $\overline{WDO}$ | Watchdog output pin                  |
| 7       | WDI              | Watchdog input pin                   |
| 8       | VDD              | Voltage input pin                    |

- \*1. Connect the heat sink of backside at shadowed area to the board, and set electric potential open or GND.  
 However, do not use it as the function of electrode.
- \*2.  $\overline{W}$  / T pin = "H": Time-out mode  
 $\overline{W}$  / T pin = "L": Window mode

## ■ Pin Functions

Refer to "■ Operation" for details.

### 1. $\overline{W}$ / T pin (S-1410 Series only)

This is a pin to switch the watchdog mode.

The S-1410 Series changes to the time-out mode when the  $\overline{W}$  / T pin is "H", and changes to the window mode when the  $\overline{W}$  / T pin is "L". Switching the mode is prohibited during the operation.

The constant current source (0.3  $\mu$ A typ.) is connected to the  $\overline{W}$  / T pin, and it is pulled down internally.

#### 1.1 Time-out mode ( $\overline{W}$ / T pin = "H")

The S-1410 Series detects an abnormality when not inputting an edge to the WDI pin during the watchdog time-out period ( $t_{WDU}$ ). And then "L" is output from the  $\overline{WDO}$  pin.

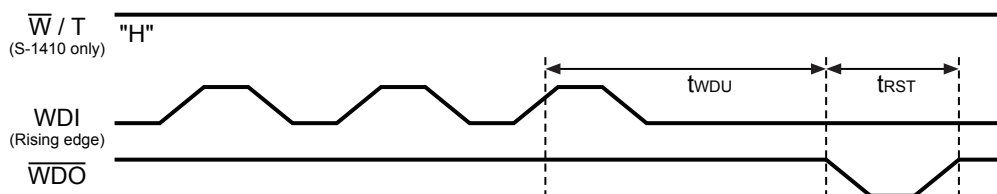


Figure 5 Abnormality Detection in Time-out Mode

#### 1.2 Window mode ( $\overline{W}$ / T pin = "L")

When not inputting an edge to the WDI pin during  $t_{WDU}$ , or when an edge is input to the WDI pin again within a specific period of time (the discharge time due to an edge detection + 1 charge-discharge time ( $t_{WDL}$ )) after inputting an edge to the WDI pin, the  $\overline{WDO}$  pin output changes from "H" to "L".

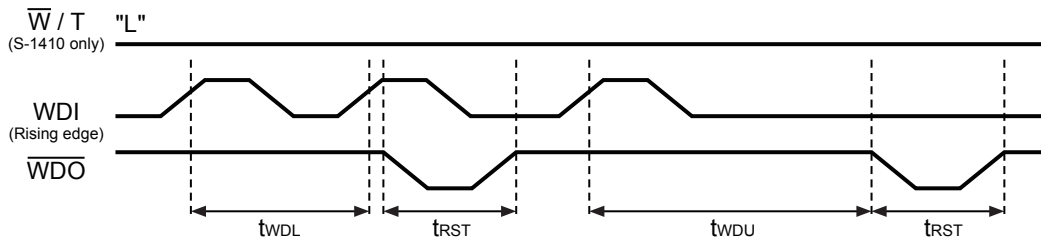


Figure 6 Abnormality Detection in Window Mode

### 2. $\overline{RST}$ pin (S-1411 Series only)

This is a reset output pin. It outputs "L" when detecting a low voltage.

Be sure to connect a pull-up resistor to the  $\overline{RST}$  pin in the product without an output pull-up resistor.

### 3. CPOR pin

This is a pin to connect an external capacitor in order to generate the reset time-out period ( $t_{RST}$ ).

The capacitor is charged and discharged by an internal constant current circuit, and the charge-discharge duration is  $t_{RST}$ .

$t_{RST}$  is calculated by using the following equation.

$$t_{RST} = 6,500,000 \times C_{POR} [F] + 0.0002$$

#### **4. CWDT pin**

This is a pin to connect an external capacitor in order to generate the watchdog time-out period ( $t_{WDU}$ ) and the watchdog double pulse detection time ( $t_{WDL}$ ). The capacitor is charged and discharged by an internal constant current circuit.

$t_{WDU}$  is calculated by using the following equation.

$$t_{WDU} = 50,000,000 \times C_{WDT} [F] + 0.0011$$

Moreover,  $t_{WDL}$  is calculated by using the following equation.

$$t_{WDL} = \frac{t_{WDU}}{32}$$

#### **5. WEN pin**

This is a pin to switch Enable / Disable of the watchdog timer.

When the WEN pin logic is active "H", the watchdog timer becomes Enable if the input is "H", and the charge-discharge operation is performed at the CWDT pin. In the active "H" product, the constant current source (0.3  $\mu$ A typ.) is connected to the WEN pin, and it is pulled down internally.

#### **6. $\overline{WDO}$ pin**

This pin combines the reset output and the watchdog output.

Be sure to connect a pull-up resistor to the  $\overline{WDO}$  pin in the product without an output pull-up resistor.

#### **7. WDI pin**

This is an input pin to receive a signal from the monitored object. By being input an edge at an appropriate timing, the WDI pin confirms the normal operation of the monitored object.

The constant current source (0.3  $\mu$ A typ.) is connected to the WDI pin, and it is pulled down internally.



## ■ Absolute Maximum Ratings

**Table 7**

(Ta = +25°C unless otherwise specified)

| Item                           |                            | Symbol                                     | Absolute Maximum Rating                                                | Unit |
|--------------------------------|----------------------------|--------------------------------------------|------------------------------------------------------------------------|------|
| VDD pin voltage                |                            | V <sub>DD</sub>                            | V <sub>SS</sub> – 0.3 to V <sub>SS</sub> + 7.0                         | V    |
| WDI pin voltage                |                            | V <sub>WDI</sub>                           | V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.3 ≤ V <sub>SS</sub> + 7.0 | V    |
| WEN pin voltage                |                            | V <sub>WEN</sub>                           | V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.3 ≤ V <sub>SS</sub> + 7.0 | V    |
| $\overline{W}$ / T pin voltage |                            | V <sub><math>\overline{W}</math> / T</sub> | V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.3 ≤ V <sub>SS</sub> + 7.0 | V    |
| CPOR pin voltage               |                            | V <sub>CPOR</sub>                          | V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.3 ≤ V <sub>SS</sub> + 7.0 | V    |
| CWDT pin voltage               |                            | V <sub>CWDT</sub>                          | V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.3 ≤ V <sub>SS</sub> + 7.0 | V    |
| $\overline{RST}$ pin voltage   | A / B / C / D / E / F type | V <sub>RST</sub>                           | V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.3 ≤ V <sub>SS</sub> + 7.0 | V    |
|                                | G / H / I / J / K / L type |                                            | V <sub>SS</sub> – 0.3 to V <sub>SS</sub> + 7.0                         | V    |
| $\overline{WDO}$ pin voltage   | A / B / C / D / E / F type | V <sub>WDO</sub>                           | V <sub>SS</sub> – 0.3 to V <sub>DD</sub> + 0.3 ≤ V <sub>SS</sub> + 7.0 | V    |
|                                | G / H / I / J / K / L type |                                            | V <sub>SS</sub> – 0.3 to V <sub>SS</sub> + 7.0                         | V    |
| Operation ambient temperature  |                            | T <sub>opr</sub>                           | –40 to +105                                                            | °C   |
| Storage temperature            |                            | T <sub>stg</sub>                           | –40 to +150                                                            | °C   |

**Caution** The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

## ■ Thermal Resistance Value

**Table 8**

| Item                                                 | Symbol        | Condition    |         | Min. | Typ. | Max. | Unit |
|------------------------------------------------------|---------------|--------------|---------|------|------|------|------|
| Junction-to-ambient thermal resistance <sup>*1</sup> | $\theta_{ja}$ | TMSOP-8      | Board 1 | –    | 160  | –    | °C/W |
|                                                      |               |              | Board 2 | –    | 133  | –    | °C/W |
|                                                      |               | HSNT-8(2030) | Board 1 | –    | 181  | –    | °C/W |
|                                                      |               |              | Board 2 | –    | 135  | –    | °C/W |

<sup>\*1</sup>. Test environment: compliance with JEDEC STANDARD JESD51-2A

**Remark** Refer to "■ Thermal Characteristics" for details of power dissipation and test board.

■ **Electrical Characteristics**

**Table 9 (1 / 2)**

(WEN pin logic active "H" product,  $V_{DD} = 5.0 \text{ V}$ ,  $T_a = +25^\circ\text{C}$  unless otherwise specified)

| Item                                 | Symbol             | Condition                                                                |                         | Min.                         | Typ.                     | Max.                         | Unit | Test Circuit |
|--------------------------------------|--------------------|--------------------------------------------------------------------------|-------------------------|------------------------------|--------------------------|------------------------------|------|--------------|
| Detection voltage*1                  | −V <sub>DET</sub>  | −                                                                        |                         | −V <sub>DET(S)</sub> × 0.985 | −V <sub>DET(S)</sub>     | −V <sub>DET(S)</sub> × 1.015 | V    | 1            |
| Hysteresis width                     | V <sub>HYS</sub>   | −                                                                        |                         | −V <sub>DET</sub> × 0.03     | −V <sub>DET</sub> × 0.05 | −V <sub>DET</sub> × 0.07     | V    | 1            |
| Current consumption during operation | I <sub>SS1</sub>   | When watchdog timer operates                                             |                         | −                            | 3.8                      | 7.8                          | μA   | 2            |
| Reset time-out period                | t <sub>RST</sub>   | C <sub>POR</sub> = 2200 pF                                               |                         | 8.7                          | 14.5                     | 20                           | ms   | 3            |
| Watchdog time-out period             | t <sub>WDU</sub>   | C <sub>WDT</sub> = 470 pF                                                |                         | 15                           | 24.6                     | 34                           | ms   | 3            |
| Watchdog double pulse detection time | t <sub>WDL</sub>   | C <sub>WDT</sub> = 470 pF                                                |                         | 461                          | 769                      | 1077                         | μs   | 4            |
| Reset output voltage "H"             | V <sub>ROH</sub>   | S-1411 Series A / B / C / D / E / F type only                            |                         | V <sub>DD</sub> − 1.0        | −                        | −                            | V    | 5            |
| Reset output voltage "L"             | V <sub>ROL</sub>   | −                                                                        |                         | −                            | −                        | 0.4                          | V    | 6            |
| Reset output pull-up current         | I <sub>RUP</sub>   | V <sub>RST</sub> = 0 V,<br>S-1411 Series A / B / C / D / E / F type only |                         | −                            | −0.85                    | −0.4                         | μA   | 7            |
| Reset output current                 | I <sub>ROUT</sub>  | V <sub>DS</sub> = 0.4 V,<br>S-1411 Series only                           | V <sub>DD</sub> = 1.5 V | 0.6                          | 1.1                      | −                            | mA   | 8            |
|                                      |                    |                                                                          | V <sub>DD</sub> = 1.8 V | 1.1                          | 1.6                      | −                            | mA   | 8            |
|                                      |                    |                                                                          | V <sub>DD</sub> = 2.5 V | 2.1                          | 2.6                      | −                            | mA   | 8            |
|                                      |                    |                                                                          | V <sub>DD</sub> = 3.0 V | 2.8                          | 3.3                      | −                            | mA   | 8            |
| Reset output leakage current         | I <sub>RLEAK</sub> | V <sub>DS</sub> = 6.0 V, V <sub>DD</sub> = 6.0 V,<br>S-1411 Series only  |                         | −                            | −                        | 0.096                        | μA   | 9            |
| Watchdog output voltage "H"          | V <sub>WOH</sub>   | A / B / C / D / E / F type only                                          |                         | V <sub>DD</sub> − 1.0        | −                        | −                            | V    | 10           |
| Watchdog output voltage "L"          | V <sub>WOL</sub>   | −                                                                        |                         | −                            | −                        | 0.4                          | V    | 11           |
| Watchdog output pull-up current      | I <sub>WUP</sub>   | V <sub>WDO</sub> = 0 V,<br>A / B / C / D / E / F type only               |                         | −                            | −0.85                    | −0.4                         | μA   | 12           |
| Watchdog output current              | I <sub>WOUT</sub>  | V <sub>DS</sub> = 0.4 V                                                  | V <sub>DD</sub> = 1.5 V | 0.6                          | 1.1                      | −                            | mA   | 13           |
|                                      |                    |                                                                          | V <sub>DD</sub> = 1.8 V | 1.1                          | 1.6                      | −                            | mA   | 13           |
|                                      |                    |                                                                          | V <sub>DD</sub> = 2.5 V | 2.1                          | 2.6                      | −                            | mA   | 13           |
|                                      |                    |                                                                          | V <sub>DD</sub> = 3.0 V | 2.8                          | 3.3                      | −                            | mA   | 13           |
| Watchdog output leakage current      | I <sub>WLEAK</sub> | V <sub>DS</sub> = 6.0 V, V <sub>DD</sub> = 6.0 V                         |                         | −                            | −                        | 0.096                        | μA   | 14           |
| Input pin voltage 1 "H"              | V <sub>SH1</sub>   | WEN pin                                                                  |                         | 0.7 × V <sub>DD</sub>        | −                        | −                            | V    | 15           |
| Input pin voltage 1 "L"              | V <sub>SL1</sub>   | WEN pin                                                                  |                         | −                            | −                        | 0.3 × V <sub>DD</sub>        | V    | 15           |
| Input pin voltage 2 "H"              | V <sub>SH2</sub>   | W̄ / T pin, S-1410 Series only                                           |                         | 0.7 × V <sub>DD</sub>        | −                        | −                            | V    | 15           |
| Input pin voltage 2 "L"              | V <sub>SL2</sub>   | W̄ / T pin, S-1410 Series only                                           |                         | −                            | −                        | 0.3 × V <sub>DD</sub>        | V    | 15           |
| Input pin voltage 3 "H"              | V <sub>SH3</sub>   | WDI pin                                                                  |                         | 0.7 × V <sub>DD</sub>        | −                        | −                            | V    | 15           |
| Input pin voltage 3 "L"              | V <sub>SL3</sub>   | WDI pin                                                                  |                         | −                            | −                        | 0.3 × V <sub>DD</sub>        | V    | 15           |

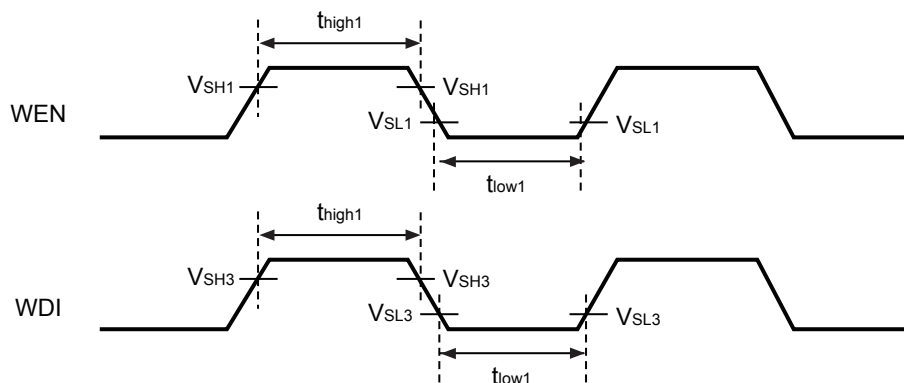
**Table 9 (2 / 2)**

(WEN pin logic active "H" product,  $V_{DD} = 5.0\text{ V}$ ,  $T_a = +25^\circ\text{C}$  unless otherwise specified)

| Item                                | Symbol             | Condition                                                                            |                                  | Min. | Typ. | Max. | Unit | Test Circuit |
|-------------------------------------|--------------------|--------------------------------------------------------------------------------------|----------------------------------|------|------|------|------|--------------|
| Input pin current 1 "H"             | I <sub>SH1</sub>   | WEN pin,<br>V <sub>DD</sub> = 6.0 V,<br>Input pin voltage = 6.0 V                    | A / B / C /<br>G / H / I<br>type | –    | 0.3  | 1.0  | μA   | 15           |
|                                     |                    |                                                                                      | D / E / F /<br>J / K / L<br>type | –0.1 | –    | 0.1  | μA   | 15           |
| Input pin current 1 "L"             | I <sub>SL1</sub>   | WEN pin, V <sub>DD</sub> = 6.0 V,<br>Input pin voltage = 0 V                         |                                  | –0.1 | –    | 0.1  | μA   | 15           |
| Input pin current 2 "H"             | I <sub>SH2</sub>   | W / T pin, S-1410 Series only,<br>V <sub>DD</sub> = 6.0 V, Input pin voltage = 6.0 V |                                  | –    | 0.3  | 1.0  | μA   | 15           |
| Input pin current 2 "L"             | I <sub>SL2</sub>   | W / T pin, S-1410 Series only,<br>V <sub>DD</sub> = 6.0 V, Input pin voltage = 0 V   |                                  | –0.1 | –    | 0.1  | μA   | 15           |
| Input pin current 3 "H"             | I <sub>SH3</sub>   | WDI pin, V <sub>DD</sub> = 6.0 V,<br>Input pin voltage = 6.0 V                       |                                  | –    | 0.3  | 1.0  | μA   | 15           |
| Input pin current 3 "L"             | I <sub>SL3</sub>   | WDI pin, V <sub>DD</sub> = 6.0 V,<br>Input pin voltage = 0 V                         |                                  | –0.1 | –    | 0.1  | μA   | 15           |
| Input pulse width "H" <sup>*2</sup> | t <sub>high1</sub> | –                                                                                    |                                  | 1.5  | –    | –    | μs   | 15           |
| Input pulse width "L" <sup>*2</sup> | t <sub>low1</sub>  | –                                                                                    |                                  | 1.5  | –    | –    | μs   | 15           |
| Watchdog output delay time          | t <sub>WOUT</sub>  | –                                                                                    |                                  | –    | 25   | 40   | μs   | 3            |
| Reset output delay time             | t <sub>ROUT</sub>  | –                                                                                    |                                  | –    | 25   | 40   | μs   | 3            |
| Input setup time                    | t <sub>iset</sub>  | –                                                                                    |                                  | 1.0  | –    | –    | μs   | 3            |

\*1.  $-V_{DET}$ : Actual detection voltage,  $-V_{DET(S)}$ : Set detection voltage

\*2. The input pulse width "H" ( $t_{high1}$ ) and the input pulse width "L" ( $t_{low1}$ ) are defined as shown in **Figure 7**.  
Inputs to the WEN pin and the WDI pin should be greater than or equal to the min. value specified in "■ Electrical Characteristics".



**Figure 7**

## ■ Test Circuits

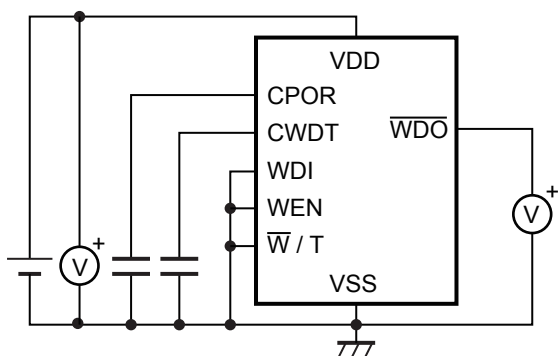


Figure 8 Test Circuit 1

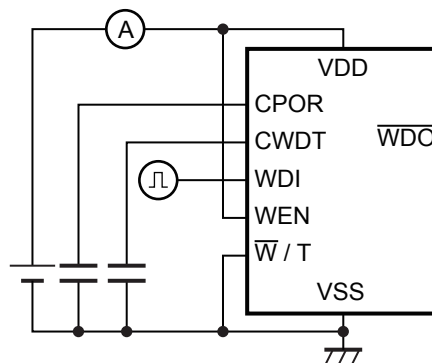


Figure 9 Test Circuit 2

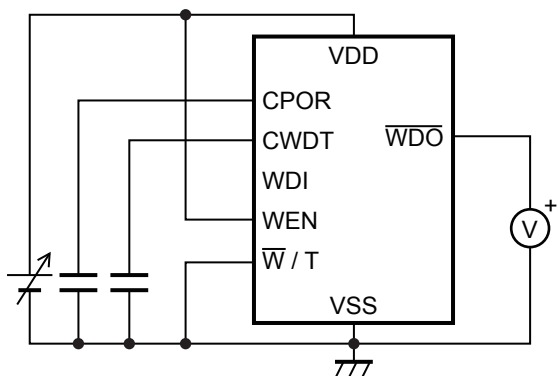


Figure 10 Test Circuit 3

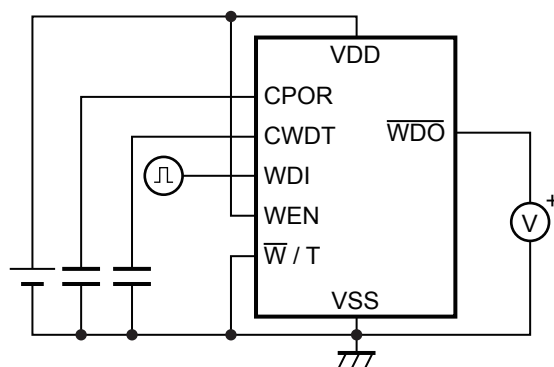


Figure 11 Test Circuit 4

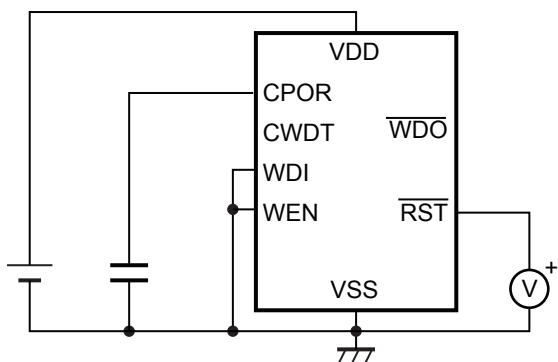


Figure 12 Test Circuit 5

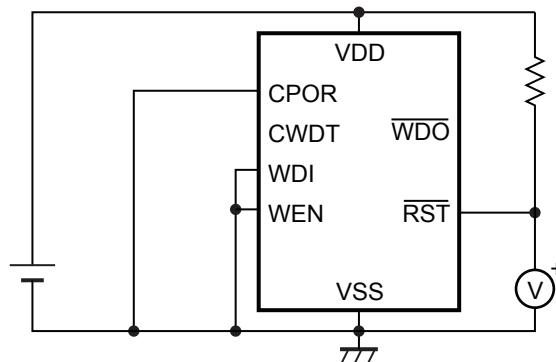


Figure 13 Test Circuit 6

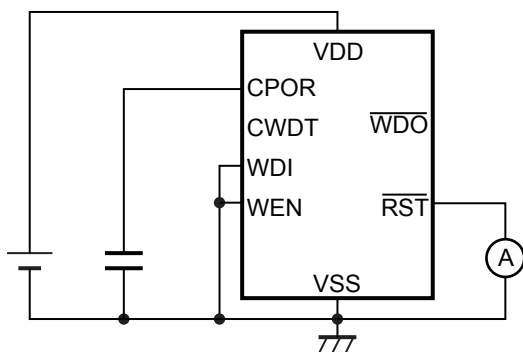


Figure 14 Test Circuit 7

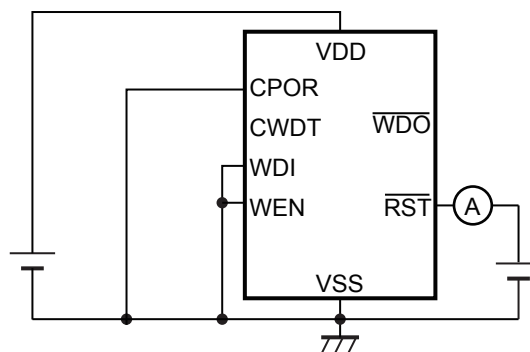


Figure 15 Test Circuit 8

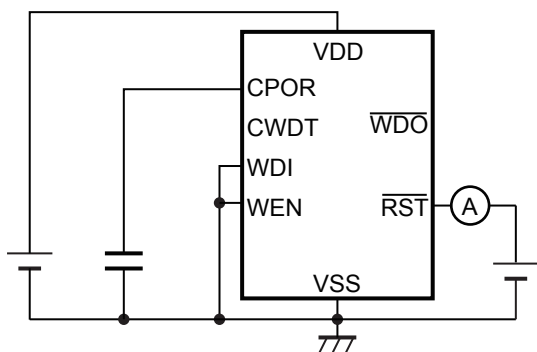


Figure 16 Test Circuit 9

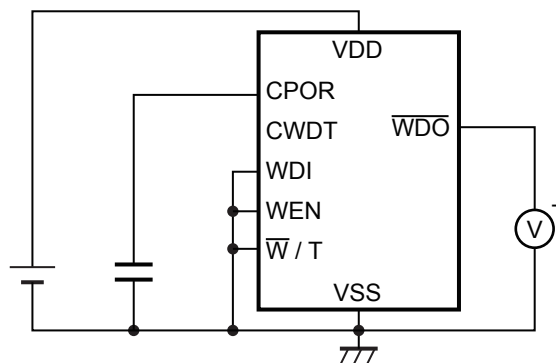


Figure 17 Test Circuit 10

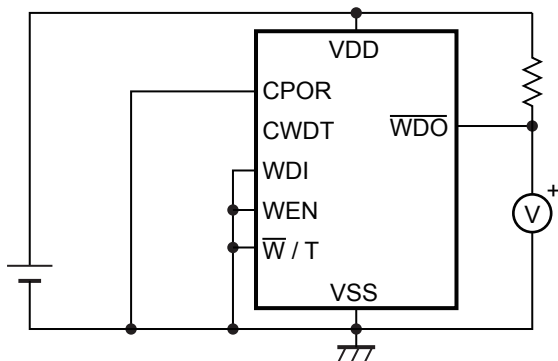


Figure 18 Test Circuit 11

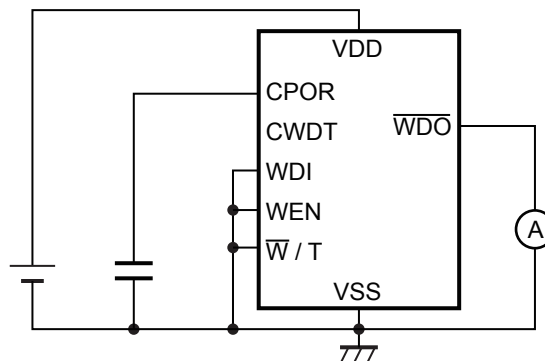


Figure 19 Test Circuit 12

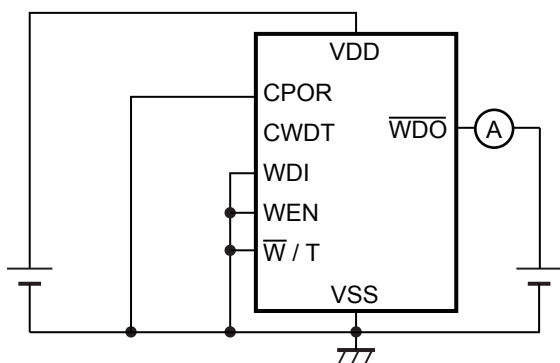


Figure 20 Test Circuit 13

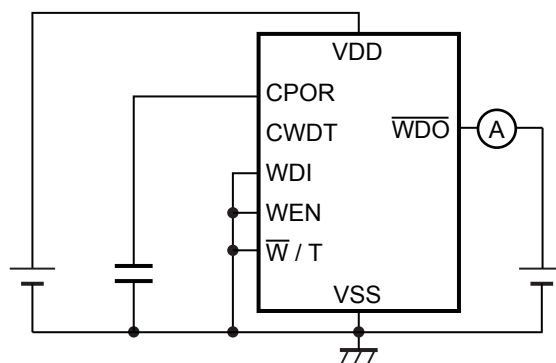


Figure 21 Test Circuit 14

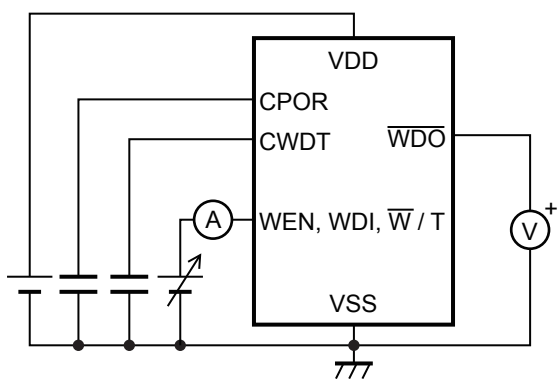
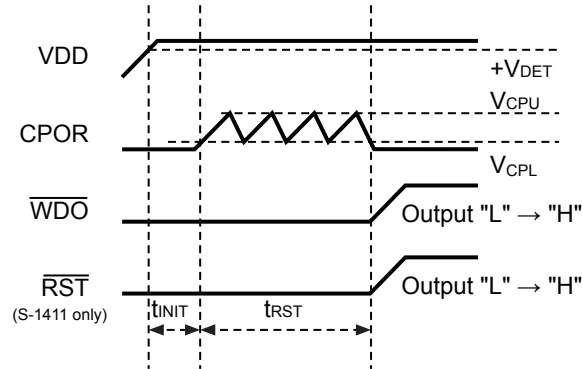


Figure 22 Test Circuit 15

## ■ Operation

### 1. From power-on to reset release

The S-1410/1411 Series initiates the initialization if the VDD pin voltage exceeds the release voltage ( $+V_{DET}$ ). The charge-discharge operation to the CPOR pin is initiated after the passage of the initialization time ( $t_{INIT}$ ), and the  $\overline{WDO}$  pin output and the  $\overline{RST}$  pin output change from "L" to "H" after the operation is performed 4 times.



**Remark** V<sub>CPU</sub>: CPOR charge upper limit threshold (1.25 V typ.)  
V<sub>CPL</sub>: CPOR charge lower limit threshold (0.20 V typ.)

Figure 23

$t_{INIT}$  changes according to the power supply rising time. Refer to **Figure 24** for the relation between  $t_{INIT}$  and the power supply rising time.

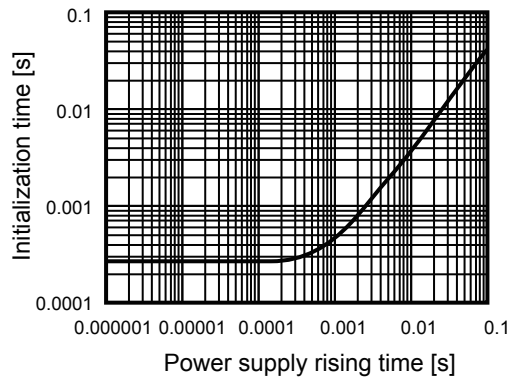
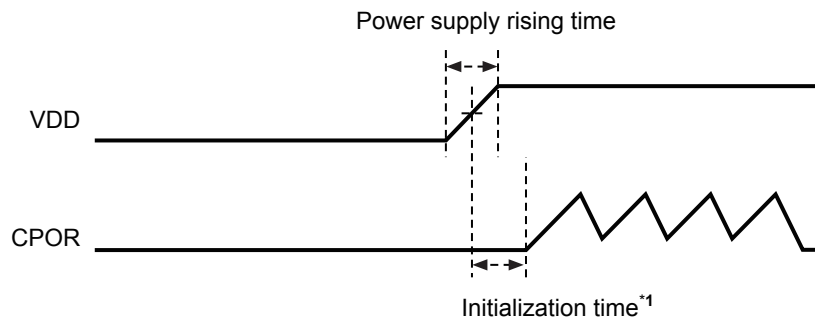


Figure 24 Power Supply Rising Time Dependency of Initialization Time



\*1. The initialization time is the time period from when the VDD pin voltage reaches  $V_{DD} / 2$  to when C<sub>POR</sub> rises.

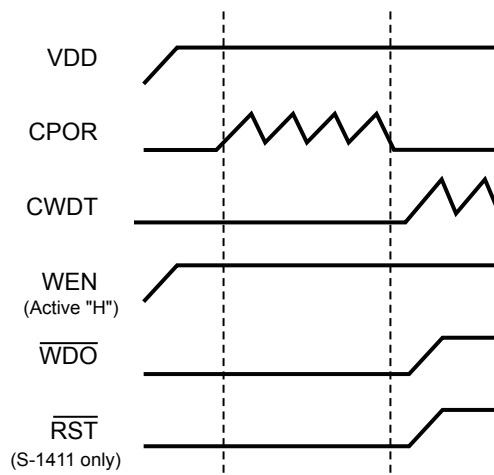
Figure 25 Initialization Time

## 2. From reset release to initiation of charge-discharge operation to CWDT pin

The charge-discharge operation to the CWDT pin differs depending on the status of the WEN pin at the reset release.

### 2.1 When WEN pin is "H" at reset release (Active "H")

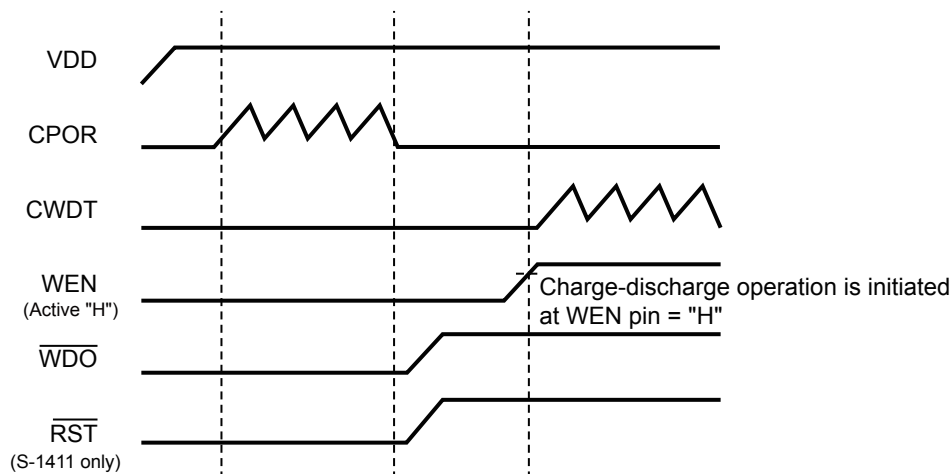
Since the watchdog timer is Enable, the S-1410/1411 Series initiates the charge-discharge operation to the CWDT pin.



**Figure 26 WEN Pin = "H"**

### 2.2 When WEN pin is "L" at reset release (Active "H")

Since the watchdog timer is Disable after the CPOR pin performs the charge-discharge operation 4 times, the S-1410/1411 Series does not initiate the charge-discharge operation to the CWDT pin. If the input to the WEN pin changes to "H" in this status, the S-1410/1411 Series initiates the charge-discharge operation to the CWDT pin.



**Figure 27 WEN Pin = "L" → "H"**



### 3. Watchdog time-out detection

The watchdog timer detects a time-out after the charge-discharge operation to the CWDT pin is performed 32 times, then the  $\overline{\text{WDO}}$  pin output changes from "H" to "L".

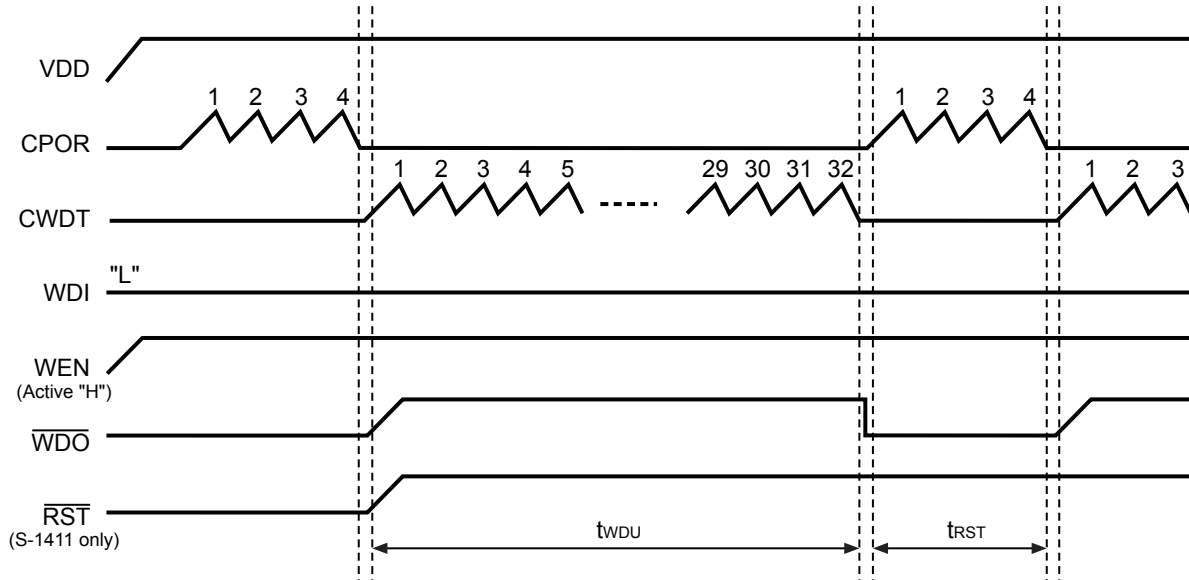


Figure 28

### 4. Internal counter reset due to edge detection

When the WDI pin detects an edge during the charge-discharge operation to the CWDT pin, the internal counter which counts the number of times of the charge-discharge operation is reset. The CWDT pin initiates the discharge operation when an edge is detected, and initiates the charge-discharge operation again after the discharge operation is completed.

#### 4.1 Counter reset due to rising edge detection (S-141xAxx, S-141xDxx, S-141xGxx, S-141xJxx)

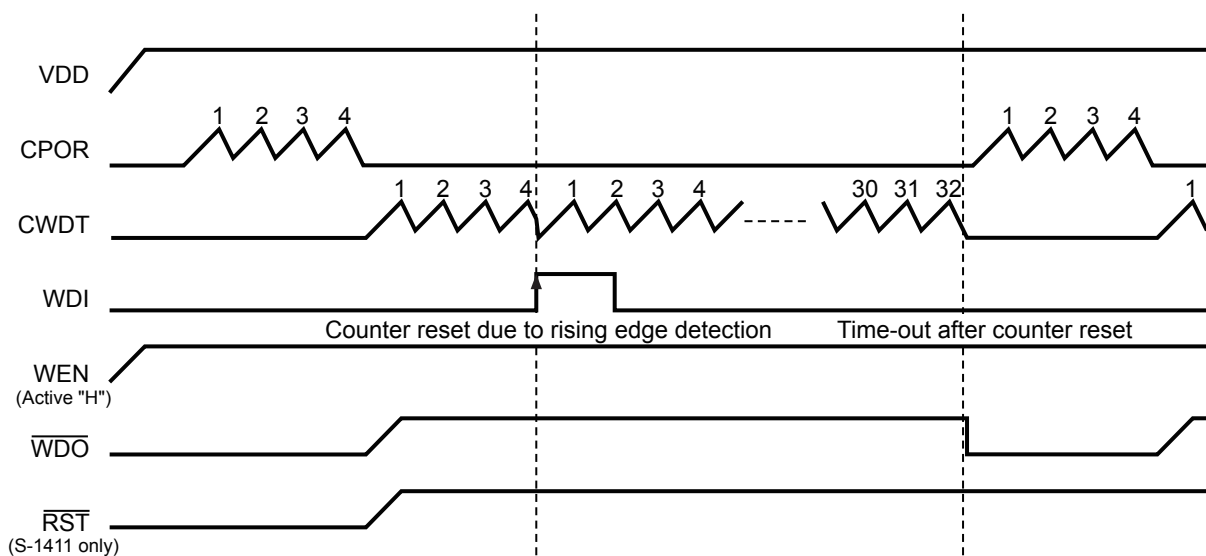


Figure 29

**4.2 Counter reset due to falling edge detection**  
**(S-141xBxx, S-141xExx, S-141xHxx, S-141xKxx)**

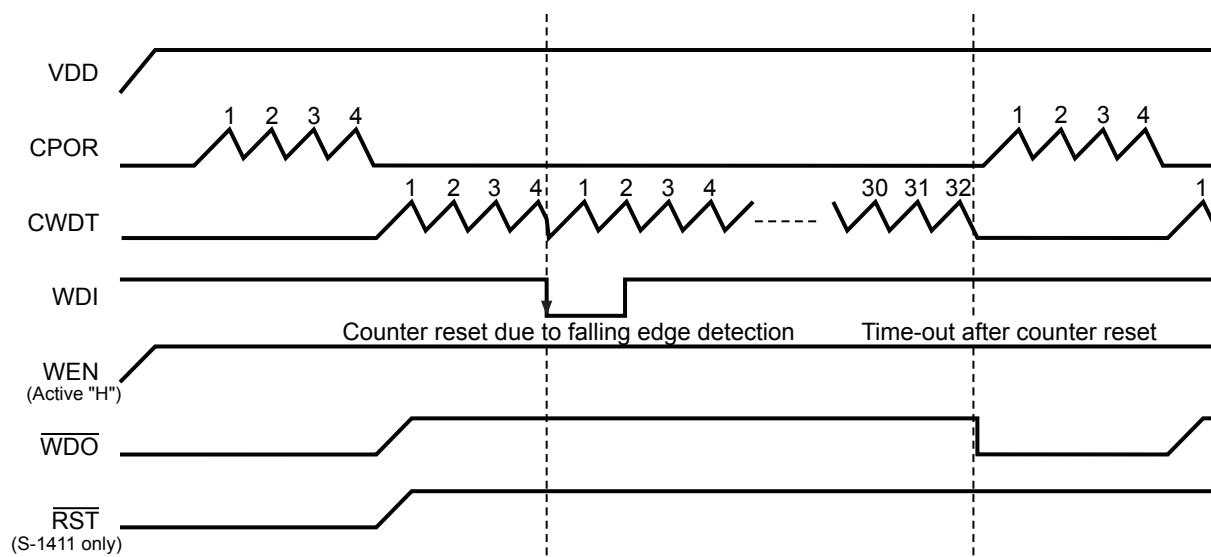


Figure 30

**4.3 Counter reset due to both rising and falling edges detection 1**  
**(S-141xCxx, S-141xFxx, S-141xLxx, S-141xLxx)**

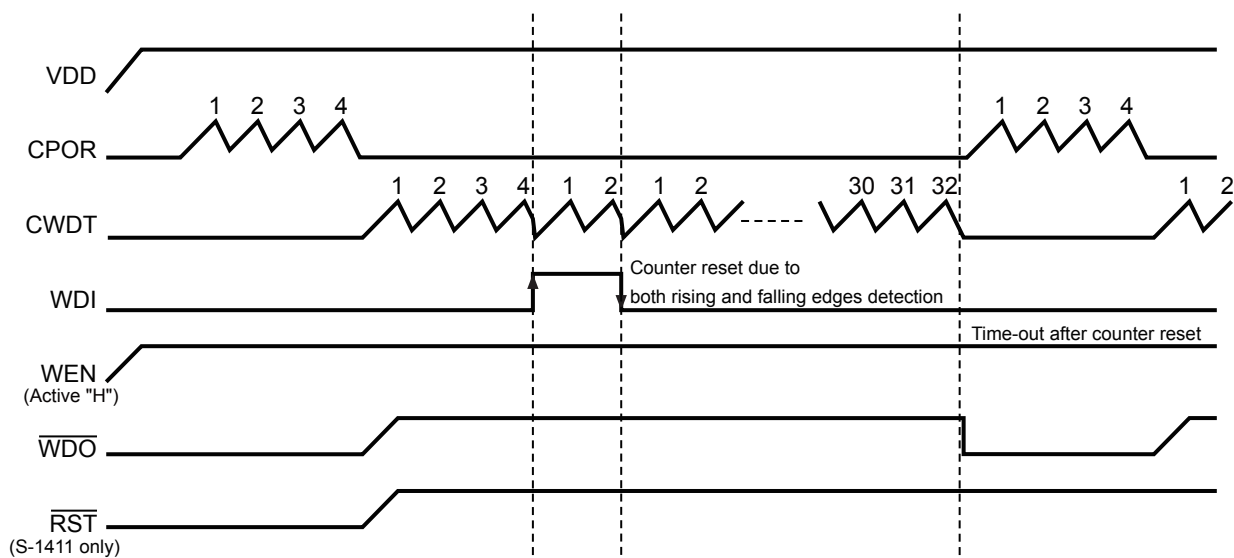


Figure 31

**4. 4 Counter reset due to both rising and falling edges detection 2**  
(S-141xCxx, S-141xFxx, S-141xLxx, S-141xLxx)

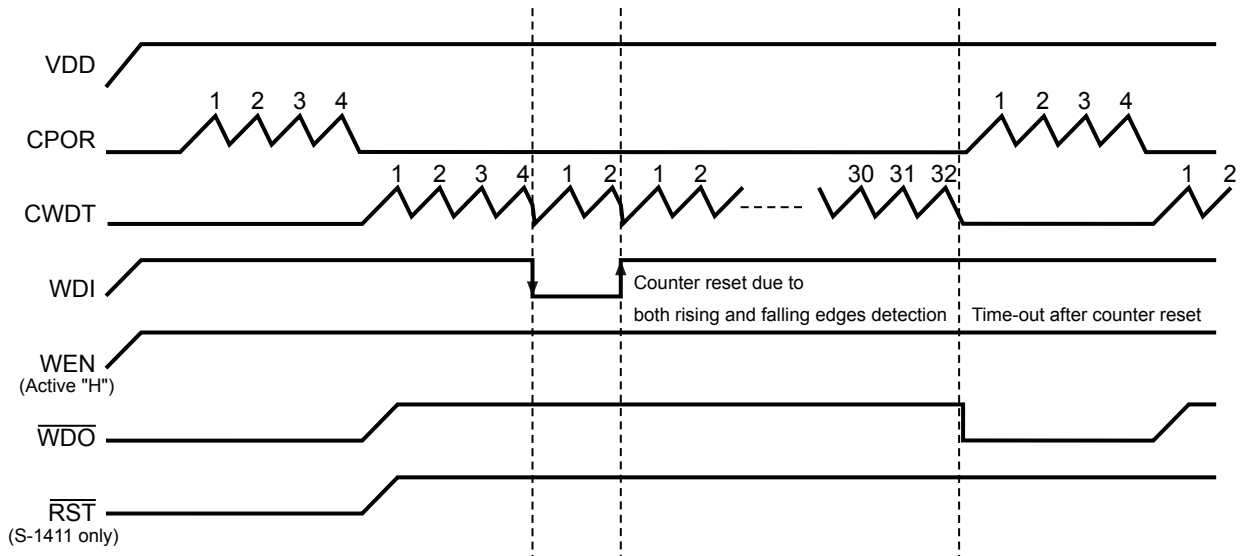


Figure 32

**5. WEN pin operation during charge-discharge operation to CWDT pin**

When the WEN pin changes from "H" to "L" during the charge-discharge operation to the CWDT pin, the CWDT pin performs the discharge operation. Moreover, the internal counter which counts the number of times of the charge-discharge operation for the CWDT pin is also reset.

If the WEN pin changes to "H" again in this status, the CWDT pin initiates the charge-discharge operation.

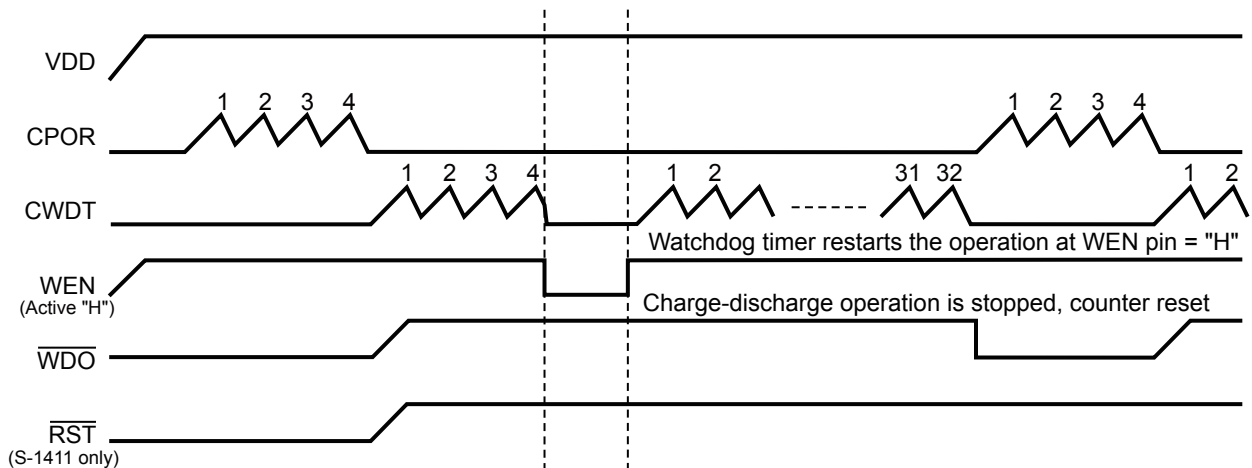


Figure 33

## 6. Watchdog double pulse detection

If an edge is input to the WDI pin again within a specific period of time (the discharge time due to an edge detection + 1 charge-discharge time ( $t_{WDL}$ )) after inputting an edge to the WDI pin when the S-1410/1411 Series is the window mode, the  $\overline{WDO}$  pin output changes from "H" to "L".

When the watchdog timer becomes Disable due to a change of the WEN pin ("H" → "L" → "H") after inputting an edge to the WDI pin, the  $\overline{WDO}$  pin continues outputting "H" even if an edge is input to the WDI pin within the specific period of time mentioned above.

### 6.1 Double pulse detection due to rising edge detection (S-141xAxx, S-141xDxx, S-141xGxx, S-141xJxx)

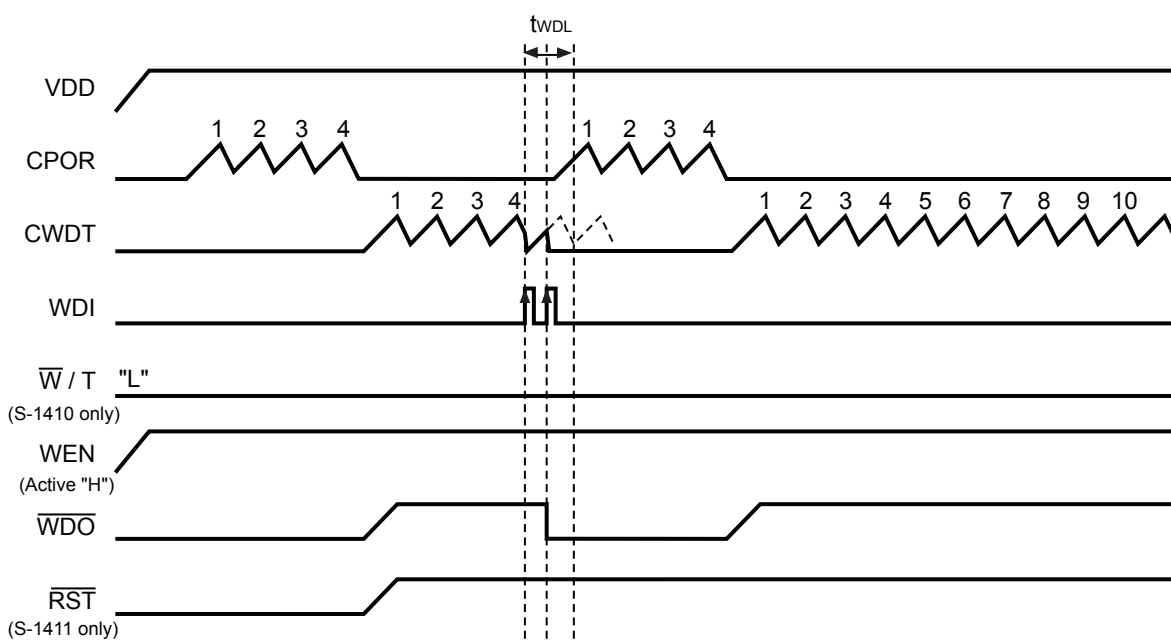


Figure 34

### 6.2 Double pulse detection due to falling edge detection (S-141xBxx, S-141xExx, S-141xHxx, S-141xKxx)

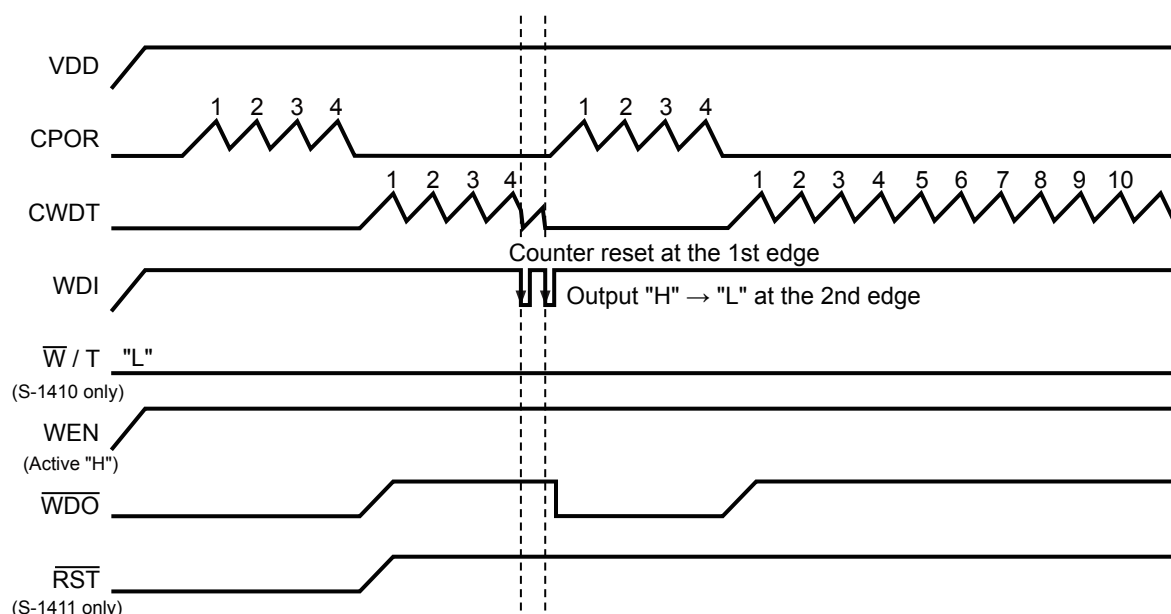


Figure 35

### 6.3 Double pulse detection due to both rising and falling edges detection (S-141xCxx, S-141xFxx, S-141xLxx, S-141xLxx)

The double pulse is detected only when edges are input in order of rising and falling.

#### 6.3.1 When edges are input to WDI pin in order of rising and falling

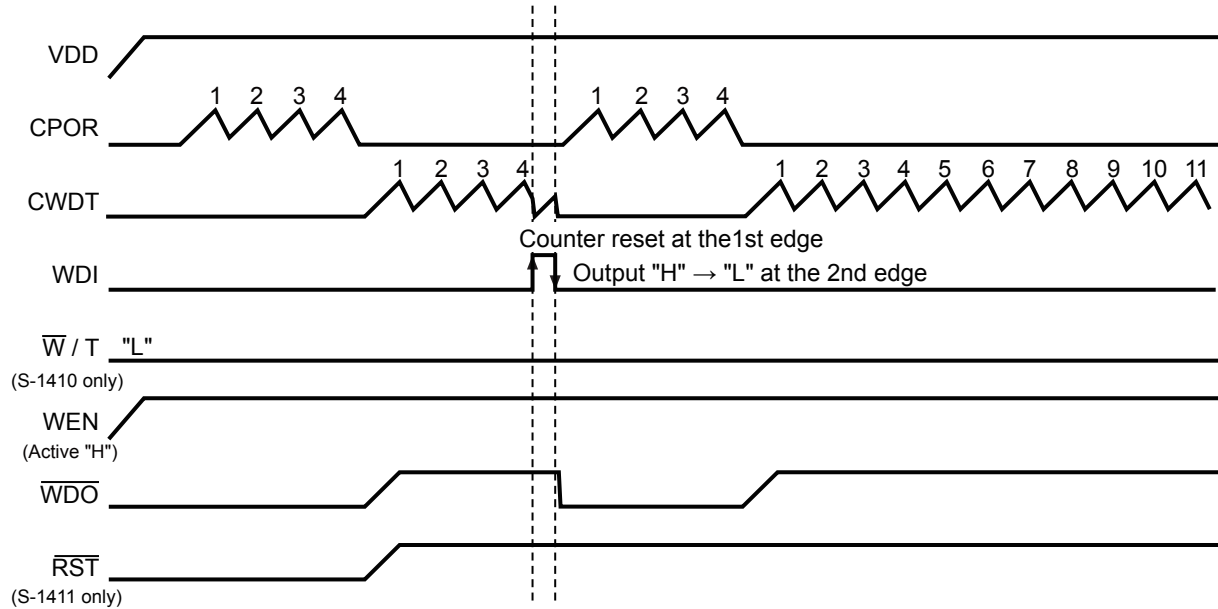


Figure 36 Double Pulse Detection

#### 6.3.2 When edges are input to WDI pin in order of falling and rising

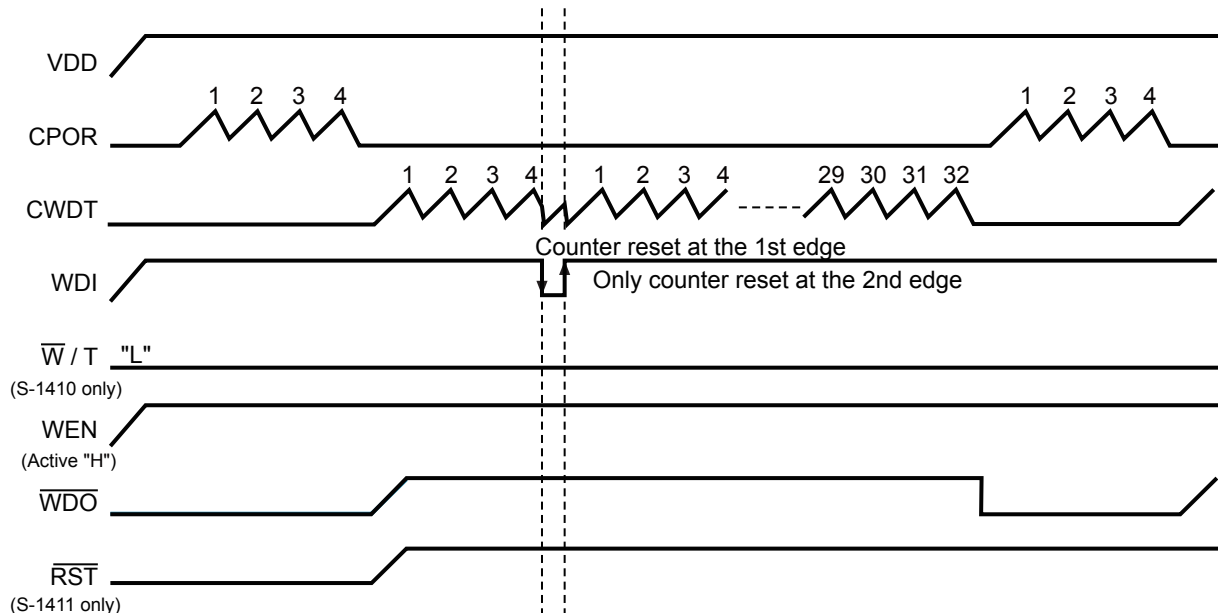
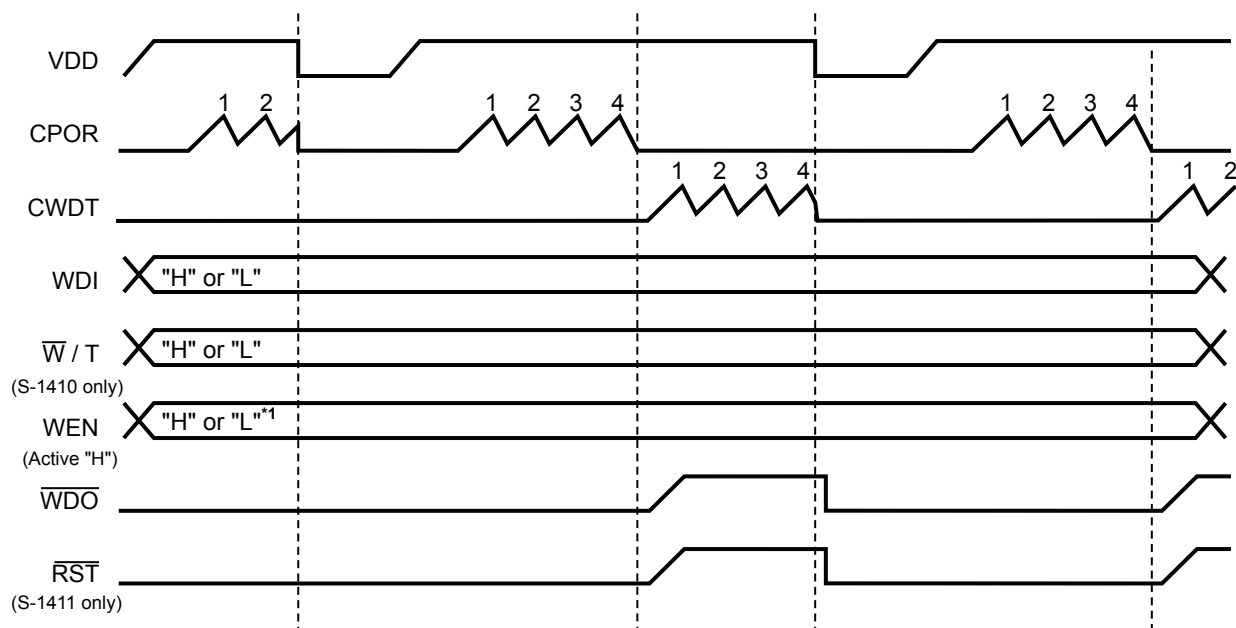


Figure 37 Double Pulse Non-detection

## 7. Operation of low voltage detection

The voltage detection circuit detects a low voltage if the power supply voltage falls below the detection voltage, and then "L" is output from the  $\overline{\text{WDO}}$  pin and the  $\overline{\text{RST}}$  pin (Only the S-1411 Series). The output is maintained until the charge-discharge operation of the CPOR pin is performed 4 times.

The S-1410/1411 Series can detect a low voltage even if either the CPOR pin or the WDT pin performs the charge-discharge operation. In this case, the status of the WEN pin or the  $\overline{\text{W}} / \text{T}$  pin does not have an affect.



**Figure 38**

\*1. When the WEN pin is Disable, the charge-discharge operation of CWDT pin is not performed.

## 8. WEN pin, WDI pin and $\overline{\text{W}} / \text{T}$ pin

Each of the WEN pin, the WDI pin and the  $\overline{\text{W}} / \text{T}$  pin has a noise filter.

If the power supply voltage is 5.0 V, noise with a minimum pulse width of 200 ns can be eliminated.

## ■ Standard Circuits

### 1. S-1410 Series (Product with $\overline{W}$ / T pin)

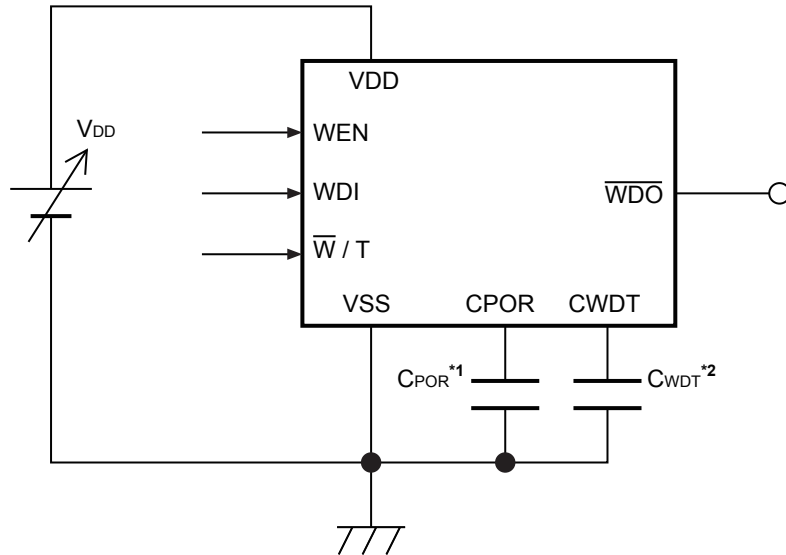


Figure 39

### 2. S-1411 Series (Product without $\overline{W}$ / T pin)

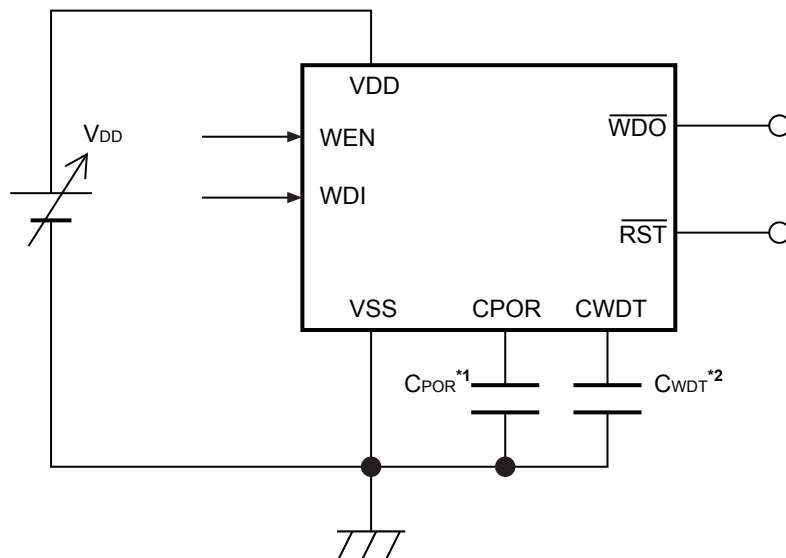


Figure 40

- \*1. Adjustment capacitor for reset output delay time ( $C_{POR}$ ) should be connected directly to the CPOR pin and the VSS pin.
  - \*2. Adjustment capacitor for watchdog output delay time ( $C_{WDT}$ ) should be connected directly to the CWDT pin and the VSS pin.
- A capacitor of 100 pF to 1  $\mu$ F can be used for  $C_{POR}$  and  $C_{WDT}$ .

**Caution** The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

## ■ Precautions

- It will take time for the discharge operation to be performed if the capacitance of  $C_{POR}$  is extremely large at the low voltage detection, so the discharge operation may not be completed by the time the power supply voltage exceeds the detection voltage. In that case, since the charge-discharge operation of the CPOR pin is performed after the discharge operation is completed, the delay time of the same time length as the discharge operation occurs in reset time-out period ( $t_{RST}$ ).
- Select a capacitor which satisfies the following equation for  $C_{POR}$  and  $C_{WDT}$ . If this condition is not satisfied, the delay time of the same time length as the discharge operation occurs in  $t_{RST}$  since the discharge operation of an external capacitor connected to the CWDT pin is not completed by the time the CWDT pin initiates the next charge-discharge operation.

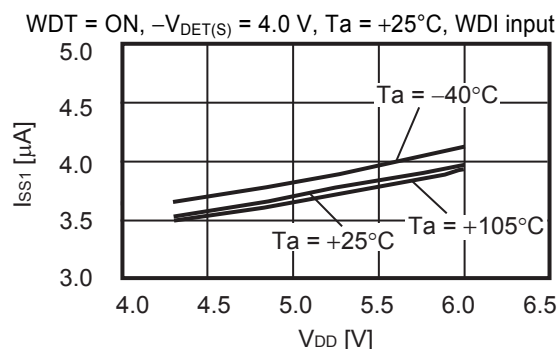
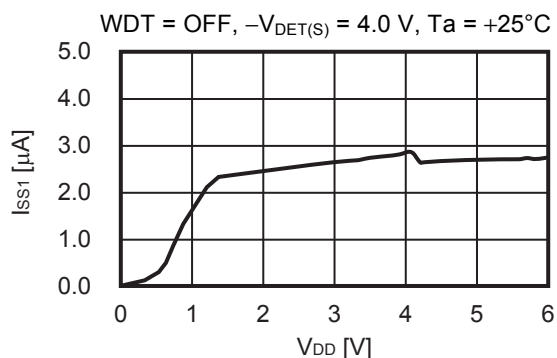
$$C_{WDT} / C_{POR} \leq 600$$

- When the power supply voltage falls to 0.9 V or lower, set a time interval of 20  $\mu$ s or longer by the time the power supply is raised again. If the appropriate time length is not secured, the time-out period after raising the power supply voltage may get delayed.
- When the time that the power supply voltage falls below the detection voltage is short, the S-1410/1411 Series may not detect a voltage. In that case, the time-out period after raising the power supply voltage may get delayed.
- Since input pins (the WEN pin, the WDI pin and the  $\overline{W}$  / T pin) in the S-1410/1411 Series are CMOS configurations, make sure that an intermediate potential is not input when the S-1410/1411 Series operates.
- Since the  $\overline{WDO}$  pin and the  $\overline{RST}$  pin are affected by external resistance and external capacitance, use the S-1410/1411 Series after performing thorough evaluation with the actual application.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII Semiconductor Corporation claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

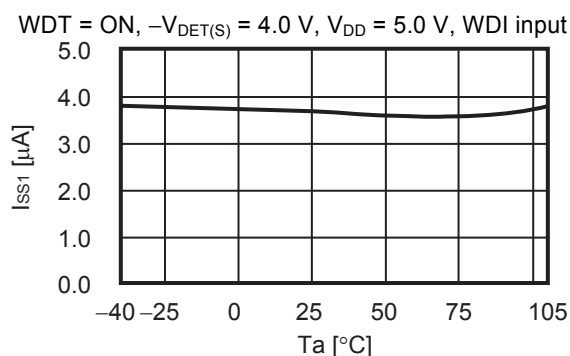


## ■ Characteristics (Typical Data)

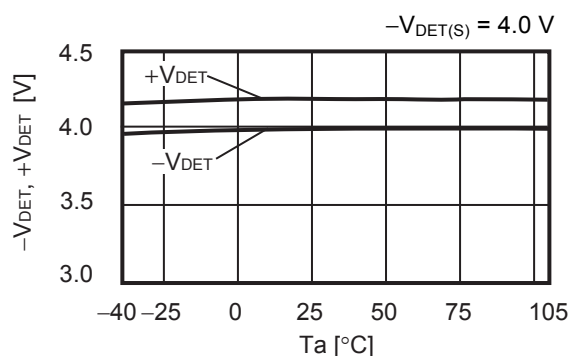
### 1. Current consumption during operation ( $I_{SS1}$ ) vs. Input voltage ( $V_{DD}$ )



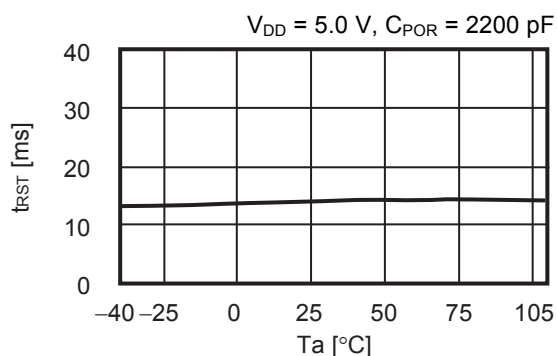
### 2. Current consumption during operation ( $I_{SS1}$ ) vs. Temperature ( $T_a$ )



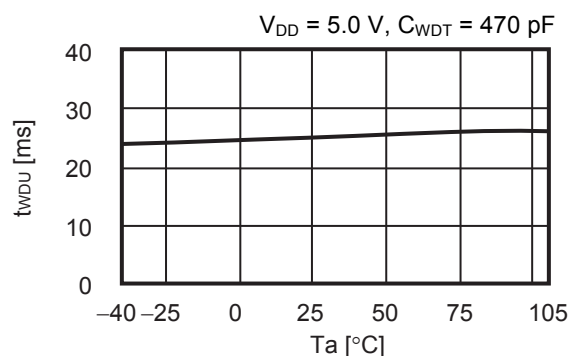
### 3. Detection voltage ( $-V_{DET}$ ), Release voltage ( $+V_{DET}$ ) vs. Temperature ( $T_a$ )



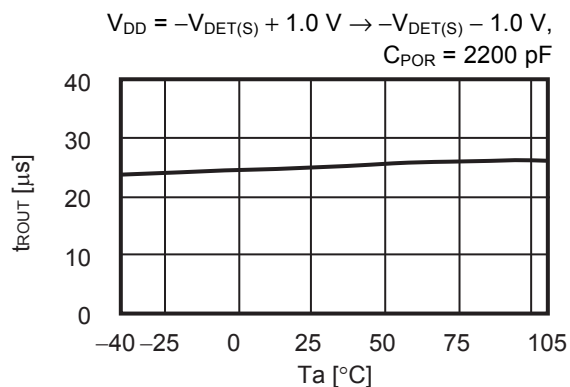
### 4. Reset time-out period ( $t_{RST}$ ) vs. Temperature ( $T_a$ )



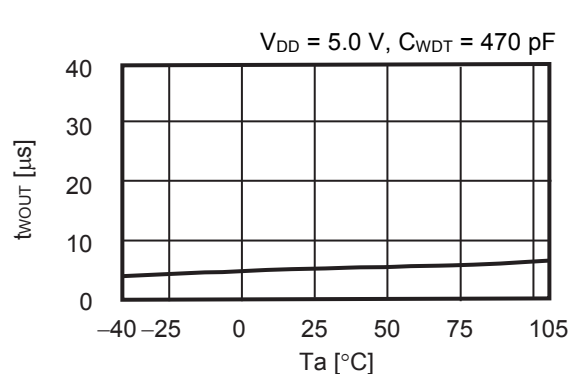
### 5. Watchdog time-out period ( $t_{WDU}$ ) vs. Temperature ( $T_a$ )



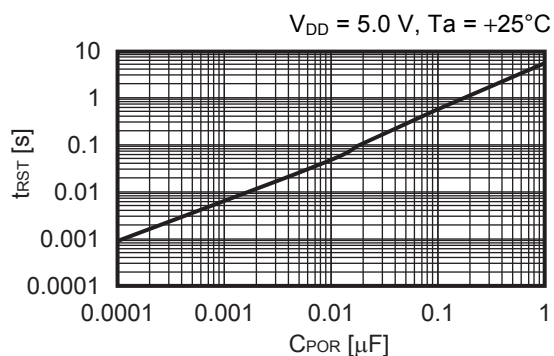
### 6. Reset output delay time ( $t_{ROUT}$ ) vs. Temperature ( $T_a$ )



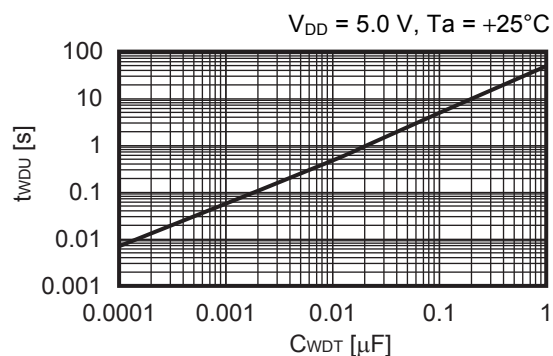
### 7. Watchdog output delay time ( $t_{WOUT}$ ) vs. Temperature ( $T_a$ )



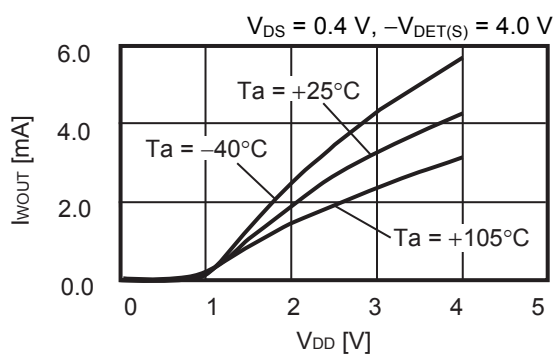
**8. Reset time-out period ( $t_{RST}$ ) vs.  $C_{POR}$**



**9. Watchdog time-out period ( $t_{WDT}$ ) vs.  $C_{WDT}$**



**10. Nch driver output current ( $I_{WOUT}$ ) vs. Input voltage ( $V_{DD}$ )**



## ■ Thermal Characteristics

### 1. TMSOP-8

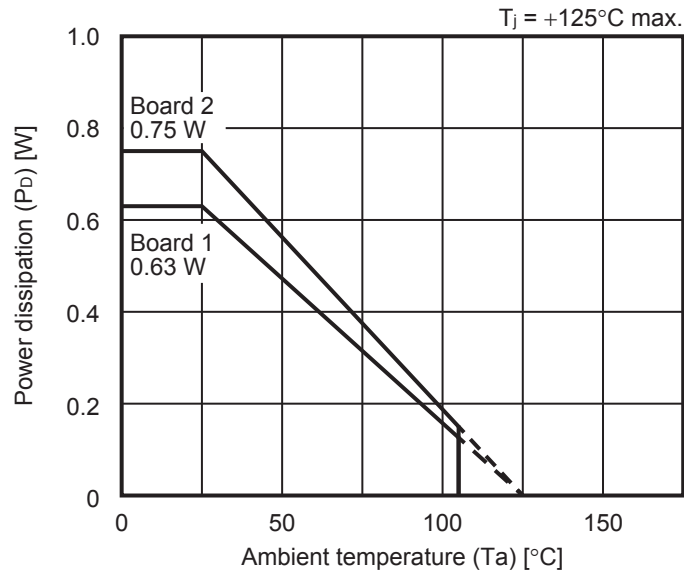


Figure 41 Power Dissipation of Package (When Mounted on Board)

#### 1.1 Board 1

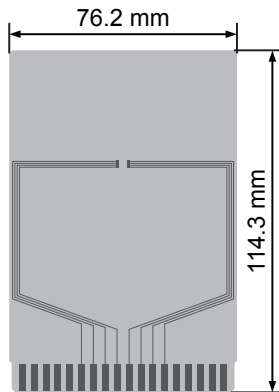


Figure 42

Table 10

| Item                                       |   | Specification                                  |
|--------------------------------------------|---|------------------------------------------------|
| Thermal resistance value ( $\theta_{ja}$ ) |   | 160°C/W                                        |
| Size                                       |   | 114.3 mm × 76.2 mm × t1.6 mm                   |
| Material                                   |   | FR-4                                           |
| Number of copper foil layer                |   | 2                                              |
| Copper foil layer                          | 1 | Land pattern and wiring for testing: t0.070 mm |
|                                            | 2 | —                                              |
|                                            | 3 | —                                              |
|                                            | 4 | 74.2 mm × 74.2 mm × t0.070 mm                  |
| Thermal via                                |   | —                                              |

#### 1.2 Board 2

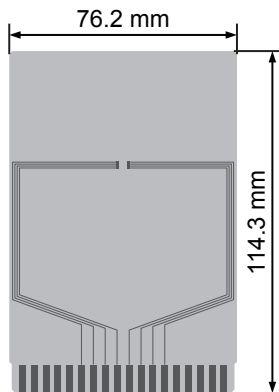


Figure 43

Table 11

| Item                                       |   | Specification                                  |
|--------------------------------------------|---|------------------------------------------------|
| Thermal resistance value ( $\theta_{ja}$ ) |   | 133°C/W                                        |
| Size                                       |   | 114.3 mm × 76.2 mm × t1.6 mm                   |
| Material                                   |   | FR-4                                           |
| Number of copper foil layer                |   | 4                                              |
| Copper foil layer                          | 1 | Land pattern and wiring for testing: t0.070 mm |
|                                            | 2 | 74.2 mm × 74.2 mm × t0.035 mm                  |
|                                            | 3 | 74.2 mm × 74.2 mm × t0.035 mm                  |
|                                            | 4 | 74.2 mm × 74.2 mm × t0.070 mm                  |
| Thermal via                                |   | —                                              |

## 2. HSNT-8(2030)

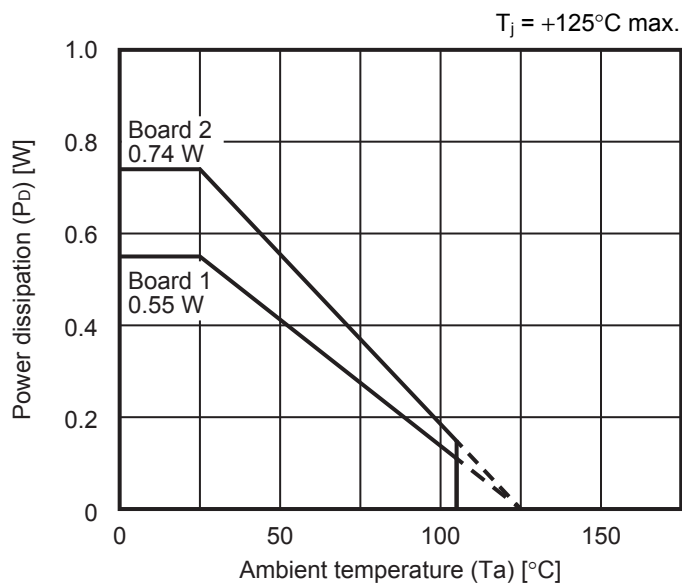


Figure 44 Power Dissipation of Package (When Mounted on Board)

### 2.1 Board 1

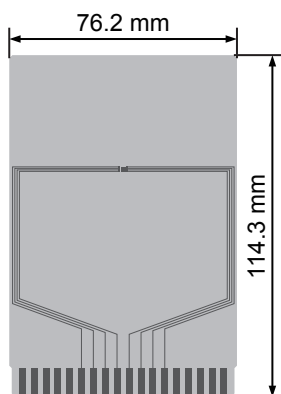


Figure 45

Table 12

| Item                                       |   | Specification                                  |
|--------------------------------------------|---|------------------------------------------------|
| Thermal resistance value ( $\theta_{ja}$ ) |   | 181°C/W                                        |
| Size                                       |   | 114.3 mm × 76.2 mm × t1.6 mm                   |
| Material                                   |   | FR-4                                           |
| Number of copper foil layer                |   | 2                                              |
| Copper foil layer                          | 1 | Land pattern and wiring for testing: t0.070 mm |
|                                            | 2 | —                                              |
|                                            | 3 | —                                              |
|                                            | 4 | 74.2 mm × 74.2 mm × t0.070 mm                  |
| Thermal via                                |   | —                                              |

### 2.2 Board 2

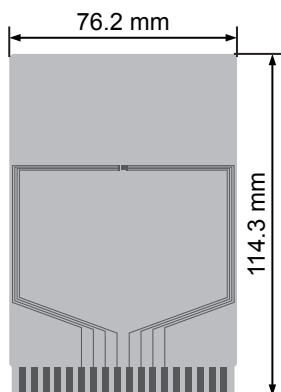
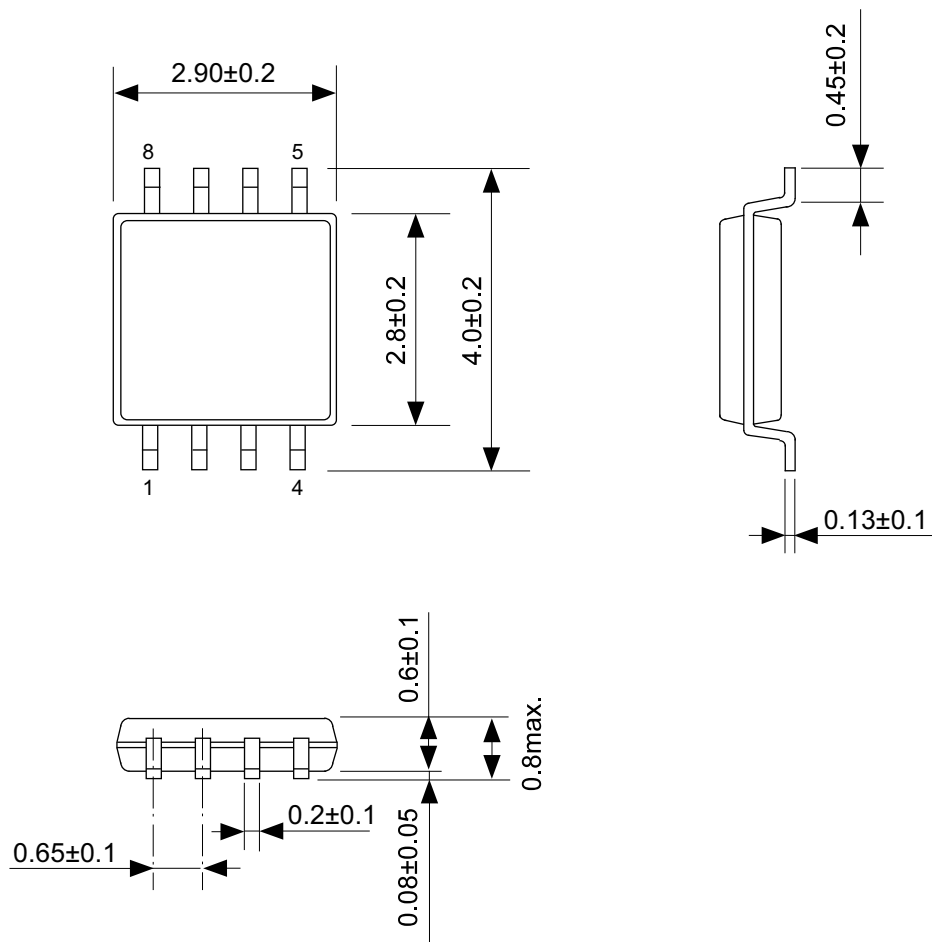


Figure 46

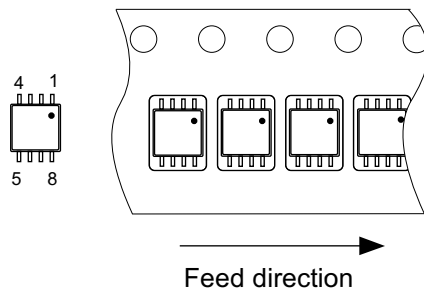
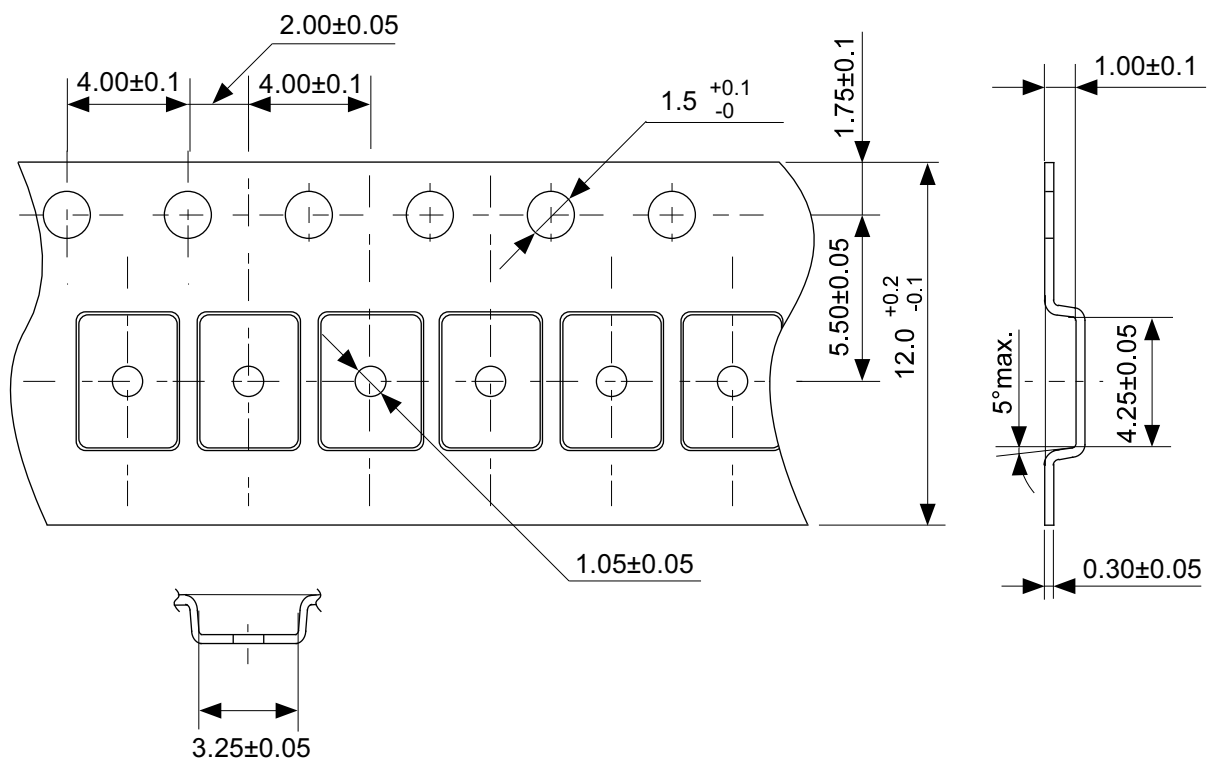
Table 13

| Item                                       |   | Specification                                  |
|--------------------------------------------|---|------------------------------------------------|
| Thermal resistance value ( $\theta_{ja}$ ) |   | 135°C/W                                        |
| Size                                       |   | 114.3 mm × 76.2 mm × t1.6 mm                   |
| Material                                   |   | FR-4                                           |
| Number of copper foil layer                |   | 4                                              |
| Copper foil layer                          | 1 | Land pattern and wiring for testing: t0.070 mm |
|                                            | 2 | 74.2 mm × 74.2 mm × t0.035 mm                  |
|                                            | 3 | 74.2 mm × 74.2 mm × t0.035 mm                  |
|                                            | 4 | 74.2 mm × 74.2 mm × t0.070 mm                  |
| Thermal via                                |   | —                                              |



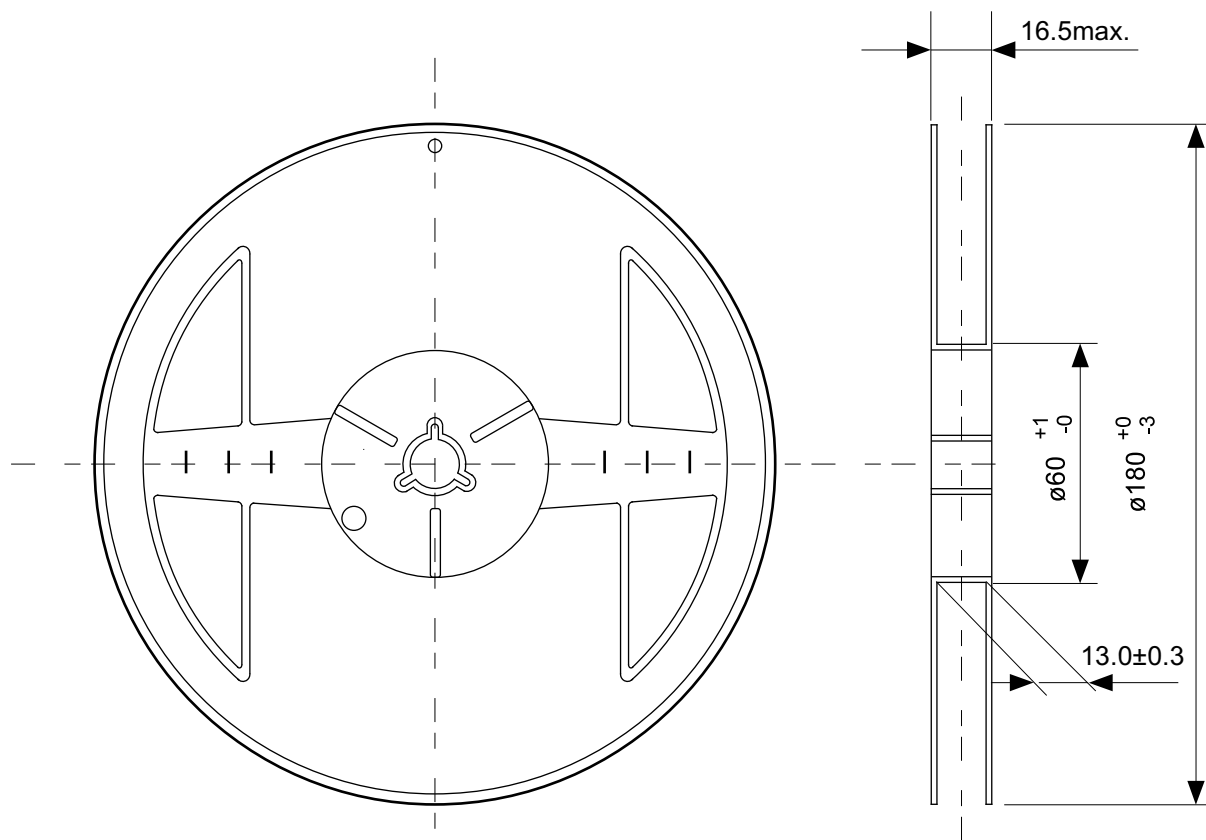
No. FM008-A-P-SD-1.2

|                               |                                                                                       |
|-------------------------------|---------------------------------------------------------------------------------------|
| TITLE                         | TMSOP8-A-PKG Dimensions                                                               |
| No.                           | FM008-A-P-SD-1.2                                                                      |
| ANGLE                         |  |
| UNIT                          | mm                                                                                    |
|                               |                                                                                       |
| SII Semiconductor Corporation |                                                                                       |

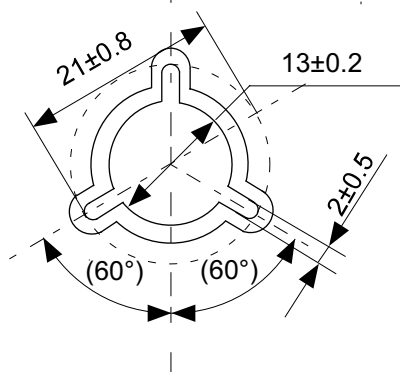


No. FM008-A-C-SD-2.0

|                               |                       |
|-------------------------------|-----------------------|
| TITLE                         | TMSOP8-A-Carrier Tape |
| No.                           | FM008-A-C-SD-2.0      |
| ANGLE                         |                       |
| UNIT                          | mm                    |
|                               |                       |
| SII Semiconductor Corporation |                       |

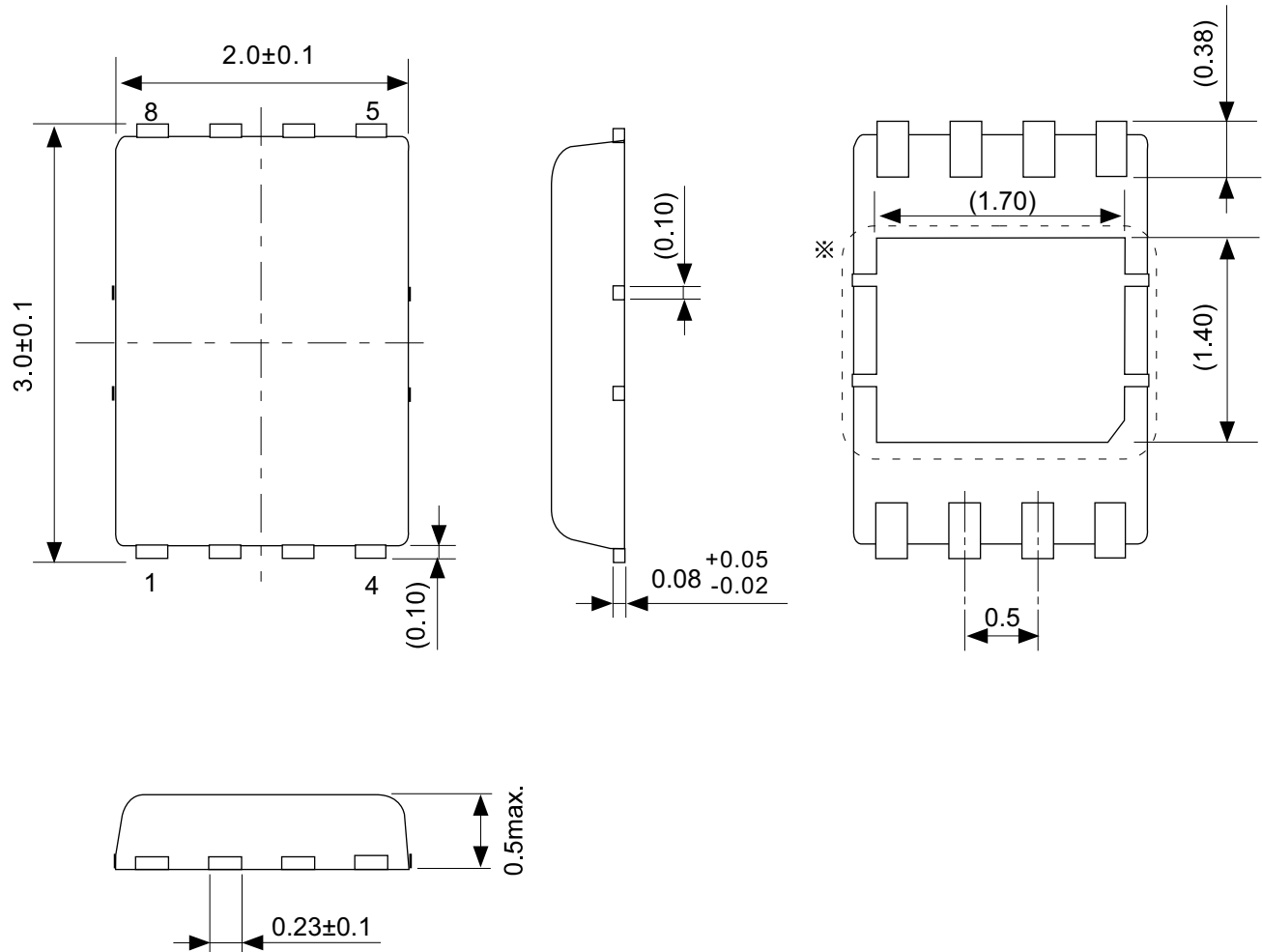


Enlarged drawing in the central part



No. FM008-A-R-SD-1.0

|                               |                  |      |       |
|-------------------------------|------------------|------|-------|
| TITLE                         | TMSOP8-A-Reel    |      |       |
| No.                           | FM008-A-R-SD-1.0 |      |       |
| ANGLE                         |                  | QTY. | 4,000 |
| UNIT                          | mm               |      |       |
|                               |                  |      |       |
| SII Semiconductor Corporation |                  |      |       |

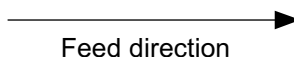
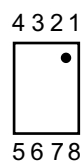
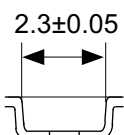


※ The heat sink of back side has different electric potential depending on the product.  
Confirm specifications of each product.  
Do not use it as the function of electrode.

No. PP008-A-P-SD-2.0

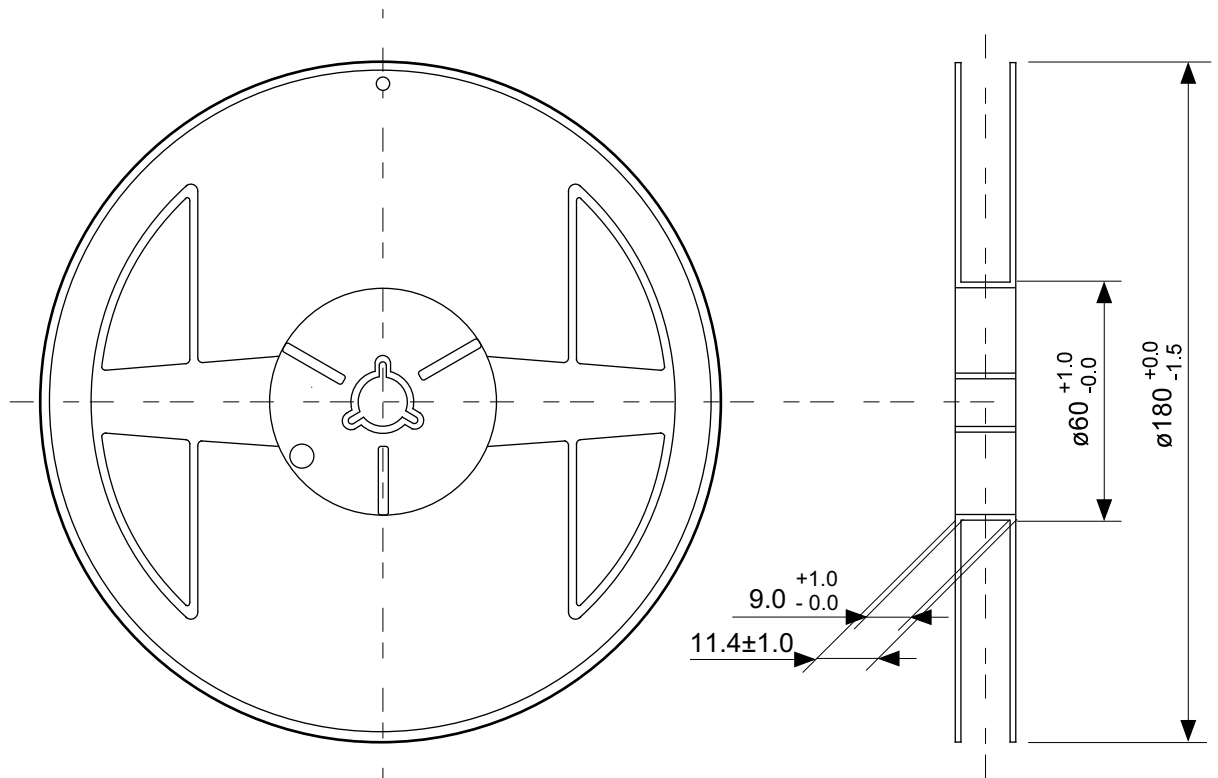
|                               |                                                                                       |
|-------------------------------|---------------------------------------------------------------------------------------|
| TITLE                         | DFN-8/HSNT-8-A-PKG Dimensions                                                         |
| No.                           | PP008-A-P-SD-2.0                                                                      |
| ANGLE                         |  |
| UNIT                          | mm                                                                                    |
|                               |                                                                                       |
| SII Semiconductor Corporation |                                                                                       |



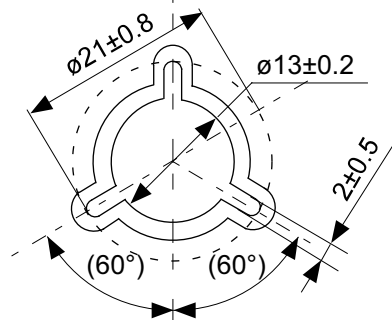


No. PP008-A-C-SD-1.0

|                               |                             |
|-------------------------------|-----------------------------|
| TITLE                         | DFN-8/HSNT-8-A-Carrier Tape |
| No.                           | PP008-A-C-SD-1.0            |
| ANGLE                         |                             |
| UNIT                          | mm                          |
|                               |                             |
| SII Semiconductor Corporation |                             |

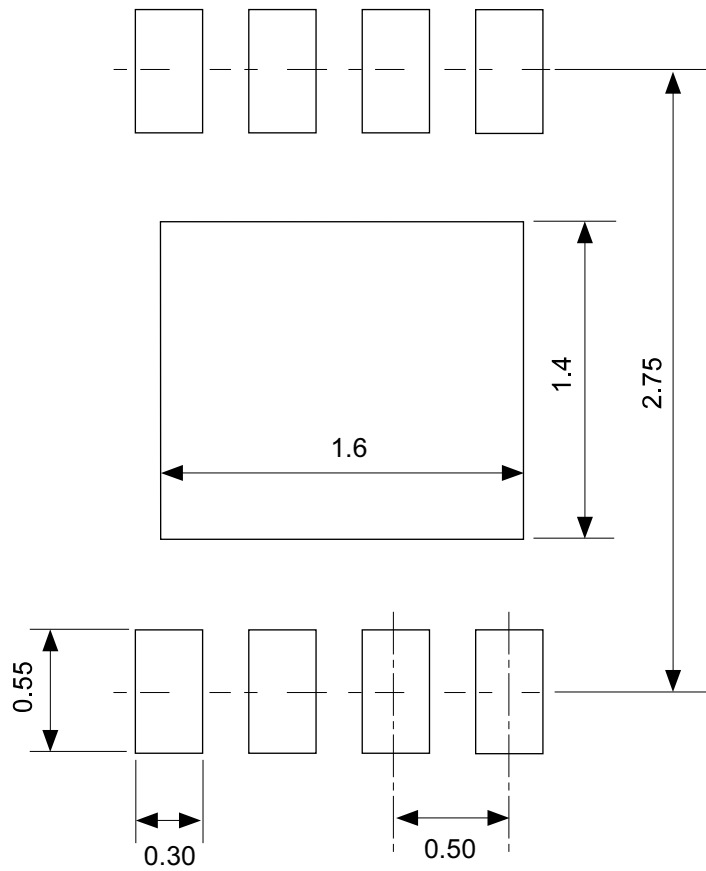


Enlarged drawing in the central part



No. PP008-A-R-SD-1.0

|                               |                     |      |       |
|-------------------------------|---------------------|------|-------|
| TITLE                         | DFN-8/HSNT-8-A-Reel |      |       |
| No.                           | PP008-A-R-SD-1.0    |      |       |
| ANGLE                         |                     | QTY. | 5,000 |
| UNIT                          | mm                  |      |       |
|                               |                     |      |       |
| SII Semiconductor Corporation |                     |      |       |



No. PP008-A-L-SD-1.0

|                               |                                        |
|-------------------------------|----------------------------------------|
| TITLE                         | DFN-8/HSNT-8-A<br>-Land Recommendation |
| No.                           | PP008-A-L-SD-1.0                       |
| ANGLE                         |                                        |
| UNIT                          | mm                                     |
|                               |                                        |
| SII Semiconductor Corporation |                                        |

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