Dual Channel, Low Resistance Load Switch

General Description

The RT9736A is a small, low R_{ON}, dual channel load switch with EN controlled pin. The product contains two N-MOSFETs that can operate between an input voltage range of 0.8V to 5.5V. Also, it supports a maximum current of 6A each channel. Each switch is independently controlled by EN pins (EN1 and EN2), which can directly interface with low-voltage control signals.

The RT9736A is available in the WDFN-14TL 3x2 package with exposed pad for high power and heat dissipation.

Ordering Information

RT9736A □□

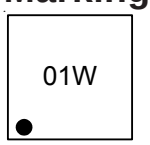
- Package Type
  QW : WDFN-14TL 3x2 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



01 : Product Code

W : Date Code

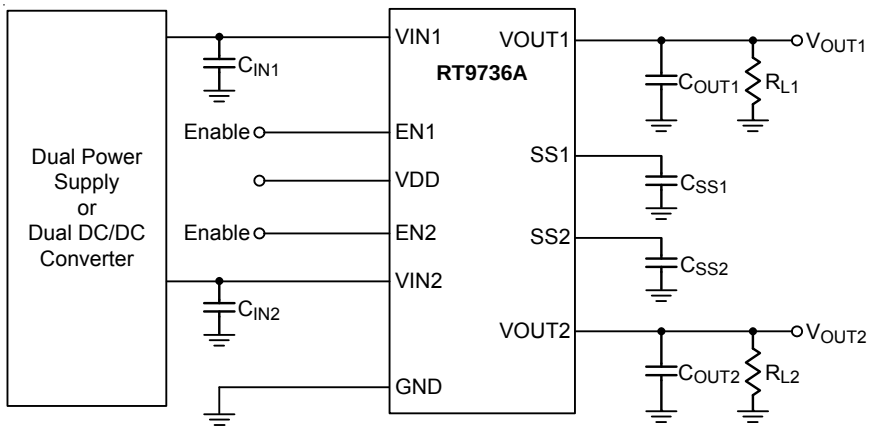
Features

- **Integrated Dual Channel Load Switch**
- **Input Voltage Range : 0.8V to 5.5V**
- **Low R_{ON} Resistance**
  - **R_{ON} = 38mΩ at V_{IN} = 5V (V_{DD} = 5V)**
  - **R_{ON} = 38mΩ at V_{IN} = 3.6V (V_{DD} = 5V)**
  - **R_{ON} = 38mΩ at V_{IN} = 1.8V (V_{DD} = 5V)**
- **6A Maximum Switch Current Per Channel**
- **Low Quiescent Current**
  - **75μA (Both Channels)**
  - **55μA (Single Channel)**
- **Low Control Input Threshold Enables Use of 1.4V/1.8V/2.5V/3.3V Logics**
- **Configurable Rise Time**
- **Quick Output Discharge (QOD)**
- **Adaptive Discharge Current**
- **14T-Lead WDFN Package with Thermal Pad**
- **RoHS Compliant and Halogen Free**

Applications

- Ultrabook™
- Notebooks/Netbooks
- Tablet PC
- Consumer Electronics
- Set-Top Boxes/Residential Gateways
- Telecom Systems
- Solid State Drives (SSD)

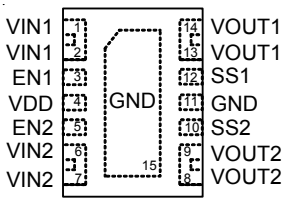
Simplified Application Circuit



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Pin Configurations

(TOP VIEW)



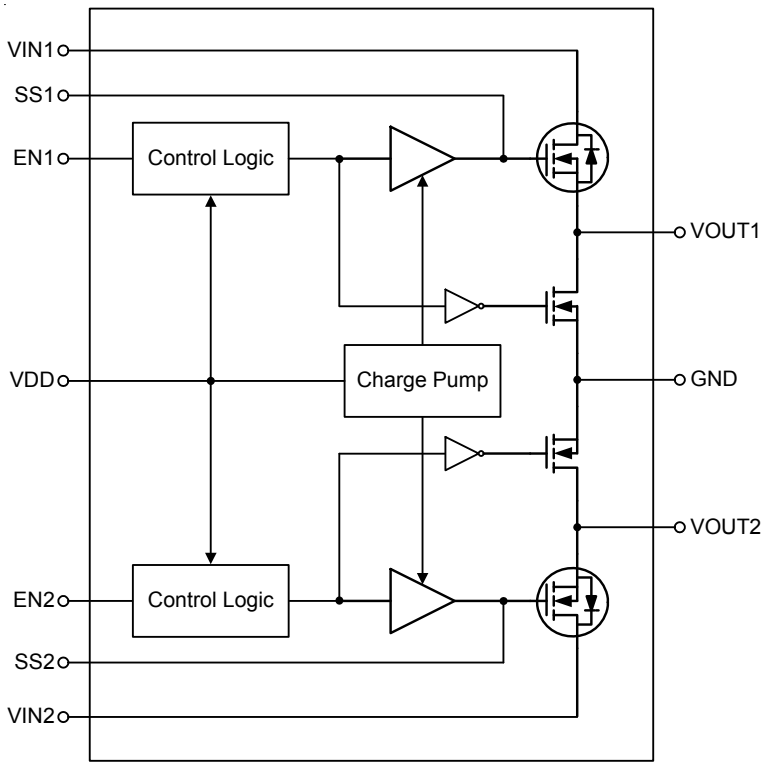
WDFN-14TL 3x2

Functional Pin Description

Pin No.	Pin Name	Pin Function
1, 2	VIN1	Input Voltage for Switch 1. Bypass this input with a ceramic capacitor to GND. Recommended voltage range for this pin for optimal R_{ON} performance is 0.8V to V_{DD}.
3	EN1	Enable Control Input for Switch 1 (Active High). Do not leave floating.
4	VDD	Charge Pump Voltage Input. Power supply to the device. Recommended voltage range for this pin is 2.5V to 5.5V.
5	EN2	Enable Control Input for Switch 2 (Active High). Do not leave floating.
6, 7	VIN2	Input Voltage for Switch 2. Bypass this input with a ceramic capacitor to GND. Recommended voltage range for this pin for optimal R_{ON} performance is 0.8V to V_{DD}.
8, 9	VOUT2	Switch 2 Output.
10	SS2	Switch 2 Slew Rate Control. Can be left floating.
11, 15 (Exposed Pad)	GND	Ground. The Exposed pad should be soldered to a large PCB and connected to GND for maximum thermal dissipation.
12	SS1	Switch 1 Slew Rate Control. Can be left floating.
13, 14	VOUT1	Switch 1 Output.

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Function Block Diagram



Operation

The RT9736A contains two N-MOSFETs which controlled by EN pin independently.

Enable Control

Asserting ENx pin high enables the switch. Switch will turn on as the EN signal is higher than V_{ENH}, and turn off when the EN signal is lower than V_{ENL}. Thus, it can operate under low voltage logic, please refer to the electrical characteristics. This pin cannot be left floating and must be tied either high or low voltage for proper functionality.

Charge Pump

Provides sufficient bias voltage to both N-MOSFETs.

Adjustable Rise Time

Connecting a capacitor to GND on the SSx pin sets the slew rate for each channel. It could also be used to prevent in-rush current.

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Absolute Maximum Ratings (Note 1)

- VIN1, VIN2, EN1, EN2, VDD, VOUT1, VOUT2, SS1, SS2 ---------- –0.3V to 6V
- Maximum Switch Current, Pulse <300μs, 15% Duty Cycle Per Channel, T_A = 25°C ---------- 6A
- Power Dissipation, P_D @ T_A = 25°C
  WDFN-14TL 3x2 ---------- 3.11W
- Package Thermal Resistance (Note 2)
  WDFN-14TL 3x2, θ_{JA} ---------- 32.1°C/W
  WDFN-14TL 3x2, θ_{JC} ---------- 6.3°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  CDM (Charged-Device Model) ---------- 1kV

Recommended Operating Conditions (Note 4)

- $V_{IN1,2}$, Input Voltage Range ---------- 0.8V to V_{DD}
- V_{DD}, Charge Pump Input Voltage Range ---------- 2.5V to 5.5V
- $V_{EN1,2}$, EN Voltage Range ---------- 0V to V_{DD}
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 0.8V to 5.5V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
EN Input Supply							
Input Voltage	High-Level	V_{ENH}		1.4	--	5.5	V
	Low-Level	V_{ENL}		0	--	0.5	
ENx Pin Input Leakage Current		I_{EN}	V_{EN} = 5.5V	--	--	1	μA

(V_{DD} = 5V, V_{IN} = 0.8V to V_{DD}, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supplies and Currents						
V_{DD} Quiescent Current (Both Channels)	$I_{IN(VDD, ON)}$	I_{OUT1} = I_{OUT2} = 0A $V_{IN1,2}$ = $V_{EN1,2}$ = V_{DD} = 5V	--	75	115	μA
V_{DD} Quiescent Current (Single Channel)	$I_{IN(VDD, ON)}$	I_{OUT1} = I_{OUT2} = 0A $V_{IN1,2}$ = V_{EN1} = V_{DD} = 5V, V_{EN2} = GND	--	55	--	μA
V_{DD} Shutdown Current	$I_{IN(VDD, OFF)}$	$V_{EN1,2}$ = GND, $V_{OUT1,2}$ = 0V	--	--	2	μA

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Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
$V_{IN1,2}$ Off-State Supply Current (Per Channel)	$I_{IN(VIN, OFF)}$	$V_{EN1,2}$ = GND, $V_{OUT1,2}$ = 0V	$V_{IN1,2}$ = 5V	--	--	8	μA
			$V_{IN1,2}$ = 3.3V	--	--	3	
			$V_{IN1,2}$ = 1.8V	--	--	2	
			$V_{IN1,2}$ = 0.8V	--	--	1	
Resistance Characteristics							
ON-State Resistance	R_{ON}	I_{OUT} = –200mA, V_{DD} = 5V	V_{IN} = 5V	--	38	44	mΩ
			V_{IN} = 3.3V	--	38	44	
			V_{IN} = 1.8V	--	38	44	
			V_{IN} = 1.5V	--	38	44	
			V_{IN} = 1.2V	--	38	44	
			V_{IN} = 0.8V	--	38	44	
Output Pull-down Resistance	R_{PD}	V_{EN} = 0V, V_{IN} = 5V, I_{OUT} = 15mA		--	220	300	Ω

(V_{DD} = 3.3V, V_{IN} = 0.8V to V_{DD}, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Power Supplies and Currents							
V_{DD} Quiescent Current (Both Channels)	$I_{IN(VDD, ON)}$	I_{OUT1} = I_{OUT2} = 0A $V_{IN1,2}$ = $V_{EN1,2}$ = V_{DD} = 3.3V		--	40	--	μA
V_{DD} Quiescent Current (Single Channel)	$I_{IN(VDD, ON)}$	I_{OUT1} = I_{OUT2} = 0A $V_{IN1,2}$ = V_{EN1} = V_{DD} = 3.3V, V_{EN2} = GND		--	--	--	μA
V_{DD} Shutdown Current	$I_{IN(VDD, OFF)}$	$V_{EN1,2}$ = GND, $V_{OUT1,2}$ = 0V		--	--	2	μA
$V_{IN1,2}$ Off-State Supply Current (Per Channel)	$I_{IN(VIN, OFF)}$	$V_{EN1,2}$ = GND, $V_{OUT1,2}$ = 0V	$V_{IN1,2}$ = 3.3V	--	--	3	μA
			$V_{IN1,2}$ = 1.8V	--	--	2	
			$V_{IN1,2}$ = 1.2V	--	--	2	
			$V_{IN1,2}$ = 0.8V	--	--	1	
Resistance Characteristics							
On-State Resistance	R_{ON}	I_{OUT} = –200mA, V_{DD} = 3.3V	V_{IN} = 3.3V	--	42	--	mΩ
			V_{IN} = 2.5V	--	40	--	
			V_{IN} = 1.8V	--	39	--	
			V_{IN} = 1.5V	--	38	--	
			V_{IN} = 1.2V	--	38	--	
			V_{IN} = 0.8V	--	38	--	
Output Pull-down Resistance	R_{PD}	V_{EN} = 0V, V_{IN} = 3.3V, I_{OUT} = 1mA		--	260	300	Ω

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

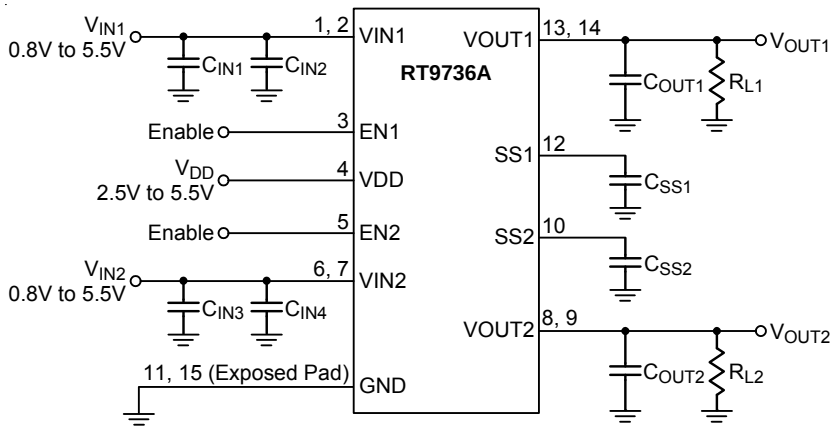
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

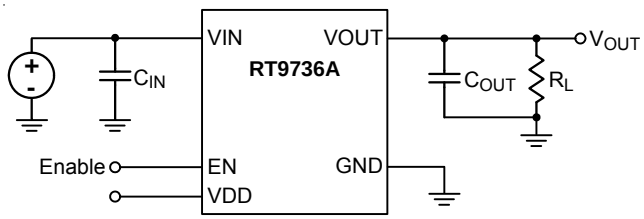
Note 4. The device is not guaranteed to function outside its operating conditions.

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Typical Application Circuit



Timing Diagram



Single Channel Shown for Clarity

TEST CIRCUIT

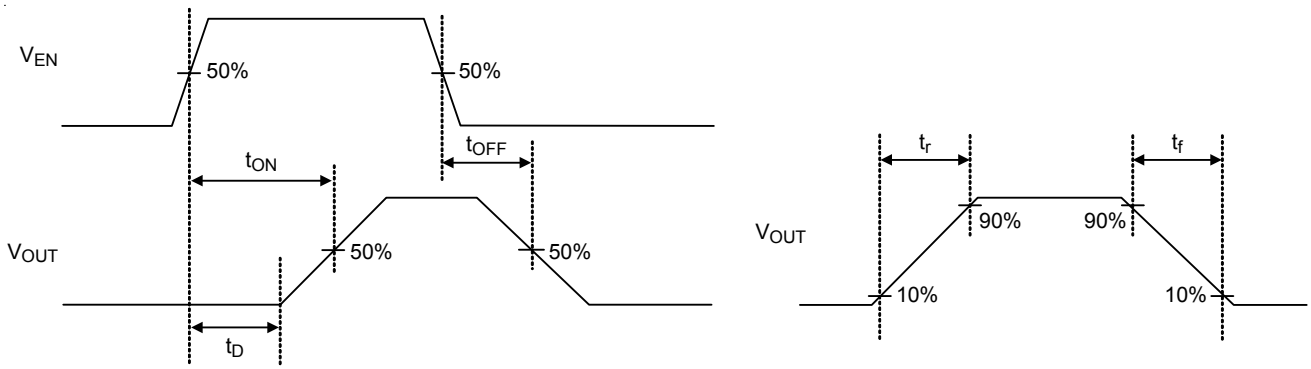


Figure 1. Test Circuit and t_{ON}/t_{OFF} Waveforms

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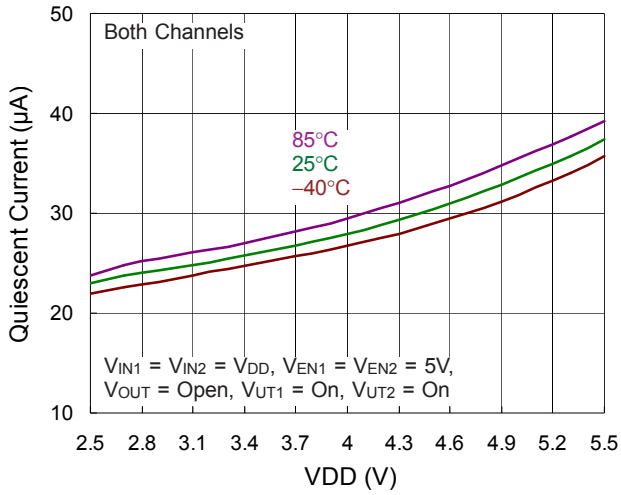
Timing Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
VIN = EN = VDD = 5V, T_A = 25°C						
T_{ON}	Turn-On Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	1220	--	μs
T_{OFF}	Turn-Off Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	4	--	
T_R	VOUT Rise Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	1350	--	
T_F	VOUT Fall Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	3	--	
T_D	ON Delay Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	400	--	
VIN = 0.8V, EN = VDD = 5V, T_A = 25°C						
T_{ON}	Turn-On Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	580	--	μs
T_{OFF}	Turn-Off Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	80	--	
T_R	VOUT Rise Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	280	--	
T_F	VOUT Fall Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	20	--	
T_D	ON Delay Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	400	--	
VIN = EN = VDD = 3.3V, T_A = 25°C						
T_{ON}	Turn-On Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	960	--	μs
T_{OFF}	Turn-Off Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	6	--	
T_R	VOUT Rise Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	940	--	
T_F	VOUT Fall Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	3	--	
T_D	ON Delay Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	400	--	
VIN = 0.8V, EN = VDD = 3.3V, T_A = 25°C						
T_{ON}	Turn-On Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	560	--	μs
T_{OFF}	Turn-Off Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	175	--	
T_R	VOUT Rise Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	280	--	
T_F	VOUT Fall Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	40	--	
T_D	ON Delay Time	R_L = 10Ω, C_{OUT} = 0.1μF, C_{SS} = 1000pF	--	400	--	

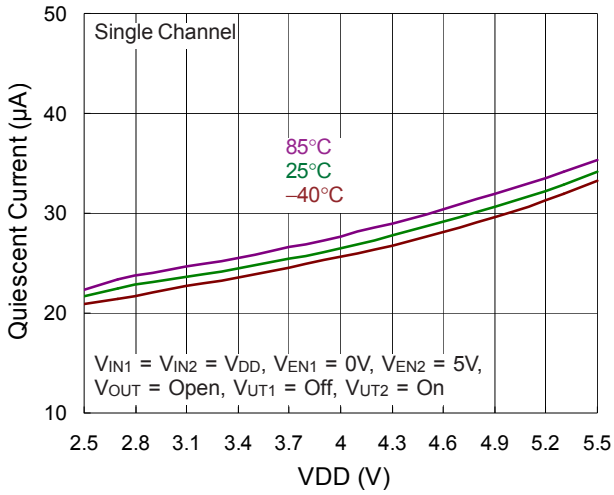
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Typical Operating Characteristics

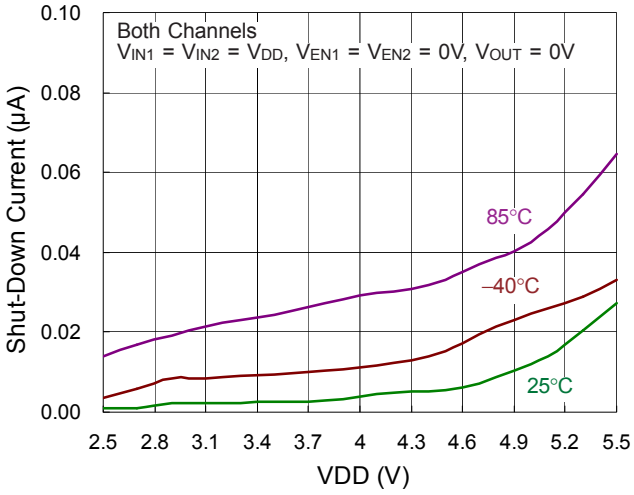
Quiescent Current vs. VDD



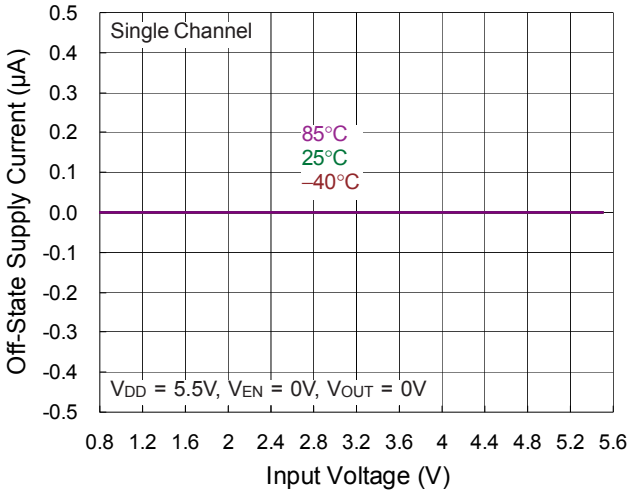
Quiescent Curren vs. VDD



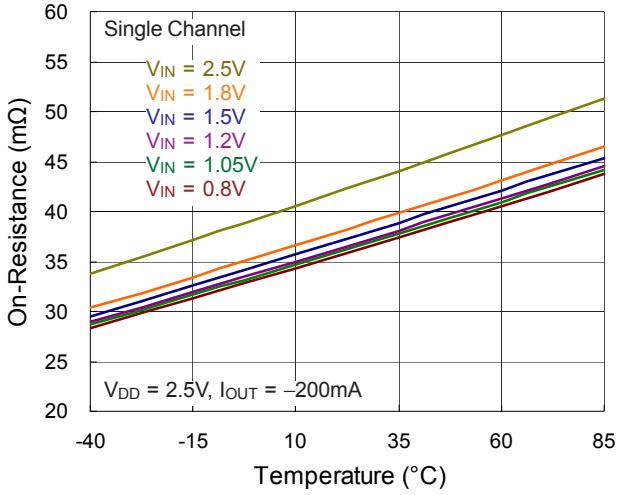
Shut-Down Current vs. VDD



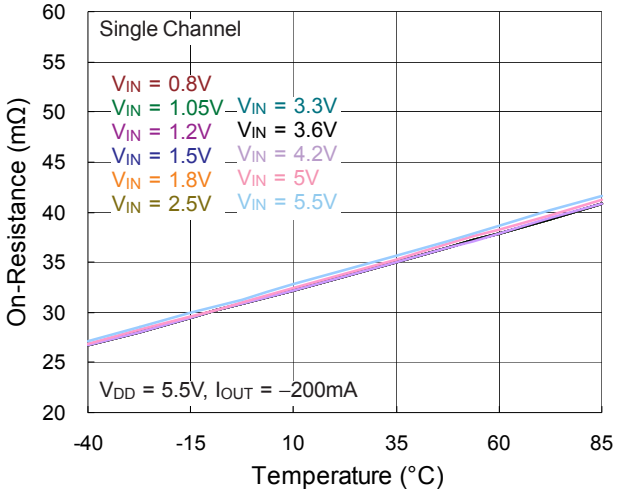
Off-State Supply Current vs. Input Voltage



On-Resistance vs. Temperature

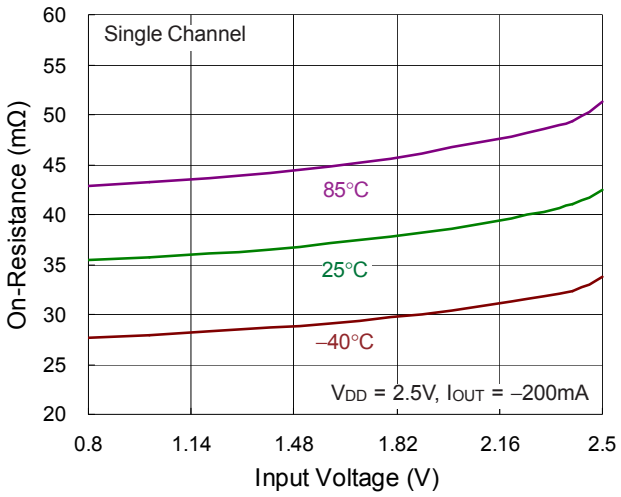


On-Resistance vs. Temperature

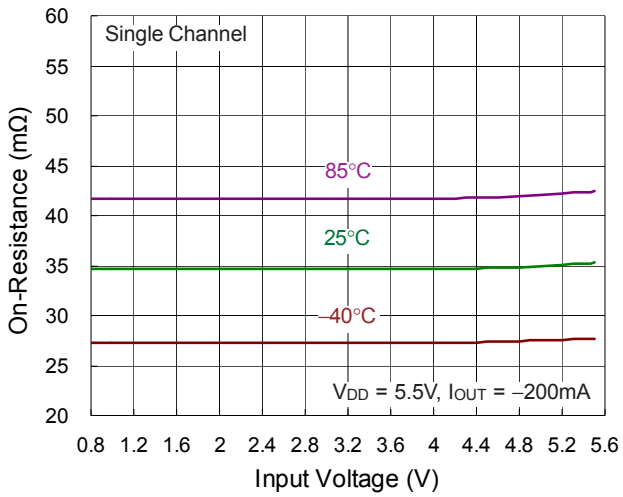


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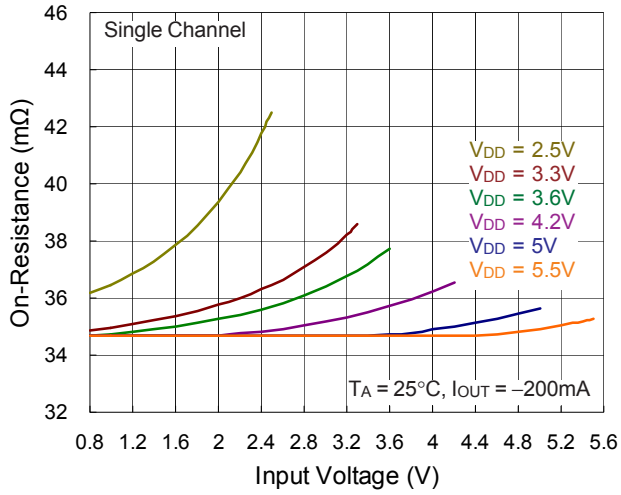
On-Resistance vs. Input Voltage



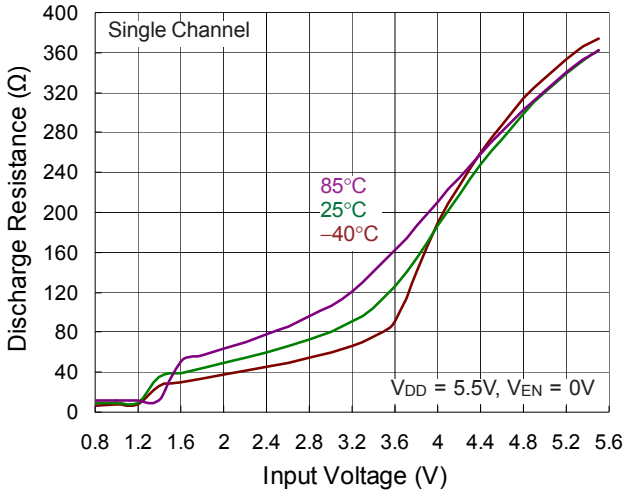
On-Resistance vs. Input Voltage



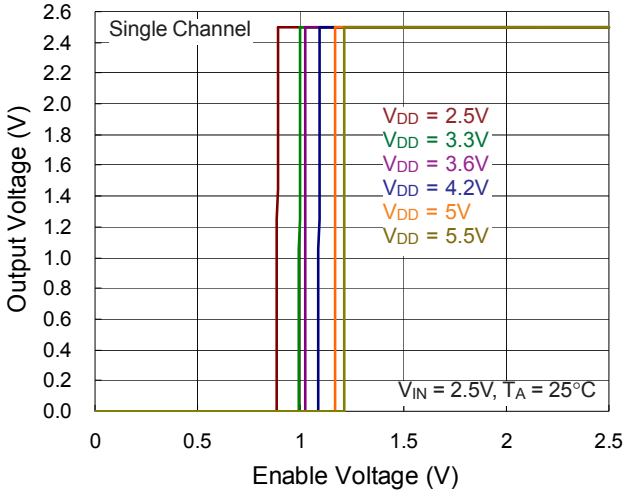
On-Resistance vs. Input Voltage



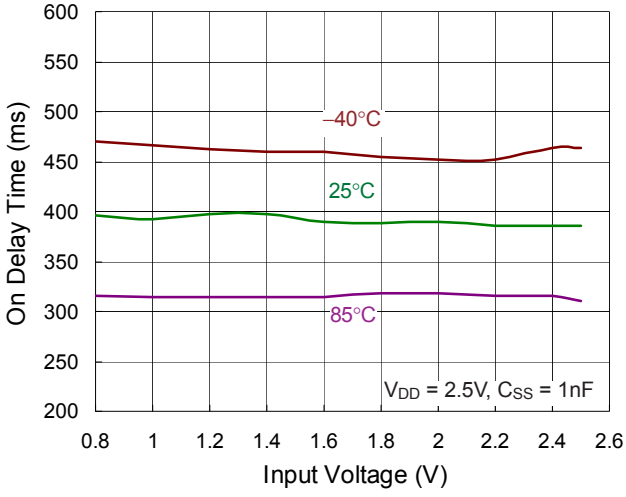
Discharge Resistance vs. Input Voltage



Output Voltage vs. Enable Voltage

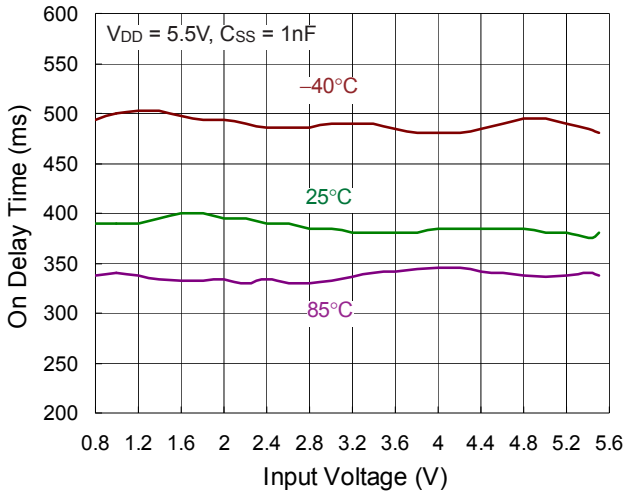


On Delay Time vs. Input Voltage

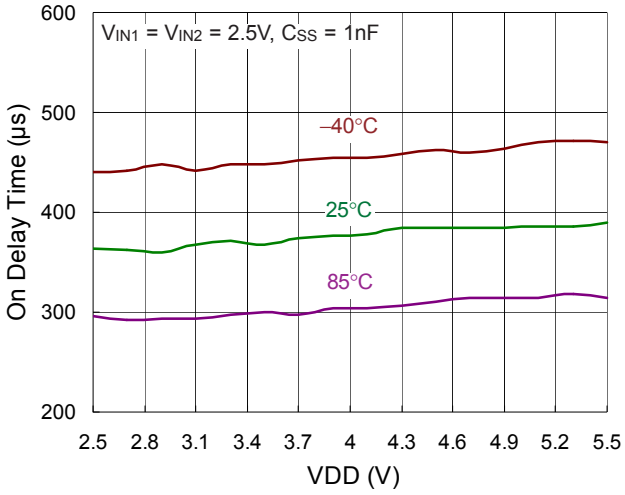


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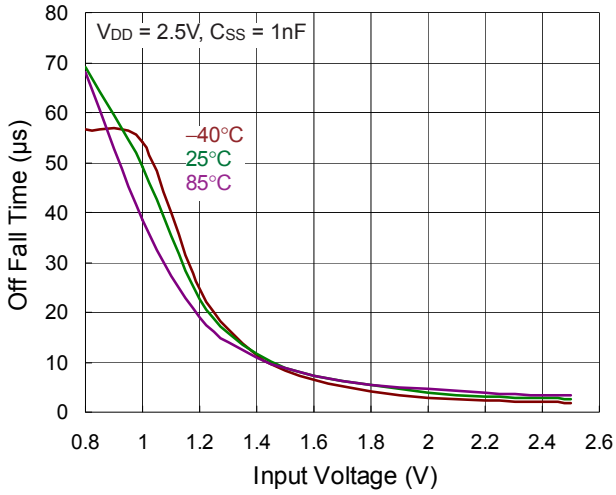
On Delay Time vs. Input Voltage



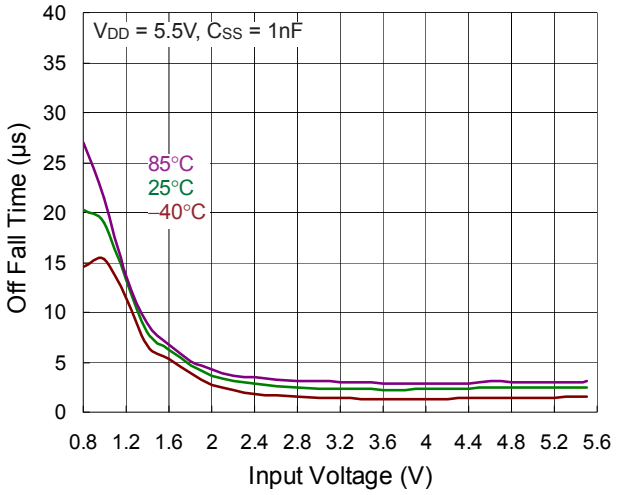
On Delay Time vs. VDD



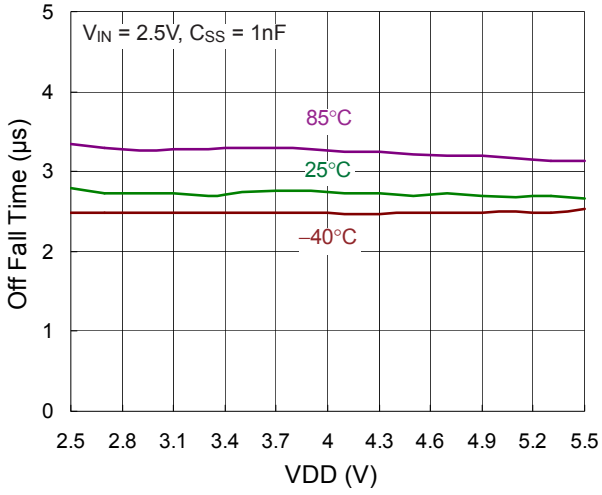
Off Fall Time vs. Input Voltage



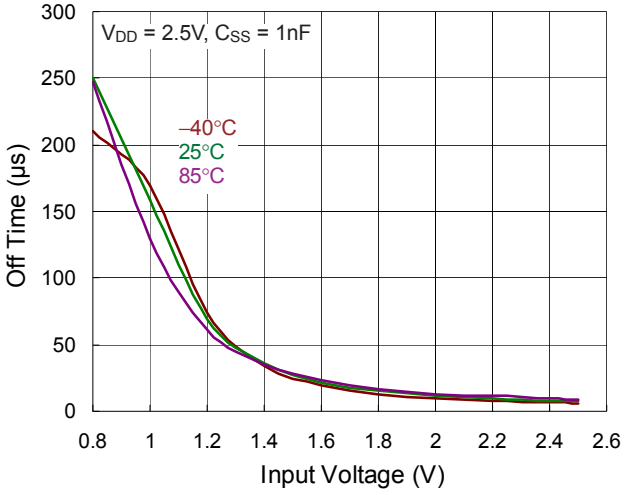
Off Fall Time vs. Input Voltage



Off Fall Time vs. VDD

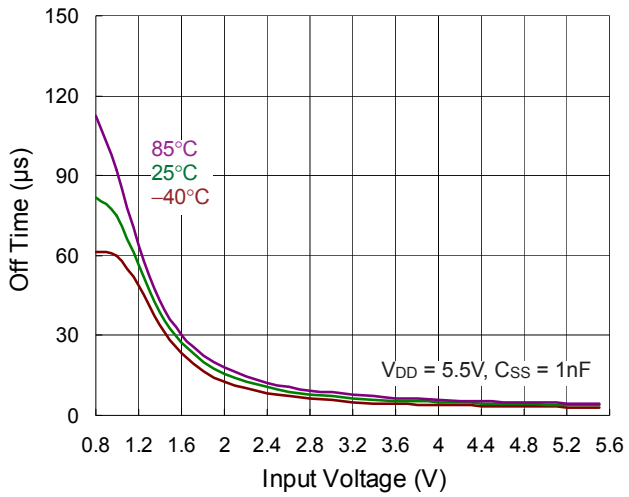


Off Time vs. Input Voltage

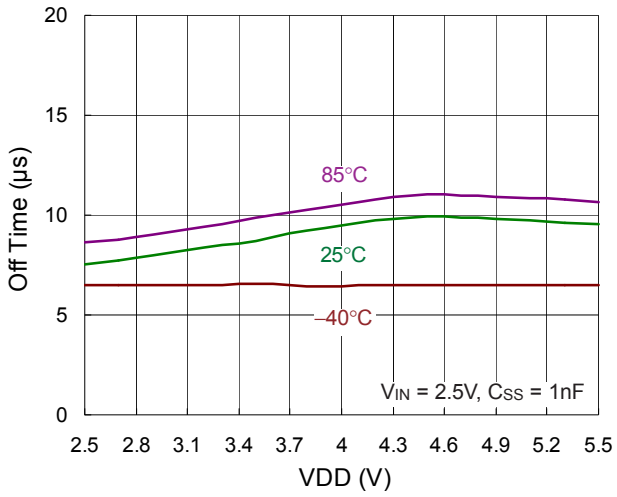


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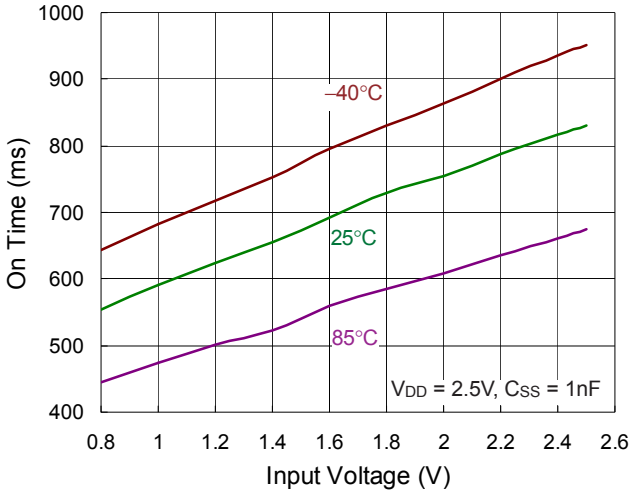
Off Time vs. Input Voltage



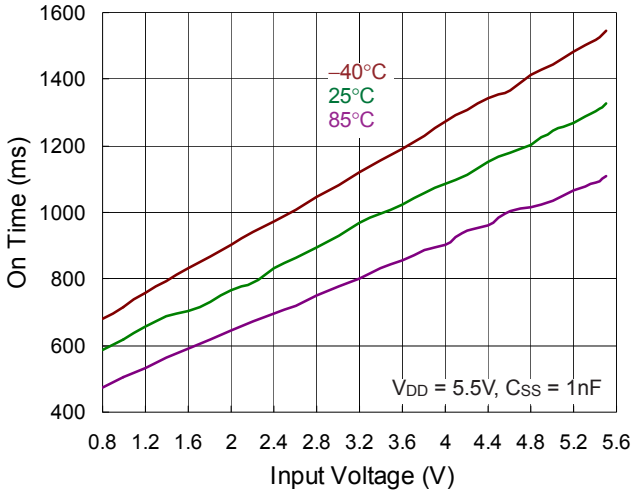
Off Time vs. VDD



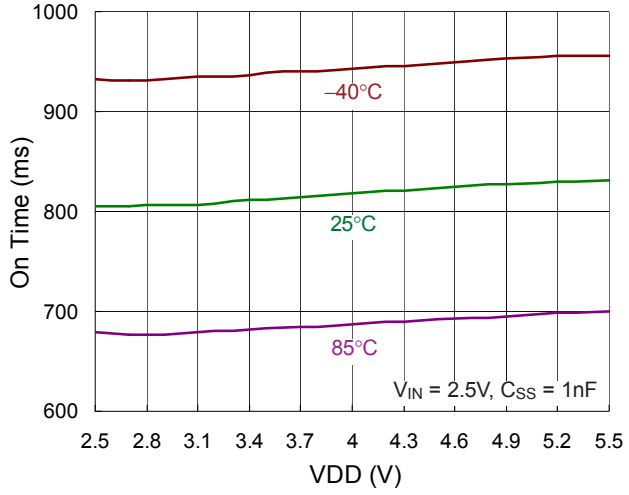
On Time vs. Input Voltage



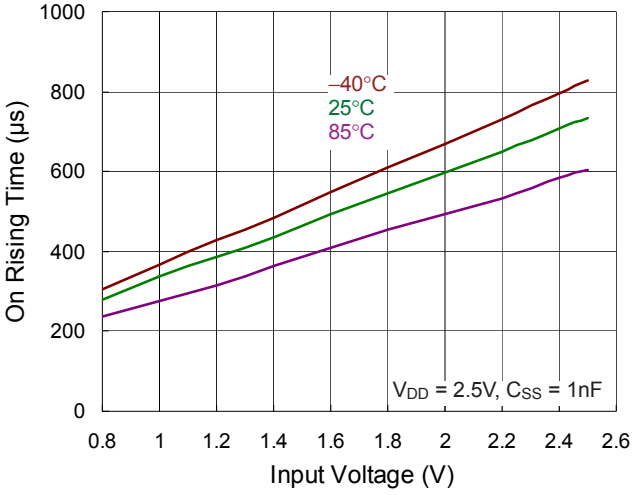
On Time vs. Input Voltage



On Time vs. VDD

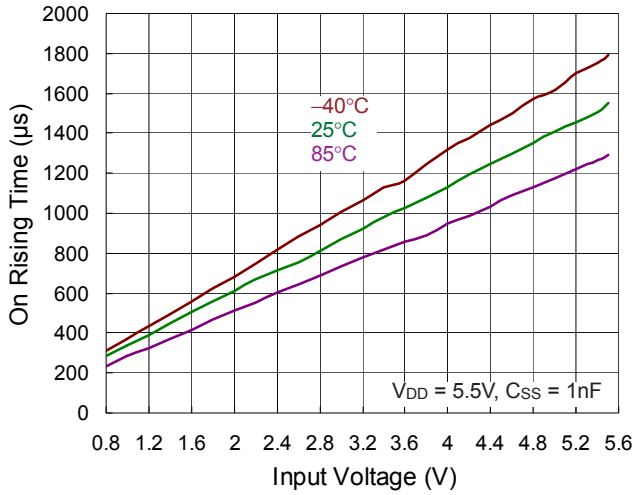


On Rising Time vs. Input Voltage

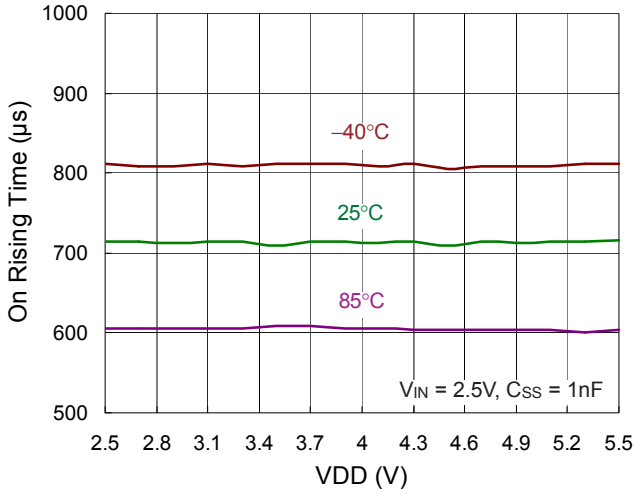


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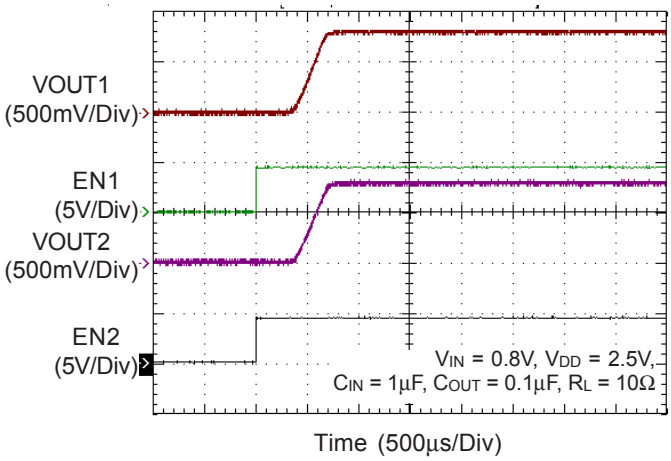
On Rising Time vs. Input Voltage



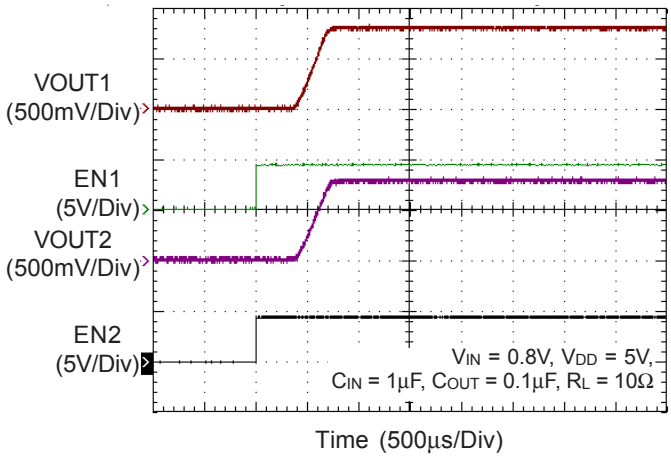
On Rising Time vs. VDD



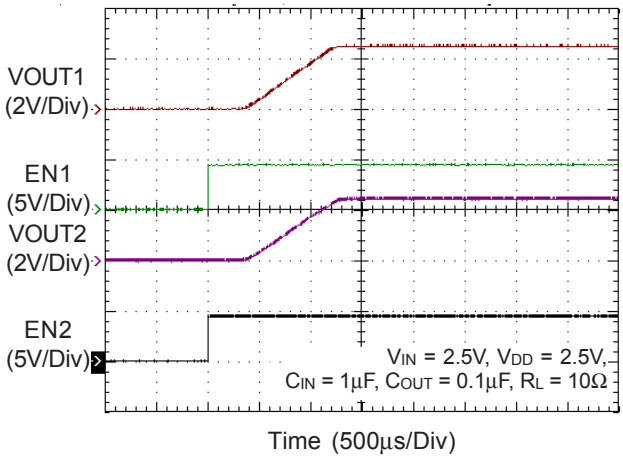
Turn-On Response Time



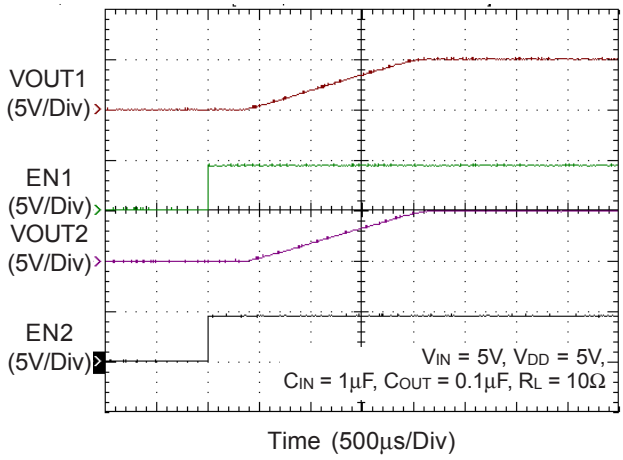
Turn-On Response Time



Turn-On Response Time

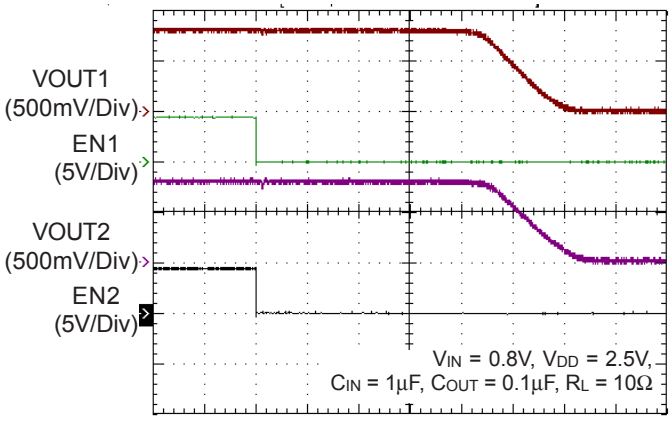


Turn-On Response Time

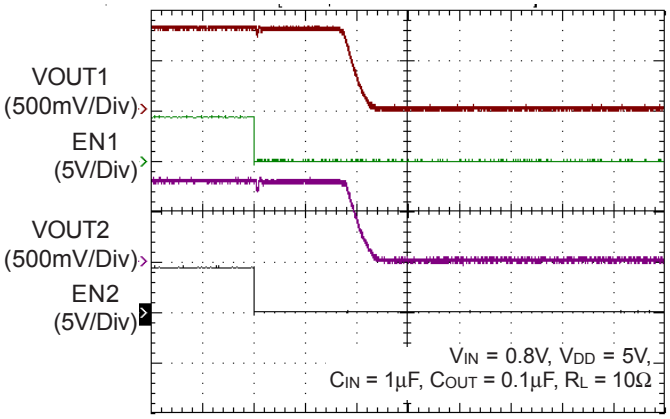


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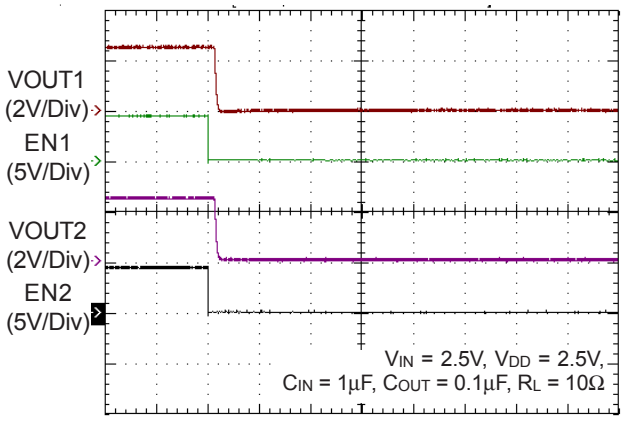
Turn-Off Response Time



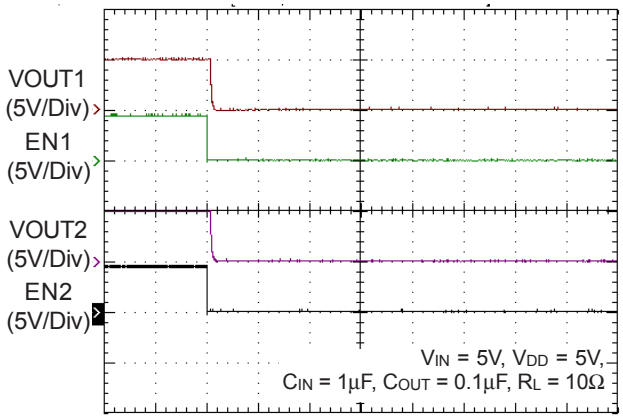
Turn-Off Response Time



Turn-Off Response Time



Turn-Off Response Time



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Application Information

The RT9736A is a small, low R_{ON}, dual channel load switch with EN controlled pins, and is equipped with a charge pump circuitry to drive the internal N-MOSFET switch. The product contains two N-MOSFETs that can operate between input voltage range of 0.8V to 5.5V. It also supports a maximum current of 6A each channel (T_A = 25°C, 15% Duty Cycle Per Channel, pulse < 300μs). Each switch is independently controlled by EN pins (EN1 and EN2), which can directly interface with low-voltage control signals.

Input and Output

VINx (input) is the power source connection to the internal circuitry and the Drain of the MOSFET. VOUTx (output) is the Source of the MOSFET. In a typical application, current flows through the switch from VINx to VOUTx toward the load. If VOUTx is greater than VINx, current will flow from VOUTx to VINx since the MOSFET is bidirectional when on.

Chip Enable Input

The switch will be disabled when the ENx pin is in a logic low condition. During this condition, the internal circuitry and MOSFET will be turned off, reducing the supply current to 0.1μA typical. Floating the ENx may cause unpredictable operation. ENx should not be allowed to go negative with respect to GND.

Supply Filter/Bypass Capacitor

A 1μF or greater low-ESR ceramic capacitor from VIN to GND, located at the device is strongly recommended to prevent the input voltage drooping during high current application. However, higher capacitor values will further reduce the voltage droop on the input. Furthermore, without the bypass capacitor, an output short may cause sufficient ringing on the input (from source lead inductance) to destroy the internal control circuitry. The input transient must not exceed 6V of the absolute maximum supply voltage even for a short duration.

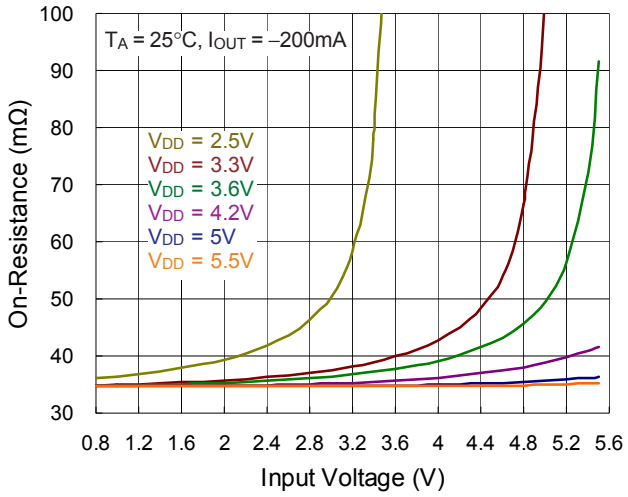
Output Filter Capacitor

A 10 to 1 ratio of supply capacitor to output capacitor from VOUTx to GND is recommended to prevent the in-rush currents during low supply voltage start-up. Because the integrated body diode in the load switch, higher output capacitor can cause output voltage to exceed supply voltage when the system supply is removed. A output capacitor smaller then supply capacitor is recommended to prevent the current flow through the integrated body diode from output to system supply.

Charge Pump

The switch has an internal charge pump circuit that is supplied from VDD pin to afford sufficient bias voltage to both N-Channel MOSFETs. The recommended VDD voltage range is 2.5V to 5.5V, and must above VIN for optimal low R_{ON} performance, or the value of R_{ON} will be greater than the value listed in the ELECTRICAL CHARACTERISTICS table.

On-Resistance vs. Input Voltage (VIN > VDD, Single Channel)



Adjustable Rise Time

The RT9736A provides an external adjustable rise time function. The adjustable rise time is used to prevent large inrush current and output voltage overshoot while the switch is being powered-up. The external capacitor connected from SS pins to GND is charged by a 1μA current source to set each rise time.

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Discharge Operation

When ENx is low, the RT9736A will discharge the system residual voltage using internal MOSFET connected between the VOUTx and GND. The discharge current depends on the voltage at the VOUTx pin. When the voltage at the VOUTx is lower than 0.8V, the RT9736A will fully turn the internal MOSFET on to pull the VOUTx low.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WDFN-14TL 3x2 package, the thermal resistance, θ_{JA}, is 32.1°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (32.1°C/W) = 3.11W for WDFN-14TL 3x2 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 2 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

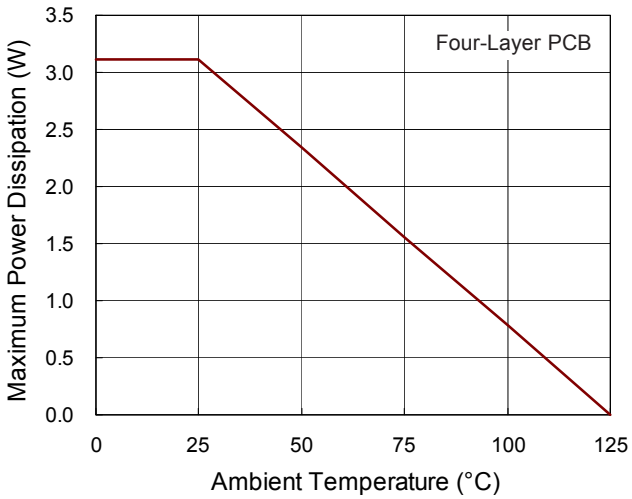
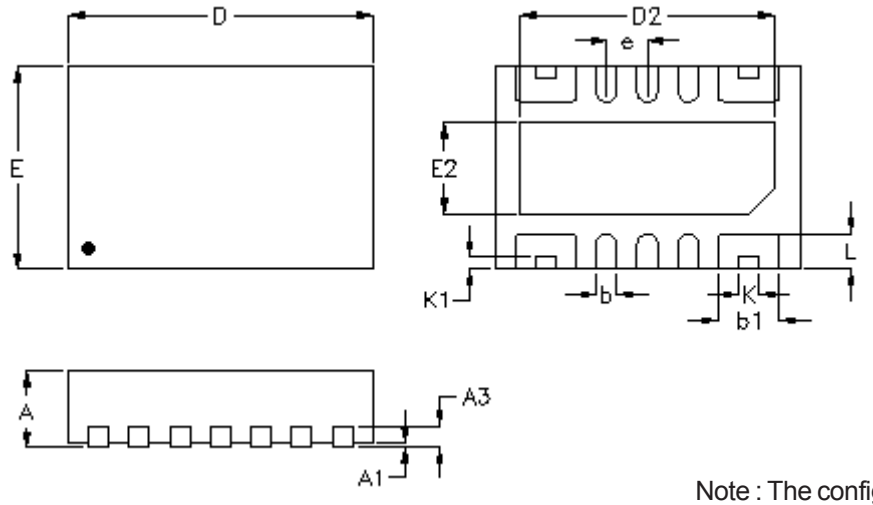
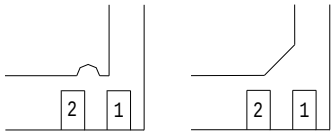


Figure 2. Derating Curve of Maximum Power Dissipation

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Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
b1	0.550	0.650	0.022	0.026
D	2.900	3.100	0.114	0.122
D2	2.450	2.550	0.096	0.100
E	1.900	2.100	0.075	0.083
E2	0.850	0.950	0.033	0.037
e	0.400		0.016	
K	0.200		0.008	
K1	0.120		0.005	
L	0.300	0.400	0.012	0.016

W-Type 14TL DFN 3x2 Package

Richtek Technology Corporation

14F, No. 8, Tai Yuen 1st Street, Chupei City

Hsinchu, Taiwan, R.O.C.

Tel: (8863)5526789

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