I²C Programmable White LED Driver with Dual LDO

General Description

The RT9367C is an integrated solution for backlighting and phone camera input supply. The part contains a charge pump white LED driver and dual low dropout linear regulators. This IC can be shutdown by pulling ENA low.

In the section of charge pump, The RT9367C can power up 4 white LEDs with regulated constant current for uniform intensity. Each channel (LED1-LED4) can support up to 25mA. The part maintains highest efficiency by utilizing a x1/x1.5/x2 fractional charge pump and low dropout current regulators. An internal 5-bit DAC is used for brightness control. Users can easily configure up to 32-step of LED current by I²C interface.

In the section of linear regulator, The RT9367C comprises a dual channel, low noise, and low dropout regulator sourcing up to 300mA at each channel. The range of output voltage can be configured from 1.1V to 3.3V by I²C interface. The outputs of LDO offer 3% accuracy and low dropout voltage of 250mV @300mA. The LDO also provides current limiting and output short circuit thermal folded back protection.

Ordering Information

RT9367C□□

- Package Type
  QW : WQFN-20L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
  Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

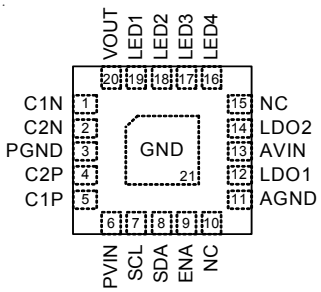
- **An Integrated Solution for Backlighting and Phone Camera Input Supply**
- **I²C Programmable, 32 Steps Dimming Control and Independent Channel On/Off Control**
- **Over Temperature Protection**
- **Power On Reset for Data Register**
- **Typical 1uA Low Shutdown Current with Interface Fully On**
- **Charge Pump White LED Driver**
  - **Over 93% Peak Efficiency Over Li-ion Battery Discharge**
  - **Typical 85% Average Efficiency Over Li-ion Battery Discharge**
  - **Support Up to 4 White LEDs**
  - **Output Current Up to 25mA/Channel 100mA Total**
  - **60mV Typical Current Source Dropout**
  - **1% Typical LED Current Accuracy**
  - **0.7% Typical LED Current Matching**
  - **Automatic x1/x1.5/x2 Charge Pump Mode Transition**
  - **Low Input Noise and EMI Charge Pump**
  - **5.5V Over Voltage Protection**
  - **Power On/Mode Transition In-rush Protection**
  - **1MHz Random Frequency Oscillator**
  - **Typical 0.1uA Low Shutdown Current**
- **Dual LDO**
  - **Wide Operating Voltage Range**
  - **Low-Noise Output**
  - **No Noise Bypass Capacitor Required**
  - **Fast Response in Line/Load Transient**
  - **Low Temperature Coefficient**
  - **Dual LDO Outputs (300mA/300mA)**
  - **3% Max Output Accuracy**
  - **Current Limit Protection**
  - **Short Circuit Thermal Folded Back Protection**
  - **Typical 0.1uA Low Shutdown Current**
- **RoHS Compliant and Halogen Free**

Applications

- Camera Phone, Smart Phone
- White LED Backlighting, CMOS Sensor Input Supply

Pin Configurations

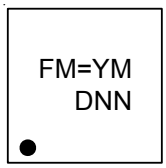
(TOP VIEW)



WQFN-20L 3x3

Marking Information

RT9367CGQW



FM= : Product Code

YMDNN : Date Code

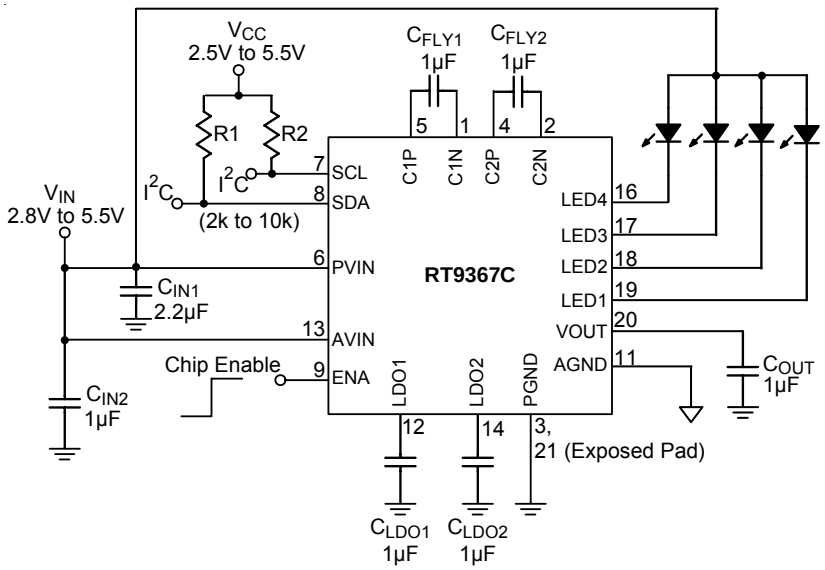
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FM : Product Code

YMDNN : Date Code

Typical Application Circuit



Timing Diagram

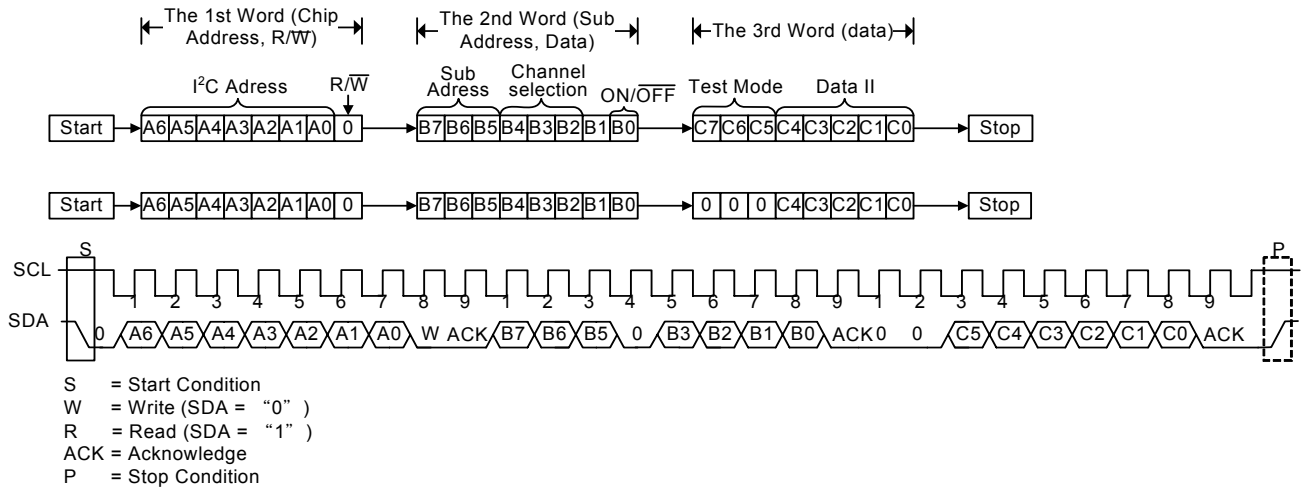


Figure 1. I²C Interface Trimming Diagram

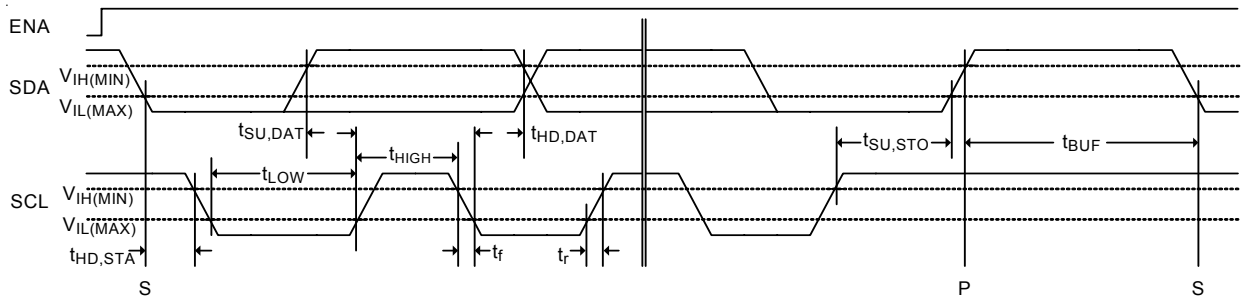
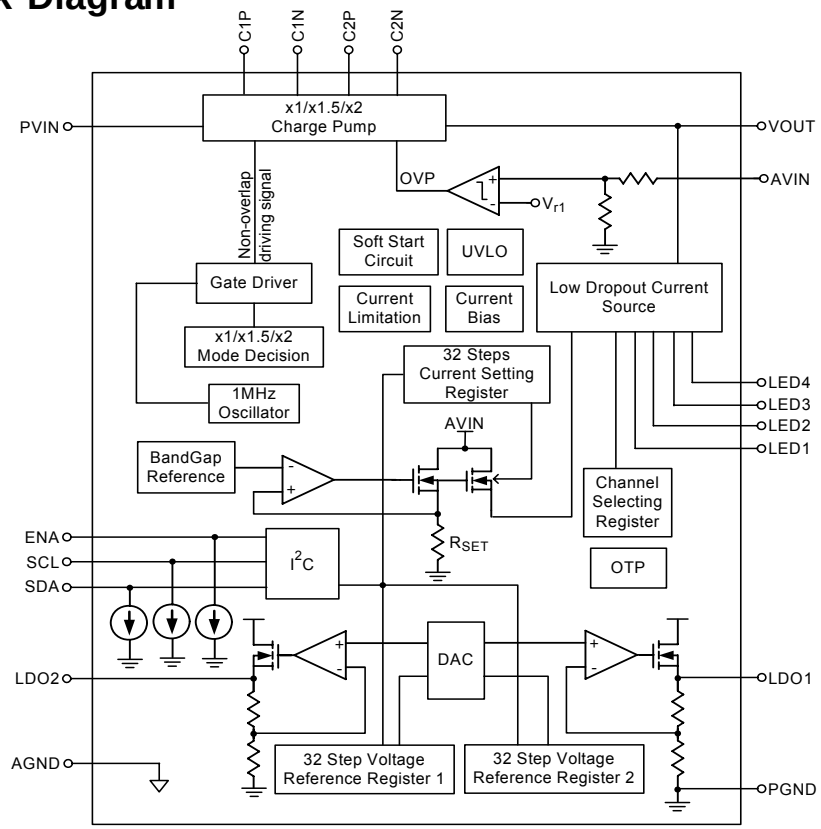


Figure 2

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	C1N	Fly Capacitor 1 Negative Connection.
2	C2N	Fly Capacitor 2 Negative Connection.
3	PGND	Power Ground.
4	C2P	Fly Capacitor 2 Positive Connection.
5	C1P	Fly Capacitor 1 Positive Connection.
6	PVIN	Power Input.
7	SCL	I^2C Clock Input.
8	SDA	I^2C Data Input.
9	ENA	Chip Enable (Active High).
10, 15	NC	No Internal Connection.
11	AGND	Analog Ground.
12	LDO1	LDO 1 Output.
13	AVIN	Analog Power Input.
14	LDO2	LDO 2 Output.
16	LED4	Current Sink for LED4.
17	LED3	Current Sink for LED3.
18	LED2	Current Sink for LED2.
19	LED1	Current Sink for LED1.
20	VOUT	Charge Pump Output.
21 (Exposed Pad)	GND	The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, AVIN, PVIN ---------- –0.3V to 6V
- Output Voltage, VOUT ---------- –0.3V to 6V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WQFN-20L 3x3 ---------- 1.471W
- Package Thermal Resistance (Note 2)
  WQFN-20L 3x3, θ_{JA} ---------- 68°C/W
  WQFN-20L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = AVIN = PVIN = 3.6V, C_{IN1} = 2.2uF, C_{IN2} = 1uF, C_{OUT} = 1uF, C_{FLY1} = C_{FLY2} = 1uF, V_F = 3.5V, I_{LED1} = I_{LED2}= I_{LED3} = I_{LED4} = 15mA, T_A = 25°C, unless otherwise specification)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Power Supply						
Input Supply Voltage	V_{IN}		2.8	--	5.5	V
Shutdown Current	I_{SHDN}	V_{IN} = 5V, ENA = 0V	--	1	7	μA
Charge Pump LED Driver Block						
Under-Voltage Lockout Threshold		V_{IN} Rising.	1.8	2.0	2.5	V
Under-Voltage Lockout Hysteresis			--	100	--	mV
Quiescent of x1 Mode	I_{Q_x1}		--	1	2.5	mA
Quiescent of x2 Mode	I_{Q_x2}		--	3.5	7	mA
LED Current						
I_{LEDX} Accuracy	$I_{LED-ERR}$	I_{LEDX} = 15mA	–8	0	+8	%
Current Matching		I_{LEDX} = 15mA	–5	0	+5	%
Oscillator Frequency	f_{OSC}		--	1000	--	kHz
Mode Decision						
x1 Mode to x2 Mode Transition Voltage	V_{TS_x2}	V_{IN} Falling	--	3.65	3.8	V
Mode Transition Hystersis			--	250	--	mV

To be continued

(V_{IN} = AVIN = PVIN = V_{LDOX} + 1V, C_{IN2} = C_{LDO1} = C_{LDO2} = 1uF, T_A = 25°C, unless otherwise specified.)

Parameter		Symbol	Conditions	Min	Typ	Max	Unit
LDO Block							
Dropout Voltage		V_{DROP}	V_{LDOx} = 3.3V, I_{OUT} = 300mA	--	240	--	mV
Output Voltage Range		V_{LDOx}		1.1	--	3.3	V
VOUT Accuracy		ΔV	I_{OUT} = 1mA	–3	--	3	%
Line Regulation		ΔV_{LINE}	V_{IN} = (V_{OUT} + 0.3V) to 5.5V or V_{IN} > 2.5V, whichever is larger	--	0.01	0.2	%/V
Load Regulation		ΔV_{LOAD}	1mA < I_{OUT} < 300mA	--	0.01	0.6	%
Current Limit		I_{LIM}	R_{LOAD} = 1Ω	330	500	700	mA
Quiescent Current		I_Q		--	60	100	μA
Output Voltage Temperature Coefficent				--	100	--	ppm/°C
Thermal Shutdown		T_{SD}		--	170	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		--	40	--	°C
I^2C Block							
Input High Voltage		V_{IH}		1.5	--	5.5	V
Input Low Voltage		V_{IL}		0	--	0.4	V
Clock Operating Frequency		f_{SCL}		--	--	400	kHz
Output Low Level		V_{OL}	I_{SDA} = 3mA	--	--	0.4	V
Input High Level Current of SCL, SDA		I_{IH}		--	2	--	μA
Bus Free Time Between a STOP and START Condition		t_{BUF}	(Note 5)	1.3	--	--	μs
Hold Time After START Condition		$t_{HD,STA}$	(Note 5)	0.6	--	--	μs
Data Setup Time		$t_{SU,DAT}$	(Note 5)	200		--	ns
Set-Up Time for STOP Condition		$t_{SU,STO}$	(Note 5)	0.6	--	--	μs
Input Date Hold Time		$t_{HD,DAT}$	(Note 5)	200	--	900	ns
Low Period of the SCL Clock		t_{LOW}	(Note 5)	1.3	--	--	μs
High Period of the SCL Clock		t_{HIGH}	(Note 5)	0.6	--	--	μs
Clock Data Fall Time		t_f	(Note 5)	20	--	300	ns
Clock Data Rise Time		t_r	(Note 5)	20	--	300	ns
Input Low Time for Shutdown		t_{SHDN}	(Note 6) Both SCL and SDA are floating	400	1000	2000	μs
ENA Threshold	Logic-High Voltage	V_{IH}		1.5	--	--	V
	Logic-Low Voltage	V_{IL}		--	--	0.4	

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. θ_{JA} is measured in the natural convection at T_A = 25°C on a high effective four layers thermal conductivity test board of JEDEC 51-7 thermal measurement standard. The case point of θ_{JC} is on the expose pad for the WQFN package.

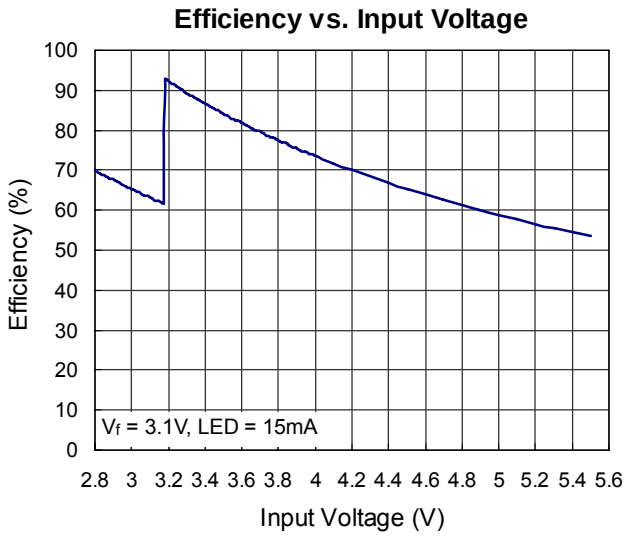
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

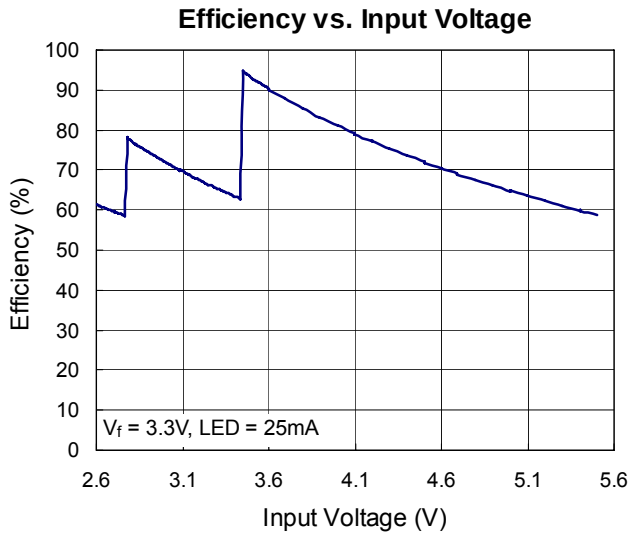
Note 4. The device is not guaranteed to function outside its operating conditions.

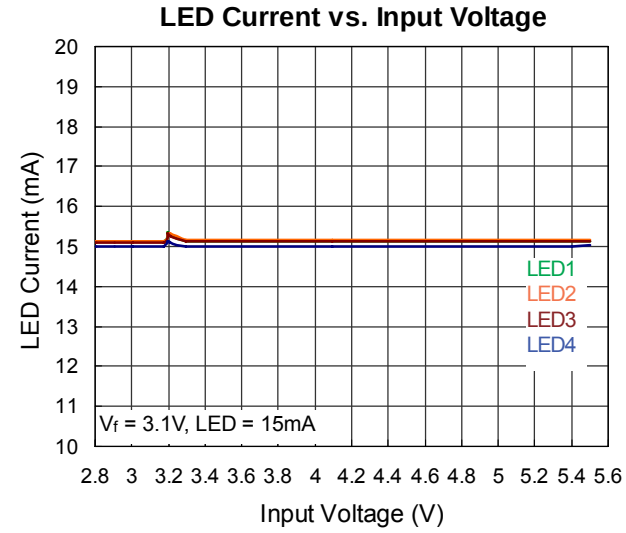
Note 5. All values are referred to V_{IH} and V_{IL} levels.

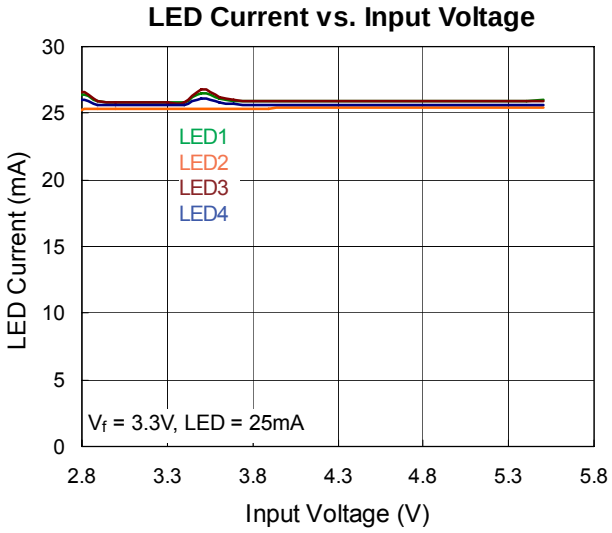
Note 6. In normal operation, the low time of both SCL and SDA must be less than 200us.

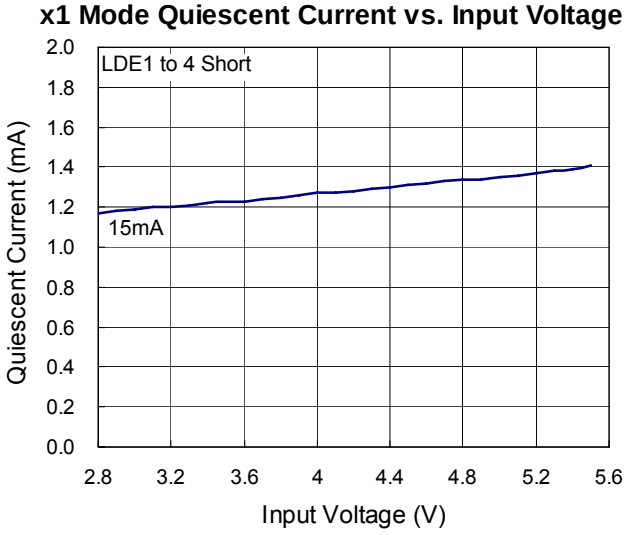
Typical Operating Characteristics

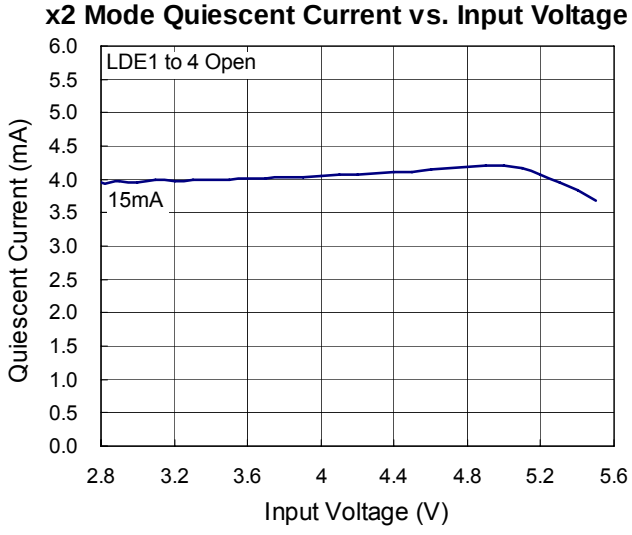




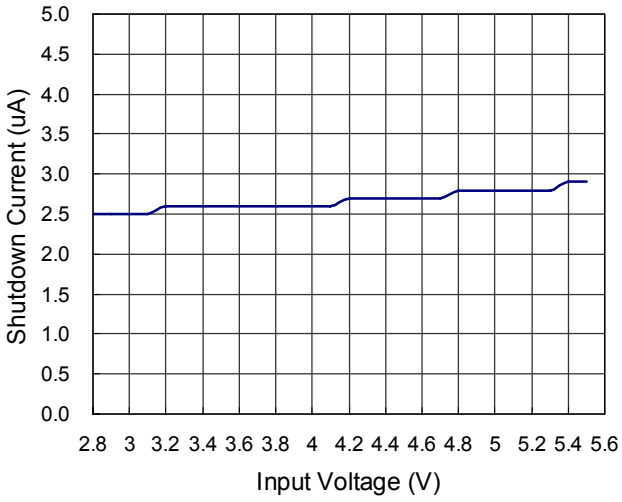




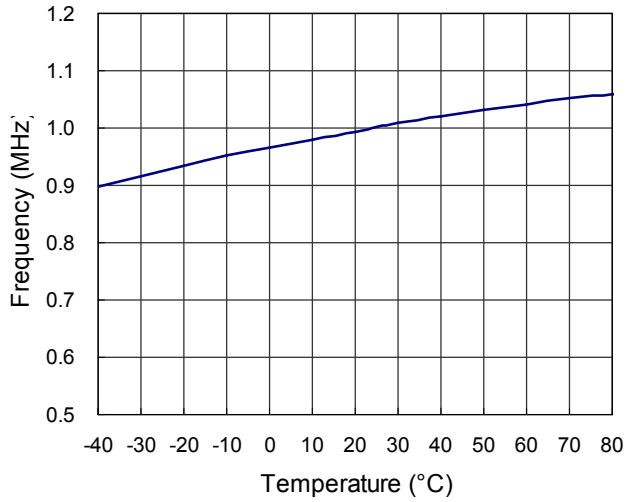




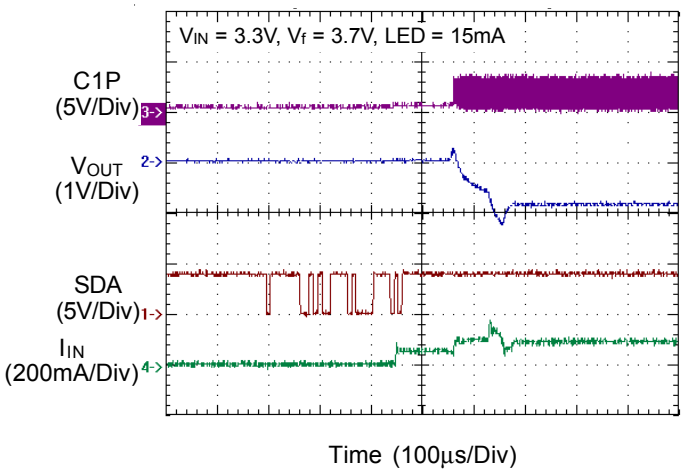
Shutdown Current vs. Input Voltage



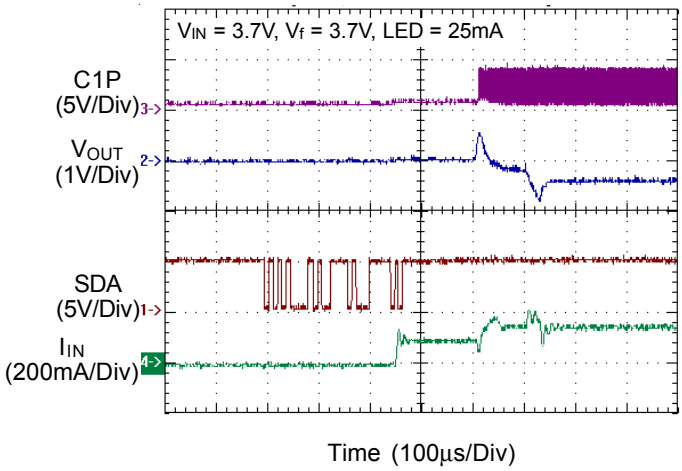
Frequency vs. Temperature



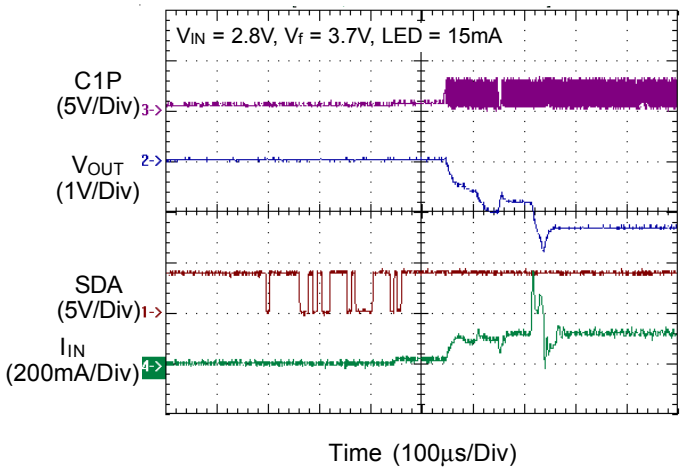
x1.5 Mode Inrush Current Response



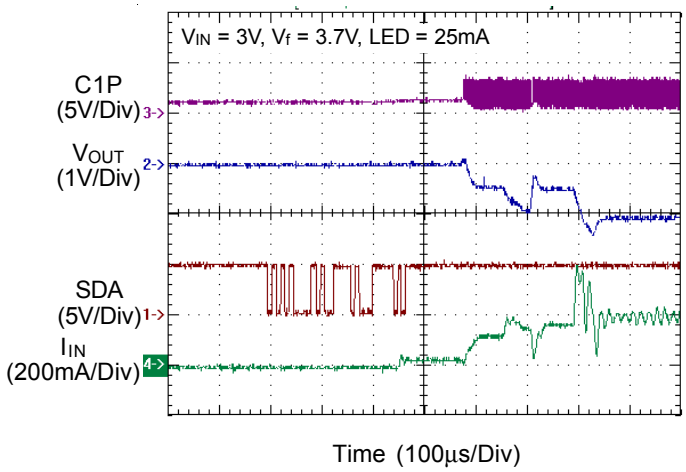
x1.5 Mode Inrush Current Response



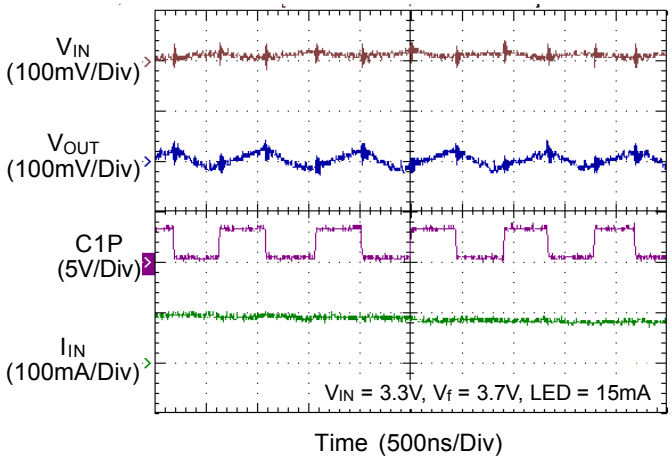
x2 Mode Inrush Current Response



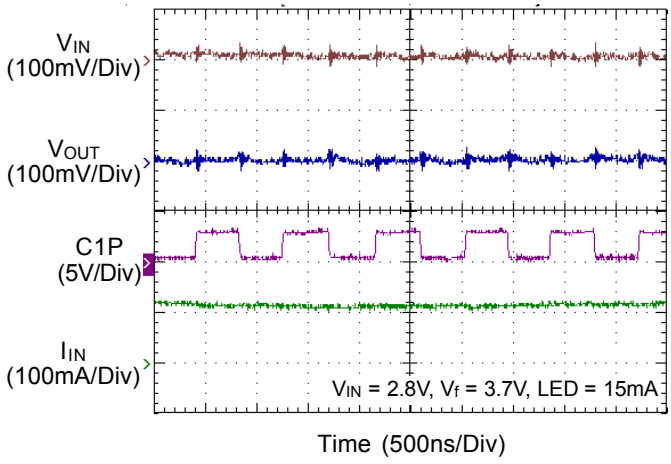
x2 Mode Inrush Current Response



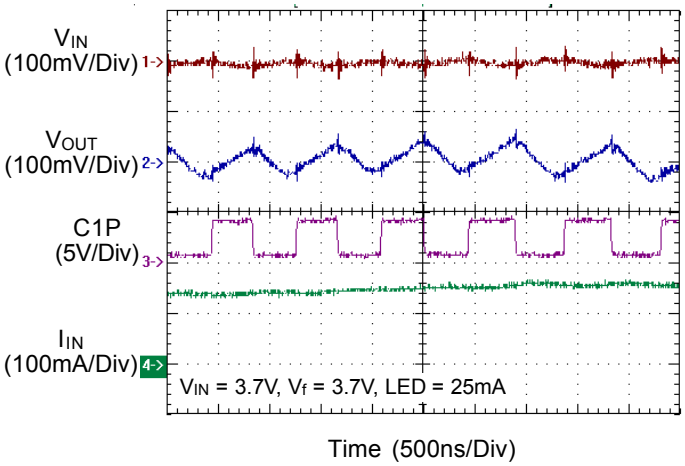
x1.5 Mode Ripple & Spike



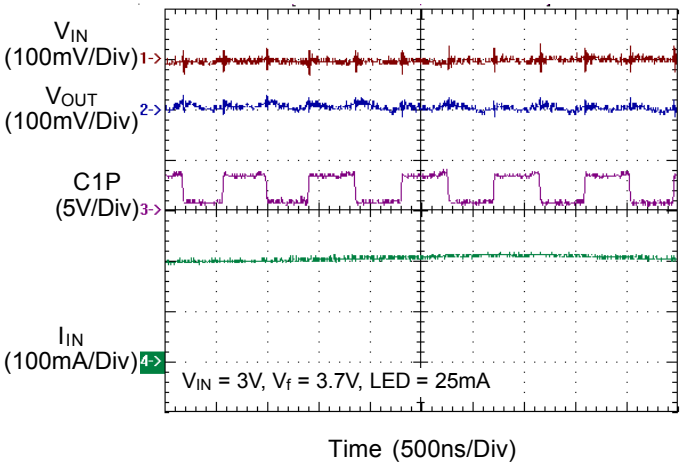
x2 Mode Ripple & Spike



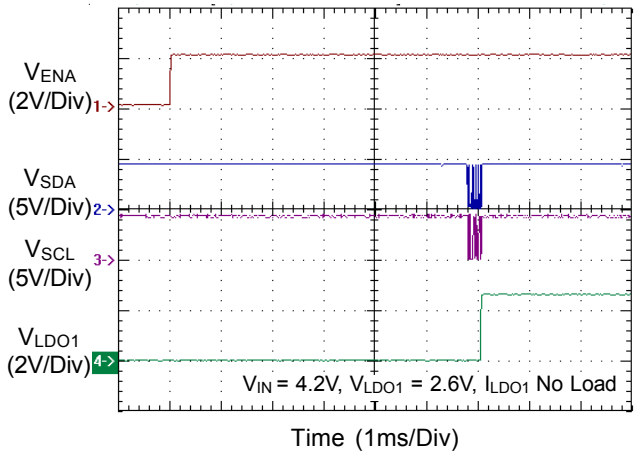
x1.5 Mode Ripple & Spike



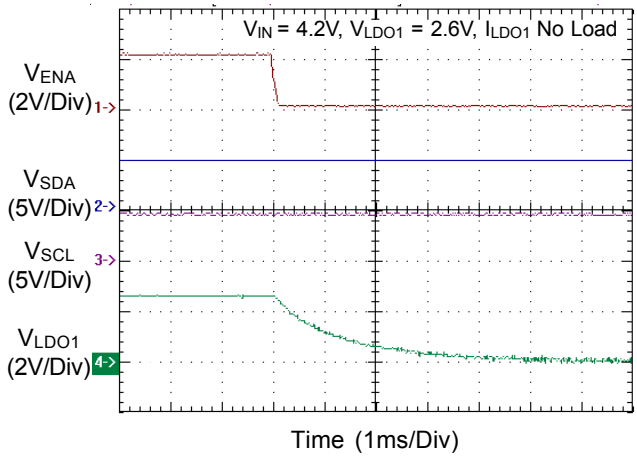
x2 Mode Ripple & Spike



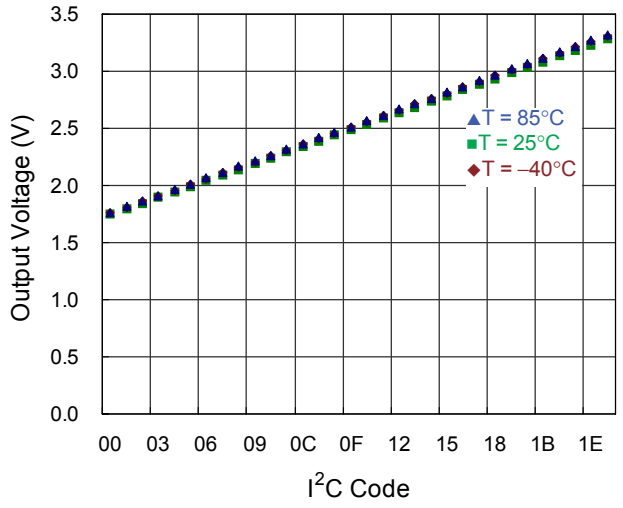
Power On from ENA



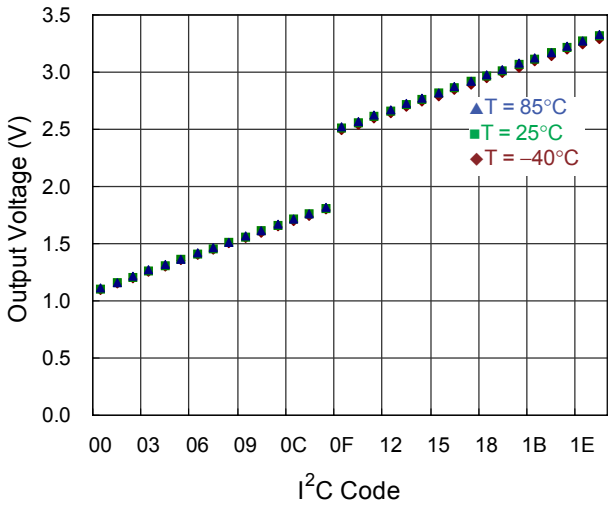
Power Off from ENA



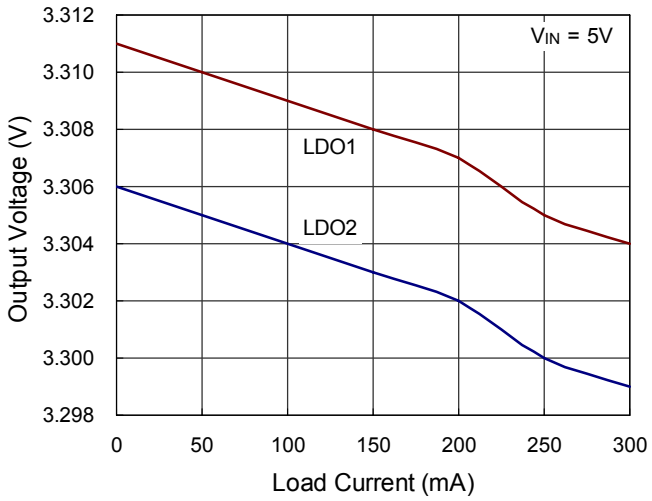
LDO1 Output Voltage vs. I²C Code



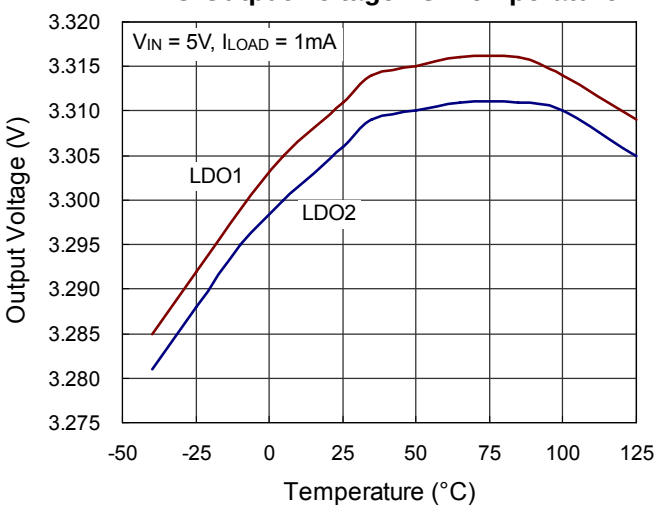
LDO2 Output Voltage vs. I²C Code



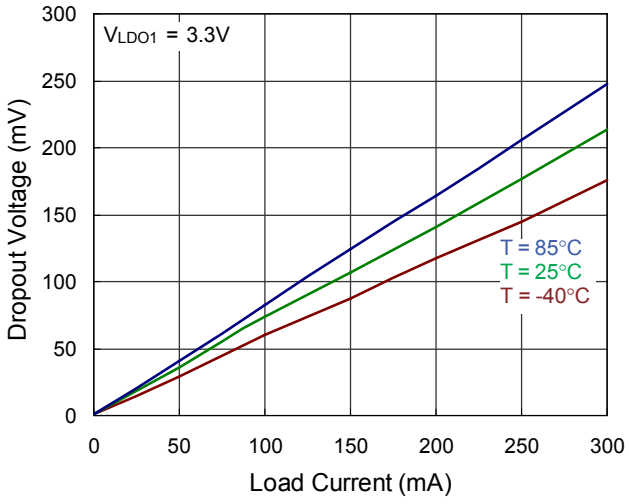
LDO Output Voltage vs. Load Current



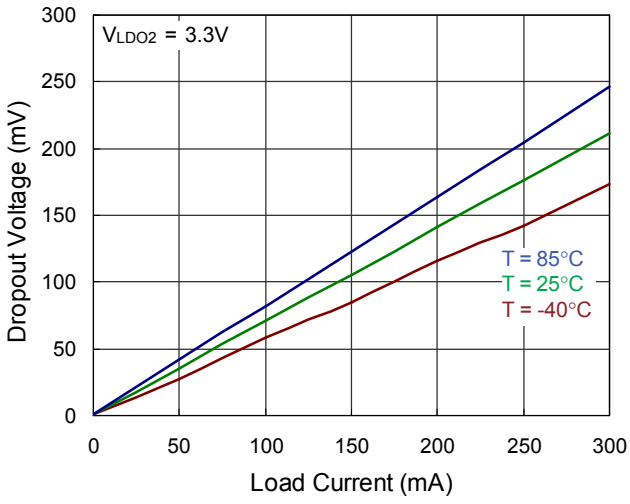
LDO Output Voltage vs. Temperature



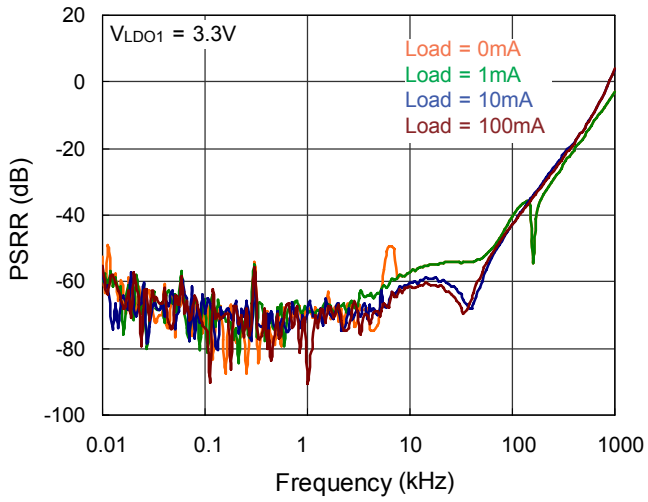
LDO1 Dropout Voltage vs. Load Current



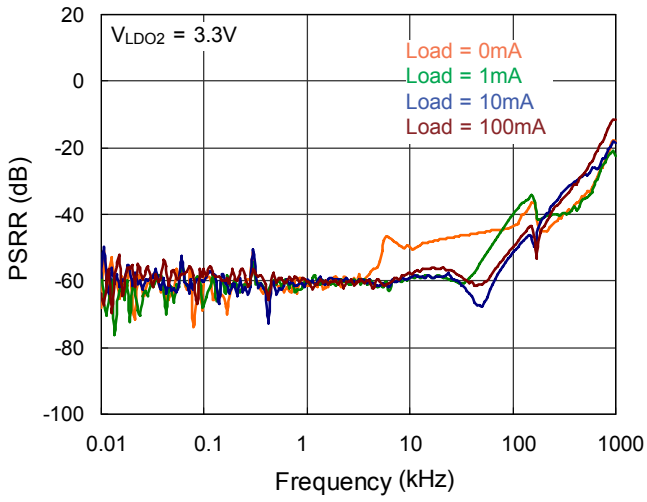
LDO2 Dropout Voltage vs. Load Current



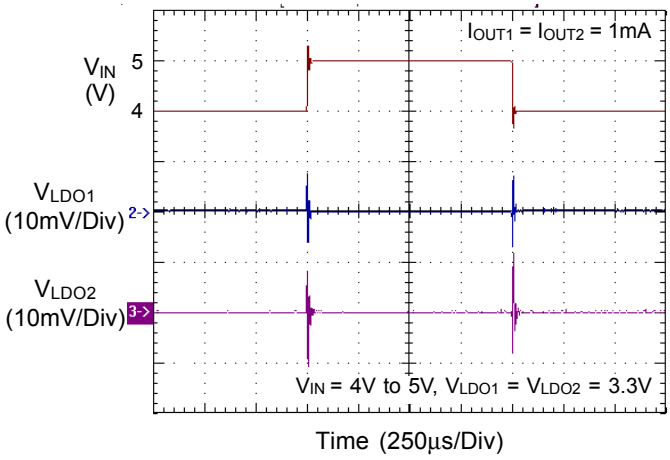
LDO1 PSRR



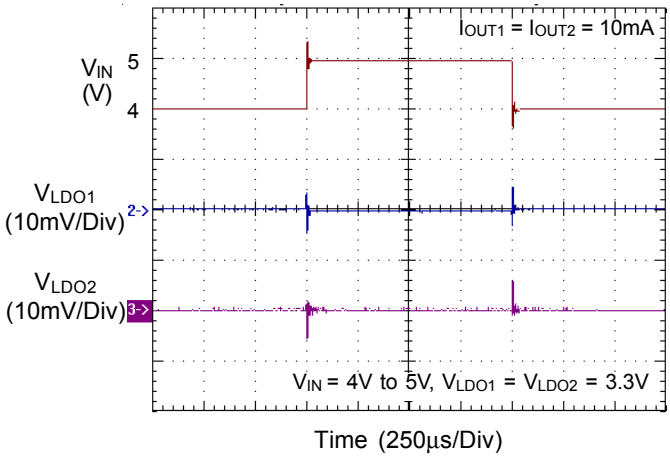
LDO2 PSRR



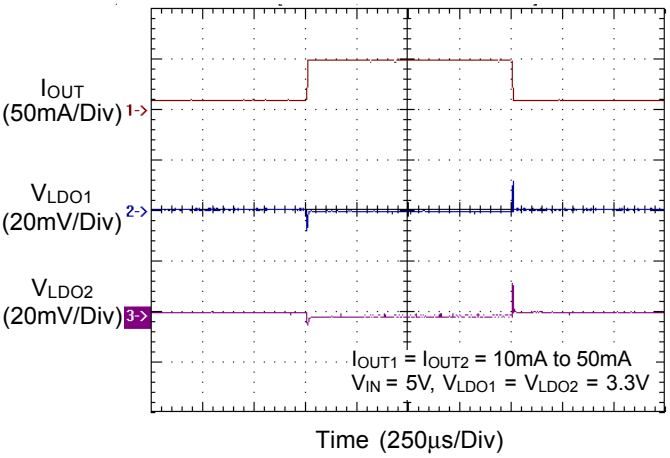
LDO Line Transient Response



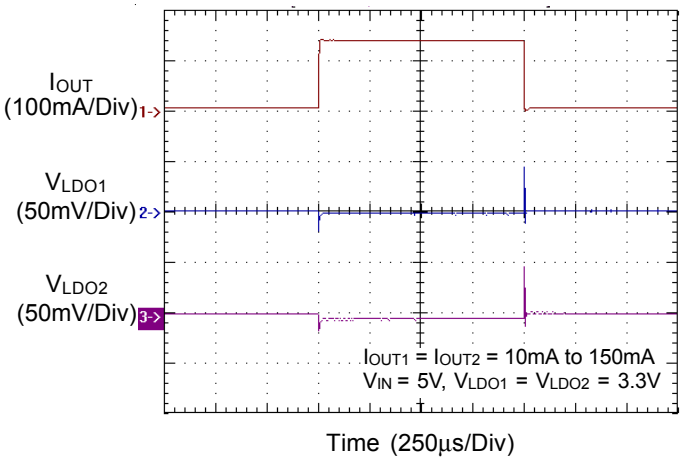
LDO Line Transient Response



LDO Load Transient Response



LDO Load Transient Response



Applications Information

The RT9367C is a high efficiency charge pump white LED driver. It provides 4 channels low dropout voltage current source to regulated 4 white LEDs current. For high efficiency, the RT9367C implements a smart mode transition for charge pump operation. The RT9367C provides I^2C dimming function for LED brightness control.

Input UVLO

The input operating voltage range of the RT9367C is 2.8V to 5.5V. An input capacitor at the VIN pin could reduce ripple voltage. It is recommended to use a ceramic 1uF or larger capacitance as the input capacitor. This IC provides an under voltage lockout (UVLO) function to prevent it from unstable issue when startup. The UVLO threshold of input rising voltage is set at 2V typically with a hysteresis 0.1V.

Soft Start

The RT9367C includes a soft start circuit to limit the inrush current at power on and mode switching. The soft start circuit limits the input current before output voltage reaching a desired voltage level.

Mode Decision

The RT9367C uses a smart mode decision method to select the working mode for maximum efficiency. The charg pump can operation at x1, x1.5 or x2 mode. The mode decision circuit senses the output voltage and LED voltage for up/down selection.

Selecting Capacitors

To get better performance of RT9367C, the selection of peripherally appropriate capacitor and value is very important. These capacitors determine some parameters such as input/output ripple voltage, power efficiency and maximum supply current by charge pump. To reduce the input and output ripple effectively, the low ESR ceramic capacitors are recommended. For LED driver applications, the input voltage ripple is more important than output ripple. The input ripple is controlled by input capacitor C_{IN}, increasing the value of input capacitance can further reduce the ripple. Practically, the input voltage ripple depends on the power supply's impedance. The flying capacitor C_{FLY1} and C_{FLY2} determine the supply current capability of the charge pump that will influence the overall efficiency of the system. The lower value will improve efficiency, but it will limit the LED's current at low input voltage. For 4 X 25mA load over the entire input voltage range of 2.8V to 5.5V, it is recommended to use 1μF ceramic capacitor on the flying capacitor C_{FLY1} & C_{FLY2}.

Power Sequence

In order to assure the RT9367C's operation in normal condition, the Input voltage and ENA should be ready before the RT9367C get the I^2C signal showed in Figure 3 and the RT9367C can be shut down by pulling ENA low. When ENA is reset, the I^2C signal also needs to be resent again for operating at normal condition.

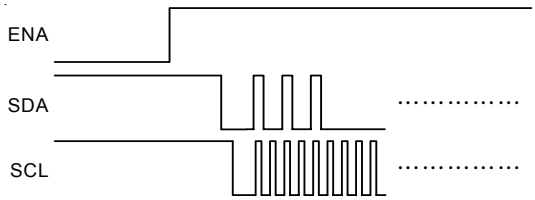


Figure 3. The power sequence

Dual LDO

Like any low-dropout regulator, the external capacitors used with the RT9367C must be carefully selected for regulator stability and performance. Using a capacitor whose value is > 1μF on the RT9367C input and the amount of capacitance can be increased without limit. The input capacitor must be located at a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The RT9367C is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 20mΩ on the RT9367C output ensures stability. The RT9367C still works well with output capacitor of other types due to the wide stable ESR range. Figure 4. shows the curves of allowable ESR range as a function of load current for various

output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located at not more than 0.5 inch from the LDO1 and LDO2 pin of the RT9367C and returned to a clean analog ground.

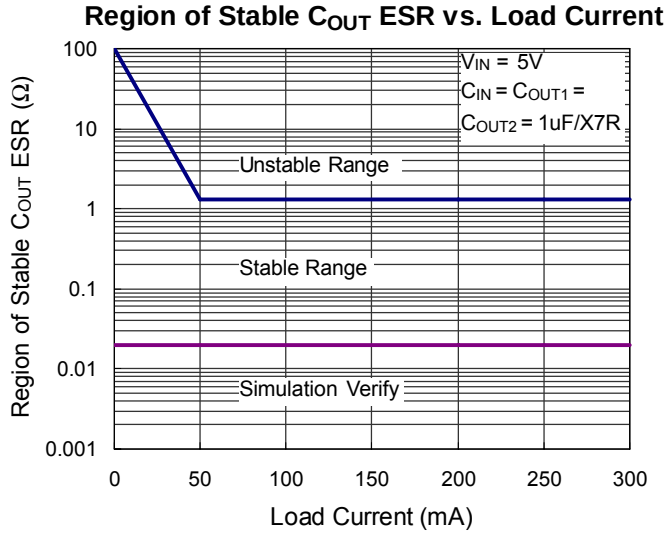


Figure 4. Stable Cout ESR Range

Thermal Protection

Thermal protection limits power dissipation in RT9367C. When the operation junction temperature exceeds 170°C, the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turn on again after the junction temperature cools by 40°C. The RT9367C lowers its OTP trip level from 170°C to 110°C when output short circuit occurs (LDO1 and LDO2 < 0.4V) as shown in Figure 5. It limits IC case temperature under 110°C and provides maximum safety to customer while output short circuit occurring.

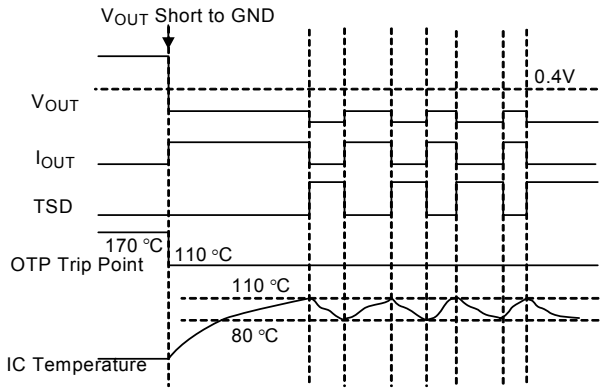


Figure 5. Short Circuit Thermal Folded Back Protection when Output Short Circuit Occurs (Patent)

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification of RT9367C, The maximum junction temperature is 125°C. The junction to ambient thermal resistance θ_{JA} is layout dependent. For WQFN-20L 3x3 packages, the thermal resistance θ_{JA} is 68°C/W on the standard JEDEC 51-7 four layers thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula:

$P_{D(MAX)}$ = (125°C – 25°C) / (68°C/W) = 1.471W for WQFN-20L 3x3 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. For RT9367C packages, the Figure 6 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

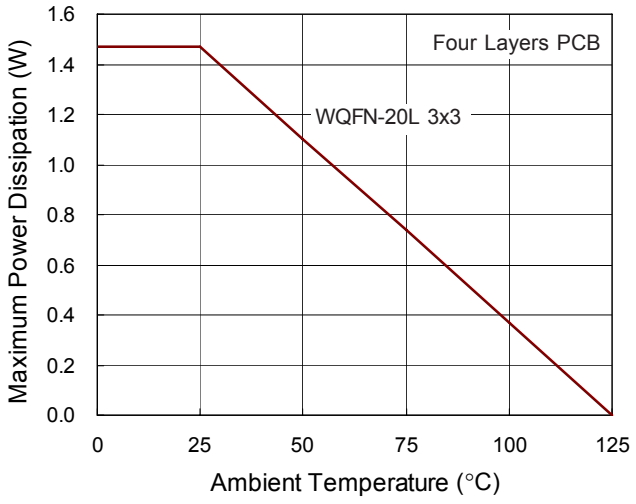


Figure 6. Derating Curves

I²C Compatible Interface

The figure 1 shows the timing diagram of I²C interface. The RT9367C communicates with a host (master) using the standard I²C 2-wire interface. The two bus lines of SCL and SDA must be pulled to high when the bus is not in use. External pull-up resistors between VCC and SDA/SCL pin are necessary. The recommended pull-up resistor value range is from 2kΩ to 10kΩ.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The RT9367C address is 1010100 (54h) and is a receive-only (slave) device. The second word selects the register to which the data will be written. The third word contains data to write to the selected register.

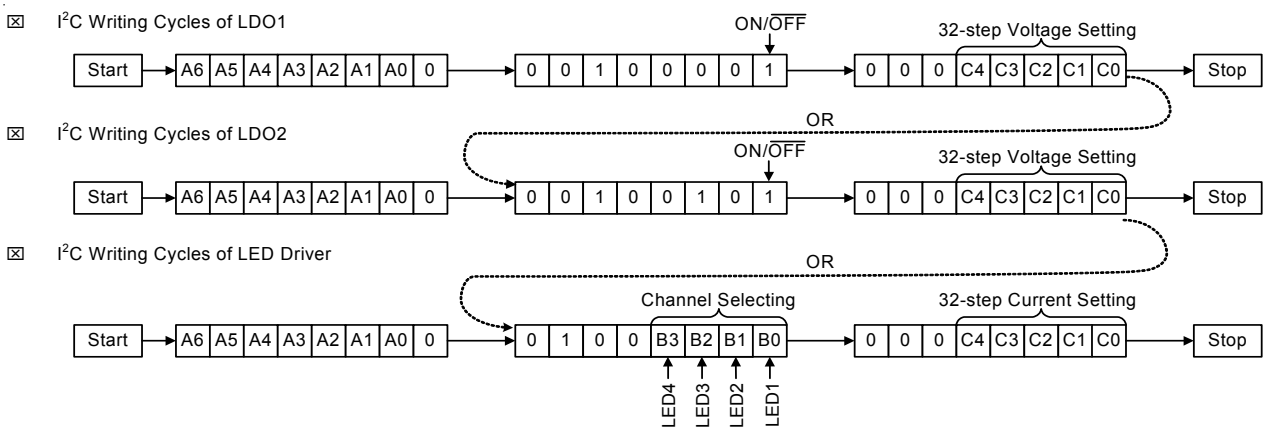


Figure 7. RT9367C I²C Writing Cycles for LDO and LED Driver

Figure 7 shows the writing information of dual LDO and LED current. In the second word, the sub-address of dual LDO is "001" and the sub-address of LED Driver is "010". For LDO, the LDO1 address is defined as "000", LDO2 address is defined as "001".

The data of second byte (B0 to B3), a "0" indicates a DISABLE and a "1" indicates an ENABLE function. The data of third byte (C0 to C4) indicates a 32-steps setting of LDO1, LDO2 output voltage or the LED current of backlight.

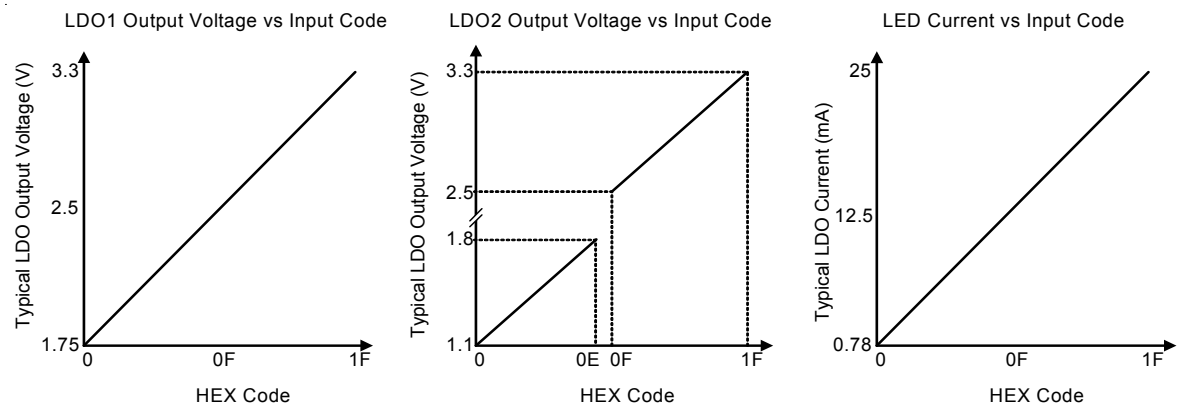


Figure 8. LDO Voltage Setting and LED Current Setting

Table 1. LDO Voltage Setting

Code C4~C0	Voltage (V)		Code C4~C0	Voltage (V)		Code C4~C0	Voltage (V)		Code C4~C0	Voltage (V)	
	LDO1	LDO2		LDO1	LDO2		LDO1	LDO2		LDO1	LDO2
00000	1.75	1.10	01000	2.15	1.50	10000	2.55	2.55	11000	2.95	2.95
00001	1.80	1.15	01001	2.20	1.55	10001	2.60	2.60	11001	3.00	3.00
00010	1.85	1.20	01010	2.25	1.60	10010	2.65	2.65	11010	3.05	3.05
00011	1.90	1.25	01011	2.30	1.65	10011	2.70	2.70	11011	3.10	3.10
00100	1.95	1.30	01100	2.35	1.70	10100	2.75	2.75	11100	3.15	3.15
00101	2.00	1.35	01101	2.40	1.75	10101	2.80	2.80	11101	3.20	3.20
00110	2.05	1.40	01110	2.45	1.80	10110	2.85	2.85	11110	3.25	3.25
00111	2.10	1.45	01111	2.50	2.50	10111	2.90	2.90	11111	3.30	3.30

Table 2. LDO Current Setting

Code C4~C0	LED Current (mA)	Code C4~C0	LED Current (mA)	Code C4~C0	LED Current (mA)	Code C4~C0	LED Current (mA)
00000	0.8	01000	7.0	10000	13.3	11000	19.5
00001	1.6	01001	7.8	10001	14.0	11001	20.3
00010	2.3	01010	8.6	10010	14.8	11010	21.1
00011	3.1	01011	9.4	10011	15.6	11011	21.8
00100	3.9	01100	10.1	10100	16.4	11100	22..6
00101	4.7	01101	10.9	10101	17.2	11101	23.4
00110	5.5	01110	11.7	10110	17.9	11110	24.2
00111	6.2	01111	12.5	10111	18.7	11111	25.0

Figure 8. illustrates the dual LDOs' output voltage and LED current setting information. The output voltage of LDO1 could be divided to 32-step levels between 1.75V (HEX Code = 0) and 3.3V (HEX Code = 1F). And the output voltage of LDO2 is separated to two regions, one is from 1.1V (HEX Code = 0) to 1.8V (HEX Code = 0E) and the other is from 2.5V (HEX Code = 0F) to 3.3V (HEX Code = 1F). In addition, the LED current could be divided to 32-step levels between 0.8mA (HEX Code = 0) and 25mA (HEX Code = 1F).

Layout Consideration

The RT9367C is a high-frequency switched-capacitor converter. Careful PCB layout is necessary. For best performance, place all peripheral components as close to the IC as possible. Place C_{IN1}, C_{IN2}, C_{OUT}, C_{LDO1}, C_{LDO2}, C_{FLY1}, and C_{FLY2} near to AVIN, PVIN, VOUT, LDO1, LDO2, C1P, C1N, C2P, C2N, and GND pin respectively. A short connection is highly recommended. The following guidelines should be strictly followed when designing a PCB layout for the RT9367C.

- The exposed GND pad must be soldered to a large ground plane for heat sinking and noise prevention. The throughhole vias located at the exposed pad is connected to ground plane of internal layer.
- VIN traces should be wide enough to minimize inductance and handle the high currents. The trace running from battery to chip should be placed carefully and shielded strictly.
- Input and output capacitors must be placed close to the part. The connection between pins and capacitor pads should be copper traces without any through-hole via connection.

- The flying capacitors must be placed close to the part. The traces running from the pins to the capacitor pads should be as wide as possible. Long traces will also produce large noise radiation caused by the large dv/dt on these pins. Short trace is recommended.
- All the traces of LED and VIN running from pins to LCM module should be shielded and isolated by ground plane. The shielding prevents the interference of high frequency noise coupled from the charge pump.
- Output capacitor must be placed between VNG and VOUT to reduce noise coupling from charge pump to LEDs.

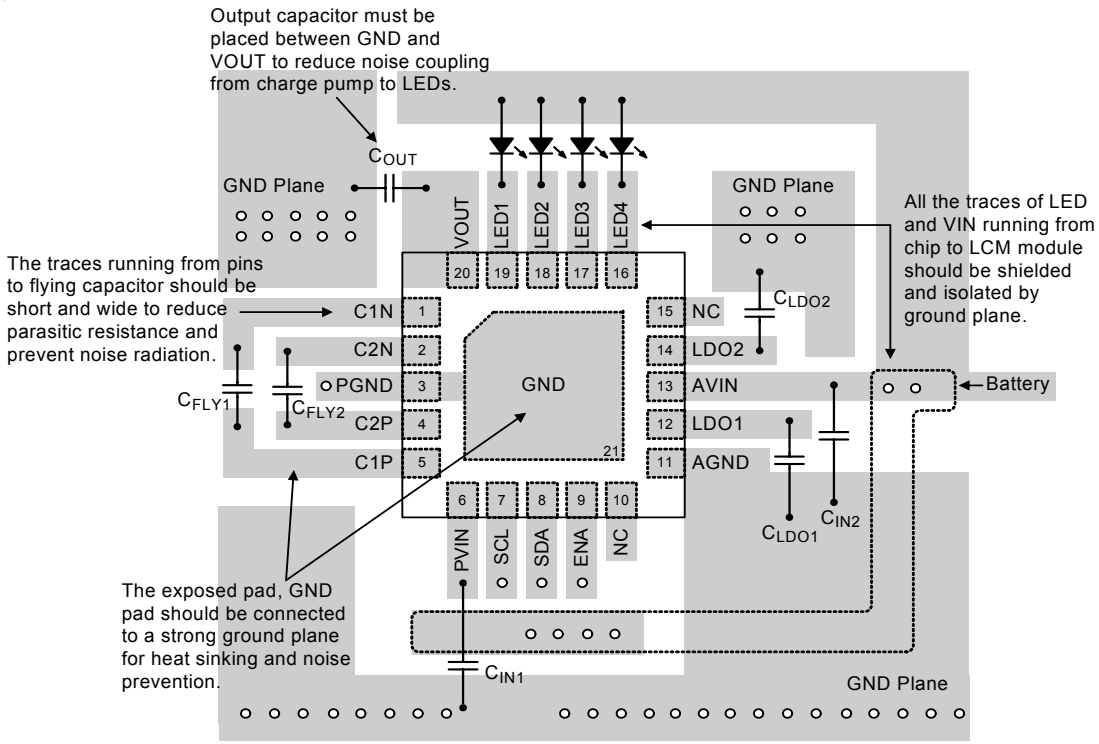
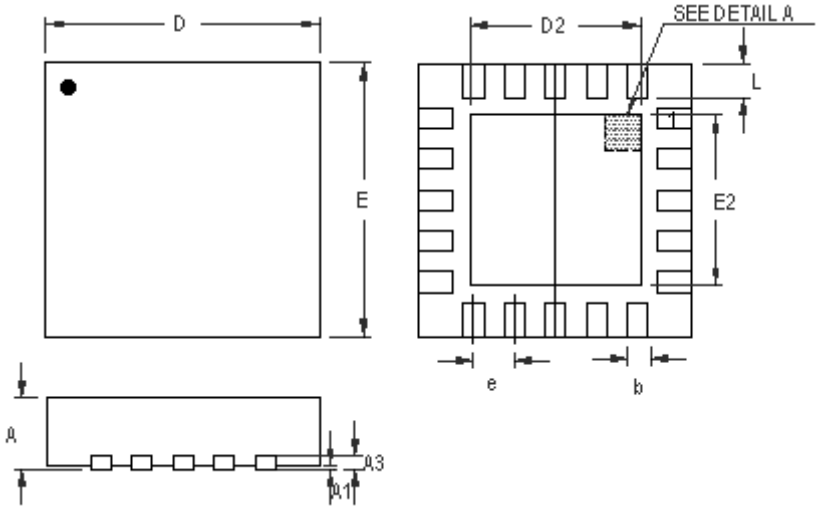
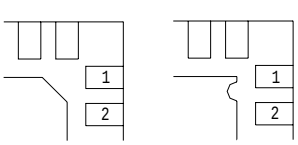


Figure 9. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.150	0.250	0.006	0.010
D	2.900	3.100	0.114	0.122
D2	1.650	1.750	0.065	0.069
E	2.900	3.100	0.114	0.122
E2	1.650	1.750	0.065	0.069
e	0.400		0.016	
L	0.350	0.450	0.014	0.018

W-Type 20L QFN 3x3 Package

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