Multi-Phase PWM Controller for CPU Core Power Supply

General Description

The RT9246A is a multi-phase buck DC/DC controller integrated with all control functions for GHz CPU VRM. The RT9246A controls 2 or 3 buck switching stages operating in interleaved phase set automatically. The multi-phase architecture provides high output current while maintaining low power dissipation on power devices and low stress on input and output capacitors. The high equivalent operating frequency also reduces the component dimension and the output voltage ripple in load transient.

RT9246A controls both voltage and current loops to achieve good regulation, response & power stage thermal balance. Precise current loop using Inductor DCR as sense component builds precise load line for strict VRM DC & transient specification and also ensures thermal balance of different power stages. The settings of current sense, droop tuning, V_{CORE} initial offset and over current protection are independent to compensation circuit of voltage loop. The feature greatly facilitates the flexibility of CPU power supply design and tuning.

The DAC output of RT9246A supports K8 CPU by 5-bit VID input, precise initial value & smooth V_{CORE} transient at VID jump. The IC monitors the V_{CORE} voltage for PGOOD and over-voltage protection. Soft-start, over-current protection and programmable under-voltage lockout are also provided to assure the safety of microprocessor and power system.

Ordering Information

RT9246A □ □

- Package Type
  C : TSSOP-28
- Operating Temperature Range
  P : Pb Free with Commercial Standard
  G : Green (Halogen Free with Commercial Standard)

Note :

RichTek Pb-free and Green products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.
- 100% matte tin (Sn) plating.

Features

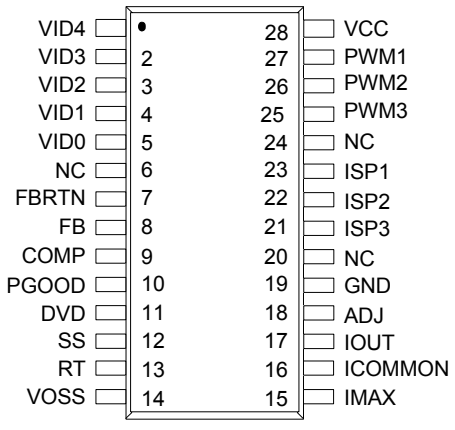
- **Multi-Phase Power Conversion with Automatic Phase Selection**
- **K8 DAC Output with Active Droop Compensation for Fast Load Transient**
- **Smooth V_{CORE} Transition at VID Jump**
- **Power Stage Thermal Balance by Inductor DCR Current Sense**
- **Hiccup Mode Over-Current Protection**
- **Programmable Switching Frequency (50kHz to 400kHz per Phase), Under-Voltage Lockout and Soft-Start**
- **High Ripple Frequency Times Channel Number**
- **RoHS Compliant and 100% Lead (Pb)-Free**

Applications

- AMD® Athlon™ 64 and Opteron™ Processors Voltage Regulator
- Low Output Voltage, High Current DC-DC Converters
- Voltage Regulator Modules

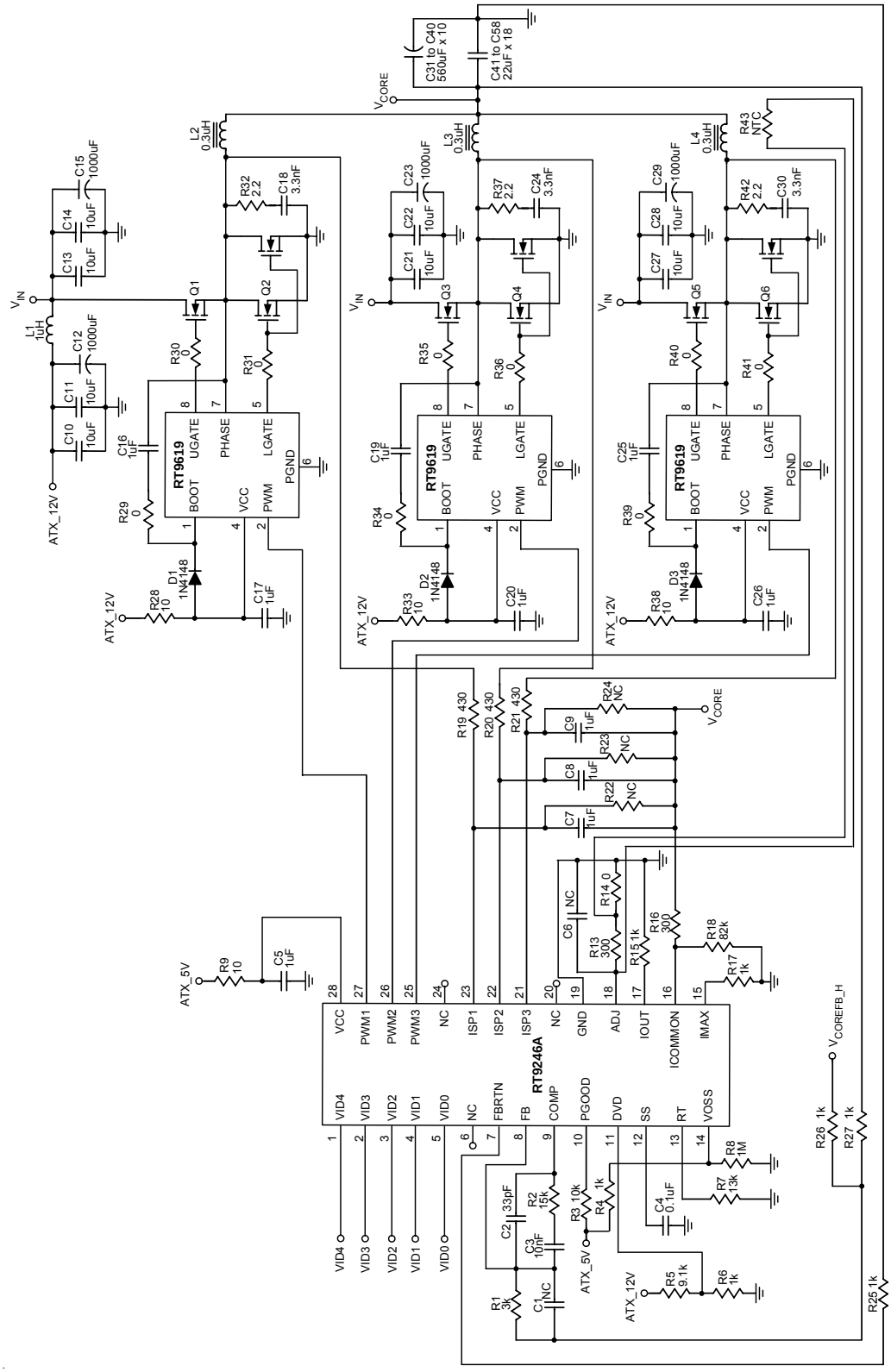
Pin Configurations

(TOP VIEW)



TSSOP-28

Typical Application Circuit



Functional Pin Description

VID4 (Pin 1), VID3 (Pin 2), VID2 (Pin 3), VID1 (Pin 4), VID0 (Pin 5)

DAC voltage identification inputs for K8. These pins are internally pulled to 2.2V if left open.

NC (Pin 6, Pin 20, Pin 24)

No Input Connection

FBRTN (Pin 7)

V_{CORE} differential sense return.

FB (Pin 8)

Inverting input of the internal error amplifier.

COMP (Pin 9)

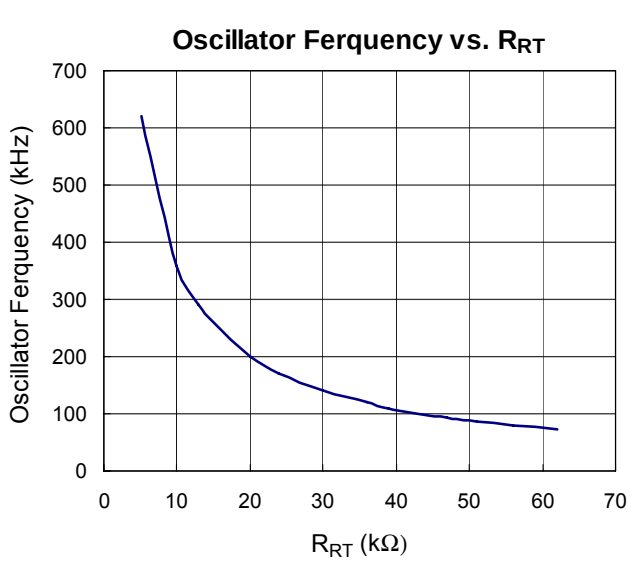
Output of the error amplifier and input of the PWM comparator.

PGOOD (Pin 10)

Power good open-drain output.

DVD (Pin 11)

Programmable power UVLO detection or converter enable input.



SS (Pin 12)

Connect this SS pin to GND with a capacitor to set the soft-start time interval and to smooth V_{CORE} transient at VID Jump.

RT (Pin 13)

Switching frequency setting. Connect this pin to GND with a resistor to set the frequency.

VOSS (Pin 14)

V_{CORE} initial value offset. Connect this pin to GND with a resistor to set the offset value.

IMAX (Pin 15)

Over-Current protection set.

ICOMMON (Pin 16)

Common negative input of current sense amplifiers for all three channels.

IOUT (Pin 17)

Output current indication pin. The current through IOUT pin is proportional to the output current.

ADJ (Pin 18)

Current sense output for active droop adjust. Connect a resistor from this pin to GND to set the load droop.

GND (Pin 19)

IC ground.

ISP1 (Pin 23), ISP2 (Pin 22), ISP3 (Pin 21)

Current sense positive input pins for individual converter channel current sensing.

PWM1 (Pin 27), PWM2 (Pin 26), PWM3 (Pin 25)

PWM outputs for each driven channel. Connect these pins to the PWM input of the MOSFET driver. For systems which use 2 channels, connect PWM3 high.

VCC (Pin 28)

IC power supply. Connect this pin to a 5V supply.

Function Block Diagram

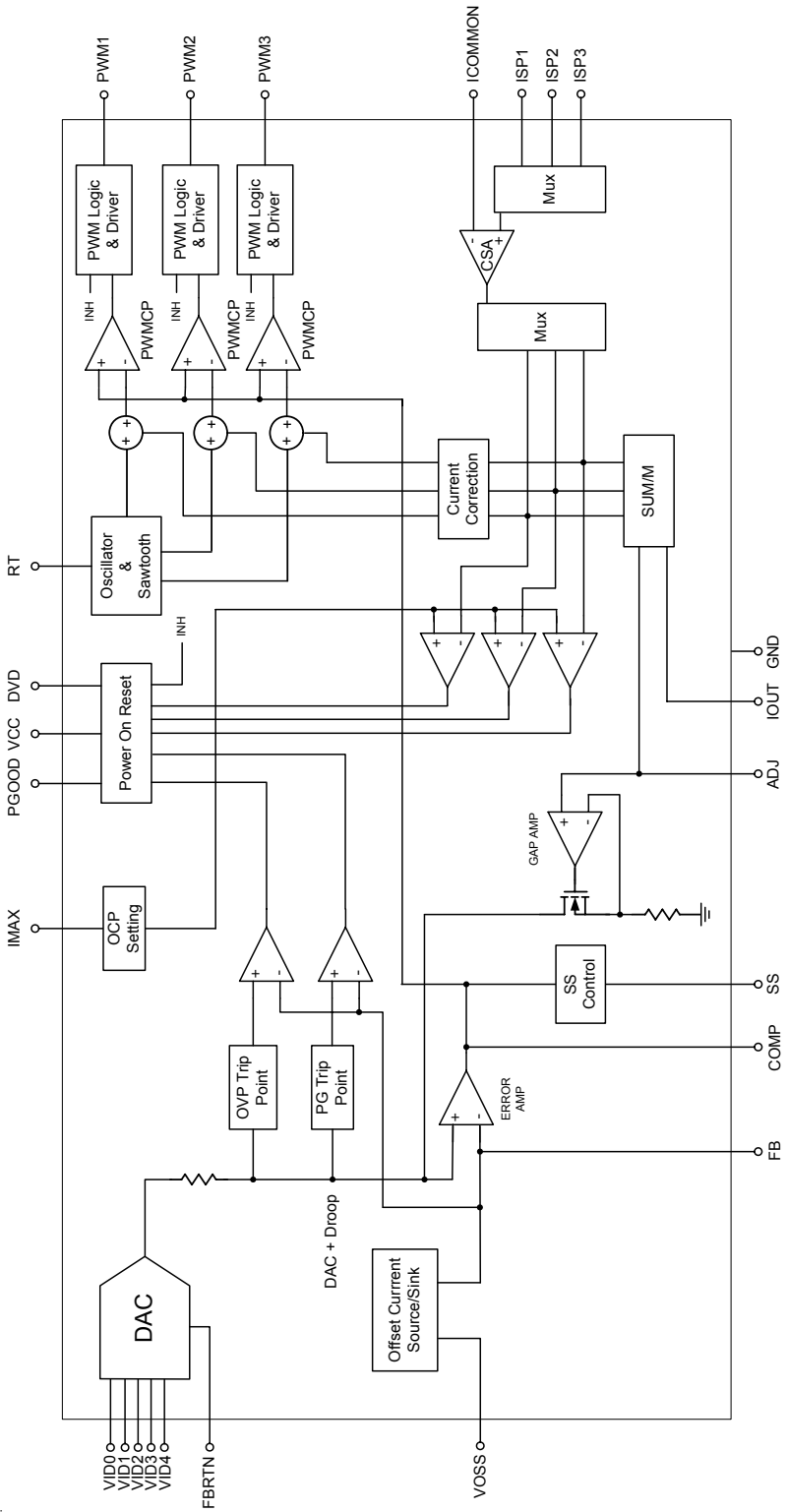


Table 1. Output Voltage Program

VID4	VID3	VID2	VID1	VID0	Nominal Output Voltage DACOUT
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.200
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

Note: (1) 0 : Connected to GND
(2) 1 : Open

Absolute Maximum Ratings (Note 1)

- Supply Voltage, V_{CC} ---------- 7V
- Input, Output or I/O Voltage ---------- GND-0.3V to V_{CC}+0.3V
- Power Dissipation, P_D @ T_A = 25°C
  TSSOP-28 ---------- 1W
- Package Thermal Resistance (Note 4)
  TSSOP-28, θ_{JA} ---------- 100°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 2)
  HBM (Human Body Mode) ---------- 2kV
  MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 3)

- Supply Voltage, V_{CC} ---------- 5V ± 10%
- Ambient Temperature Range ---------- 0°C to 70°C
- Junction Temperature Range ---------- 0°C to 125°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
V_{CC} Supply Current							
Nominal Supply Current		I_{CC}	PWM 1,2,3 Open	--	12	--	mA
Power-On Reset							
POR Threshold		V_{CCRTH}	V_{CC} Rising	4.0	4.2	4.5	V
Hysteresis		V_{CCHYS}		0.2	0.5	--	V
V_{DVD} Threshold	Input High	V_{DVDTH}	Enable	0.9	1.0	1.1	V
	Input Low	V_{DVDHYS}		--	60	--	mV
Oscillator							
Free Running Frequency		f_{OSC}	R_{RT} = 20kΩ	170	200	230	kHz
Frequency Adjustable Range		f_{OSC_ADJ}		50	--	400	kHz
Ramp Amplitude		ΔV_{OSC}	R_{RT} = 20kΩ	--	1.9	--	V
Ramp Valley		V_{RV}		--	1.0	--	V
Maximum On-Time of Each Channel				62	66	75	%
RT Pin Voltage		V_{RT}	R_{RT} = 20kΩ	0.9	1.0	1.1	V
Reference and DAC							
DACOUT Voltage Accuracy		ΔV_{DAC}	$V_{DAC} \geq 1V$	–1	--	+1	%
			$V_{DAC} < 1V$	–10	--	+10	mV
DAC (VID0-VID4) Input Low		ΔV_{ILDAC}		--	--	0.8	V
DAC (VID0-VID4) Input High		ΔV_{IHDAC}		1.2	--	--	V

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DAC (VID0-VID4) Pull-up Voltage			2.0	2.2	2.4	V
DAC (VID0-VID4) Pull-up Resistance			10	13	16	kΩ
VOSS Pin Voltage	V_{VOSS}	R_{VOSS} = 100kΩ	0.9	1.0	1.1	V
Error Amplifier						
DC Gain			--	65	--	dB
Gain-Bandwidth Product	GBW		--	10	--	MHz
Slew Rate	SR	C_{COMP} = 10pF	--	8	--	V/μs
Current Sense GM Amplifier						
ICOMMON Full Scale Source Current			100	--	--	μA
ICOMMON Current for OCP			150	--	--	μA
Protection						
IMAX Voltage	V_{IMAX}	R_{IMAX} = 10k	0.84	0.94	1.05	V
Over-Voltage Trip (V_{FB}- V_{DAC})	Δ_{OVT}	R_{ADJ} = 0	340	400	450	mV
Power Good						
Output Low Voltage	V_{PGOODL}	I_{PGOOD} = 4mA	--	--	0.2	V

Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

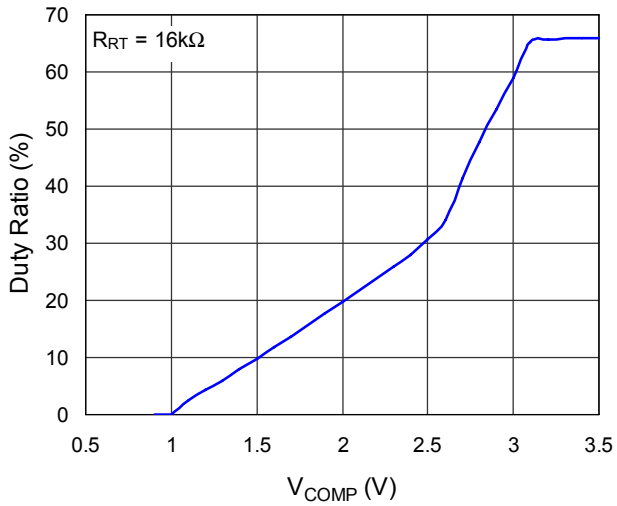
Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. The device is not guaranteed to function outside its operating conditions.

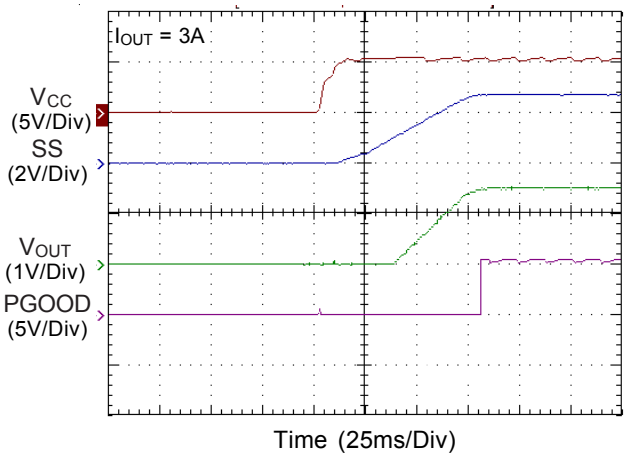
Note 4. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Typical Operating Characteristics

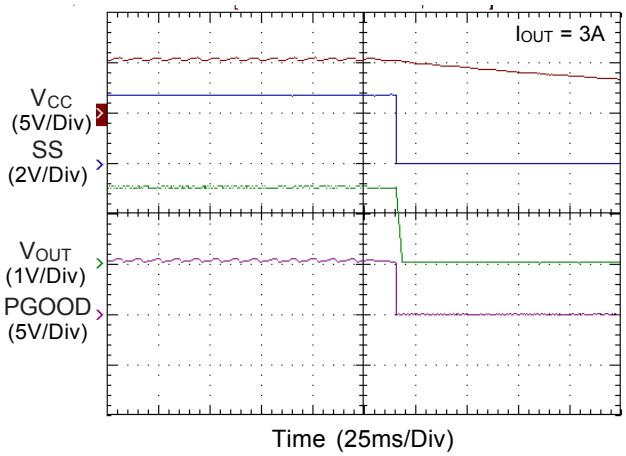
Duty Ratio vs. V_{COMP}



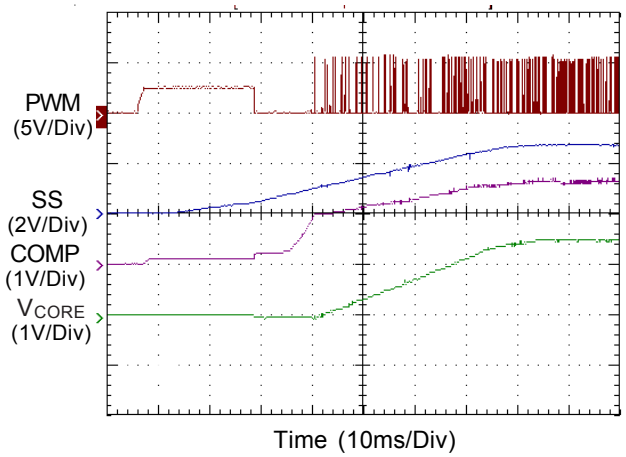
Power On



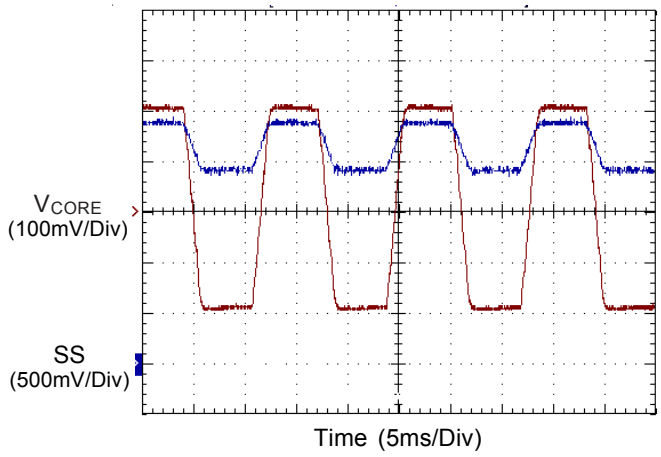
Power Off



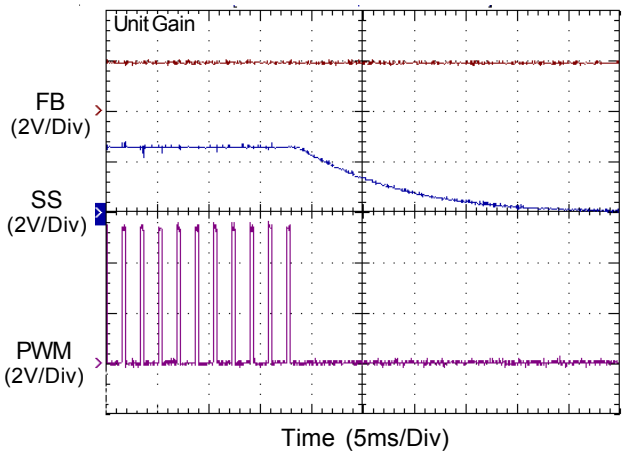
Start Up



VID Jump



OVP



Applications Information

RT9246A is a multi-phase DC/DC controller specifically designed to deliver high quality power for next generation CPU. Phase currents are sensed by innovative time-sharing DCR current sensing technique for channel current balance, droop tuning, and over current protection. Using one common GM amplifier for current sensing eliminates offset errors and linearity variation between GMs. As sub-milli-ohm-grade inductors are widely used in modern mother boards, slight mismatch of GM amplifiers offset and linearity results in considerable current shift between phases. The time-sharing DCR current sensing technique is extremely important to guarantee phase current balance at mass production.

Converter Initialization, Phase Selection, and Power Good Function

The RT9246A initiates only after two pins are ready: VCC pin power on reset (POR) and DVD pin is higher than 1V. VCC POR is to make sure RT9246A is powered by a voltage for normal work. The rising threshold voltage of VCC POR is 4.2V typically. At VCC POR, RT9246A checks PWM3 status to determine phase number of operation. Pull high PWM3 for two-phase operation. The unused current sense pin should be connected to GND or left floating.

DVD is to make sure that ATX12V is ready for companion MOSFET drivers(RT960X series) to work normally. Connect a voltage divider from ATX12V to DVD pin as shown in the Typical Application Circuit. Make sure that DVD pin voltage is below its threshold voltage before drivers are ready and above its threshold voltage for minimum ATX12V during normal operation.

If either one of VCC and DVD is not ready, RT9246A keeps its PWM outputs high impedance and the companion drivers turn off both upper and lower MOSFETs. After VCC and DVD are ready, RT9246A initiates its soft start cycle as shown in Figure 1. A time-variant internal current source charges the capacitor connected to SS pin. SS voltage ramps up piecewise linearly and locks VID_DAC output with a specified voltage drop. Consequently, V_{CORE} is built up according to VID_DAC output. PGOOD output is tripped to high impedance when V_{CORE} reaches VID_DAC output with 1~2ms delay. An SS capacitor about 47nF is recommend for typical application.

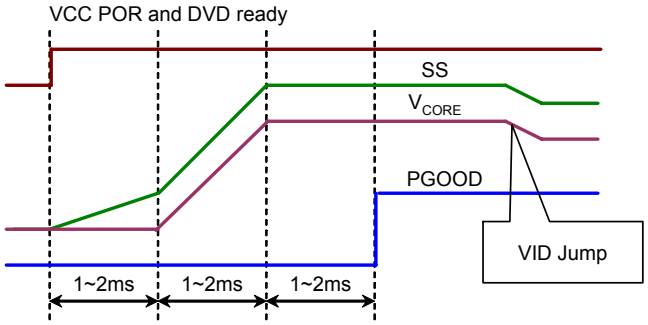


Figure 1. Timming Diagram During Soft Start Interval

Voltage Control

CPU V_{CORE} voltage is Kelvin sensed by FB and FBRTN pins and precisely regulated to VID_DAC output by internal high gain Error Amplifier (EA). The sensed signal is also used for power good and over voltage function. The typical OVP trip point is 400mV above VID_DAC output. RT9246A pulls PWM outputs low and latches up upon OVP trip to prevent CPU from damaging. It can only restart by resetting either VCC or DVD pin.

The VID pins are internally pulled high to internal 2.2V with 13kΩ resistors and are easily interfaced with CPU VID outputs. The change of VID_DAC output at VID Jump is also smoothed by capacitor connected to SS pin. Consequently, V_{CORE} shifts to its new position smoothly.

DCR Current Sensing

RT9246A adopts an innovative time-sharing DCR current sensing technique to sense the phase currents for phase current balance (phase thermal balance) and load line regulation as shown in Figure 2. Current sensing amplifier GM samples and holds voltages V_X across the current sensing capacitor C_X by turns in a switching cycle. According to the Basic Circuit Theory, if

$$\frac{L_X}{R_{LX}} = R_X \times C_X \text{ then } V_X = I_{LX} \times R_{LX}$$

Consequently, the sensing current I_X is proportional to inductor current I_{LX} and is expressed as :

$$I_X = \frac{I_{LX} \times R_{LX}}{R_{COMM}}$$

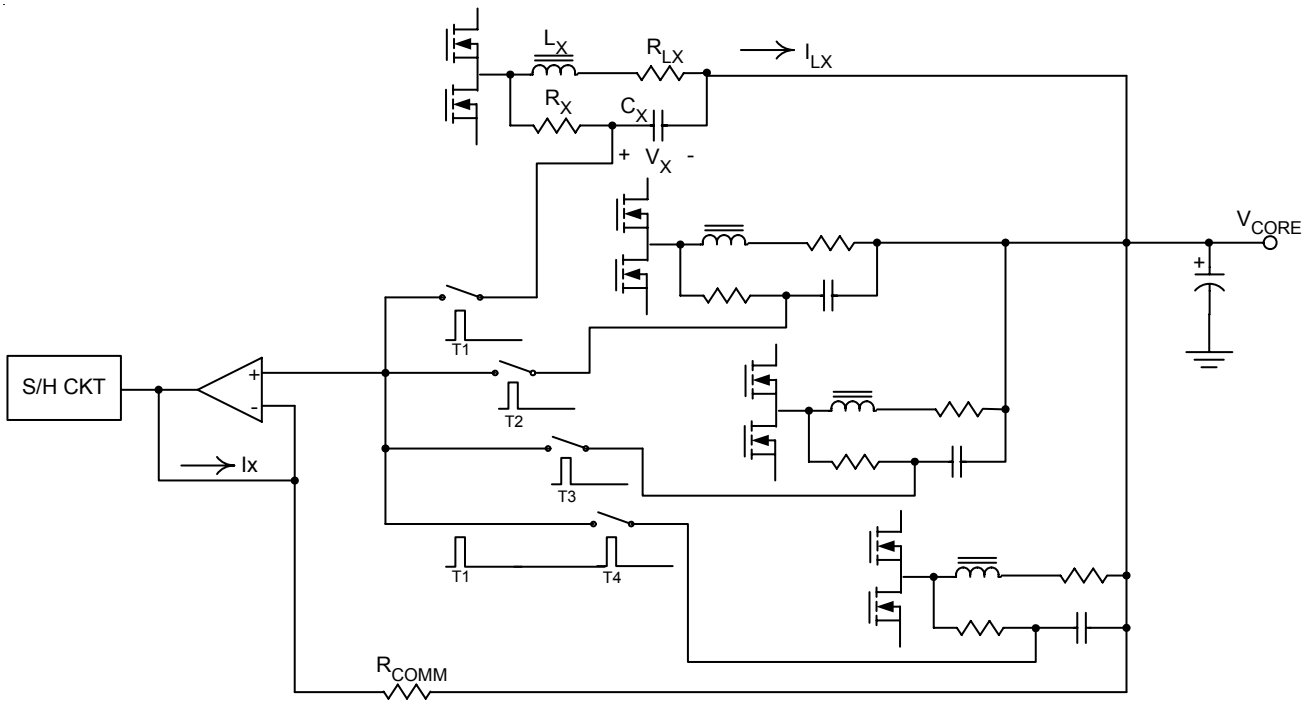


Figure 2

The sensed current I_X is used for current balance and droop tuning as described as followed. Since all phases share one common GM, GM offset and linearity variation effect is eliminated in practical applications. As sub-milli-ohm-grade inductors are widely used in modern mother boards, slight mismatch of GM amplifiers offset and linearity results in considerable current shift between phases. The time-sharing DCR current sensing technical is extremely important to guarantee phase current balance at mass production.

Phase Current Balance

The sampled and held phase current I_X are summed and averaged to get the averaged current $\overline{I_X}$. Each phase current I_X then is compared with the averaged current. The difference between I_X and $\overline{I_X}$ is injected to corresponding PWM comparator. If phase current I_X is smaller than the averaged current , RT9246A increases the duty cycle of corresponding phase to increase the phase current accordingly, vice versa.

Over Current Protection

RT9246A uses an external resistor R_{IMAX} connected to IMAX pin to generate a reference current I_{IMAX} for over current protection:

$$I_{IMAX}=\frac{V_{IMAX}}{R_{IMAX}}$$

where V_{IMAX} is 1.0V typical. OCP comparator compares each sensed phase current I_X with this reference current as shown in Figure 3. Equivalently, the maximum phase current is calculated as:

$$I_{LX(MAX)}=\frac{3}{2}\frac{V_{IMAX}}{R_{IMAX}}\frac{R_{COMM}}{R_{LX}}$$

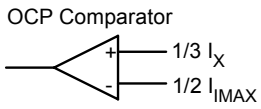


Figure 3. Over Current Comparator

RT9246A uses hiccup mode to eliminate nuisance detection of OCP or reduce output current when output is shorted to ground as shown in Figure 4 and 5.

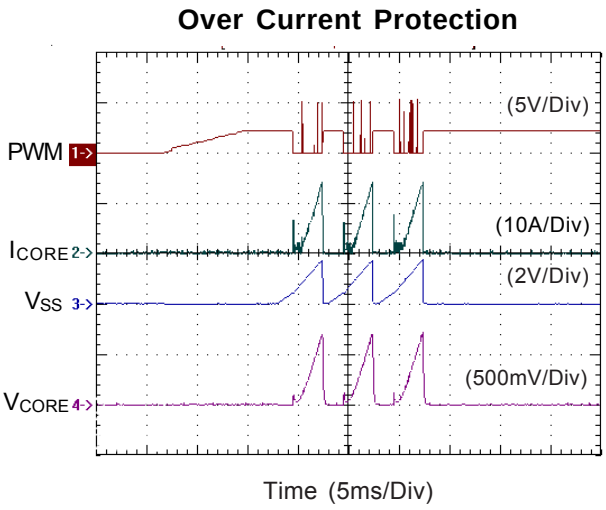


Figure 4. The Over Current Protection in the soft start interval

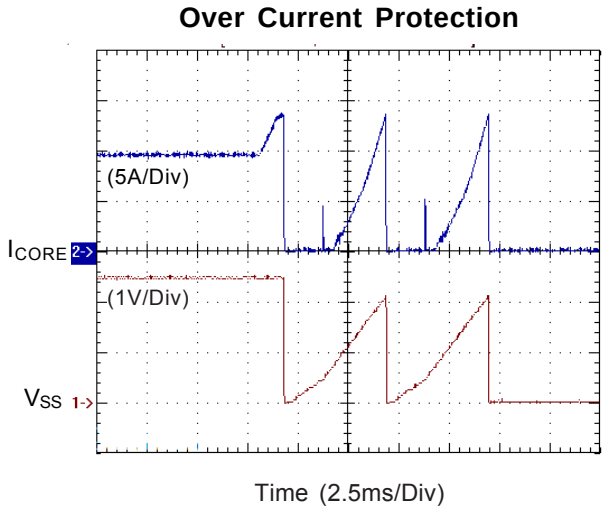


Figure 5. Over Current Protection at steady state

Droop and Load Line Setting

RT9246A injects averaged phase current $\overline{I_X}$ into the resistor R_{ADJ} connected to ADJ pin to generate a load-current-dependent voltage V_{ADJ} for droop setting:

$$V_{ADJ} = 8\overline{I_X} R_{ADJ}$$

V_{ADJ} is then subtracted form VID_DAC output as the real reference voltage at non-inverting input of the error amplifier as shown if Figure 6. Consequently, load line slope is calculated as:

$$\text{Load Line} = \frac{\Delta V_{CORE}}{\Delta I_{CORE}} = \frac{8 \times R_{ADJ} \times R_{LX}}{N \times R_{COMM}}$$

where N is the phase number of operation.

The averaged current $\overline{I_X}$ is also injected into the resistor R_{IOUT} connected to IOUT pin for monitoring load current. Voltage at IOUT pin V_{IOUT} is proportional to load current and is calculated as:

$$V_{IOUT} = 8\overline{I_X} \times R_{IOUT} = \frac{8 \times I_{CORE} \times R_{ADJ} \times R_{LX}}{N \times R_{COMM}}$$

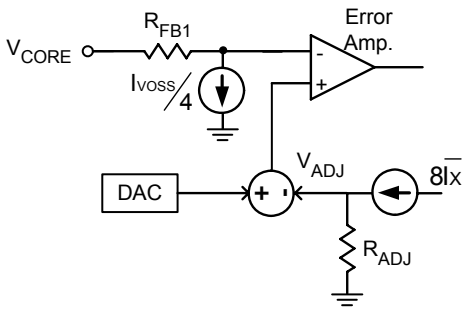


Figure 6. Load Line and Offset Function

Output Voltage Offset Function

RT9246A provides programmable initial offset function. External resistor R_{VOSS} and voltage source at VOSS pin generate offset current $I_{VOSS} = \frac{V_{VOSS}}{R_{VOSS}}$, where V_{VOSS} is 1V typical. One quarter of I_{VOSS} flows through R_{FB1} as shown in Figure 6. Error amplifier would hold the inverting pin equal to $V_{DAC} - V_{ADJ}$. A constant offset voltage is consequently added to $V_{DAC} - V_{ADJ}$ as :

$$V_{CORE} = V_{DAC} - V_{ADJ} + \frac{R_{FB1}}{4 \times R_{VOSS}}$$

Current Ratio Setting

Current ratio adjustment is possible as described below. It is important for achieving thermal balance in practical application where thermal conditions between phases are not identical. Figure 7 shows the application circuit of GM for current ratio requirement. According to Basic Circuit Theory, if

$$\frac{L_X}{R_{LX}} = (R_{SX} // R_{PX}) \times C_X \text{ then}$$

$$V_X = \frac{R_{PX}}{R_{SX}+R_{PX}} \times I_{LX} \times R_{LX}$$

With other phase kept unchanged, this phase would share (R_{PX}+R_{SX})/R_{PX} times current than other phases. Figure 8 and 9 show different current ratio setting for the power stage when Phase 3 is programmed 2 times current than other phases. Figure 10 and 11 compare the above current ratio setting results.

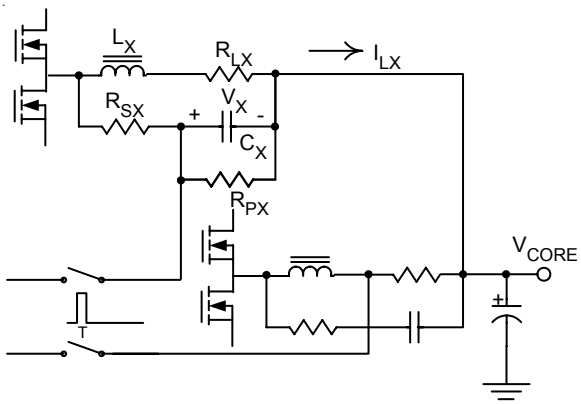


Figure 7

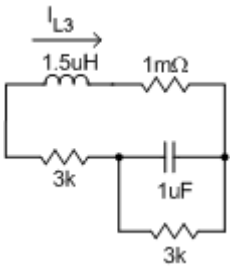


Figure 8. Phase 3 Setting for current ratio function

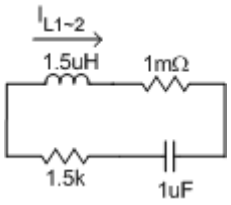


Figure 9. Phase 1~2 Setting for current ratio function

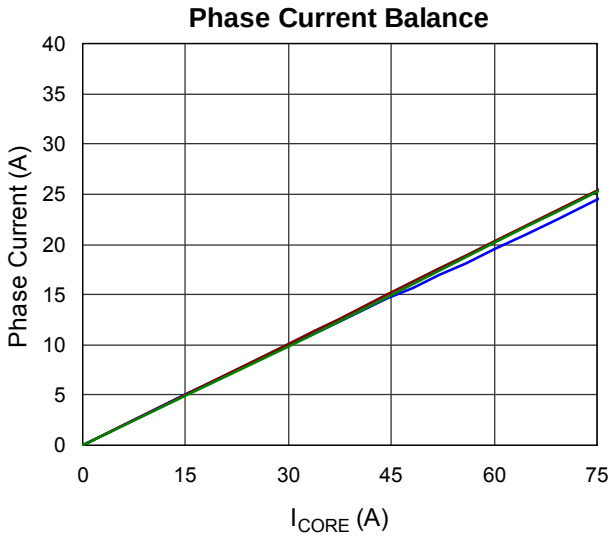


Figure 10

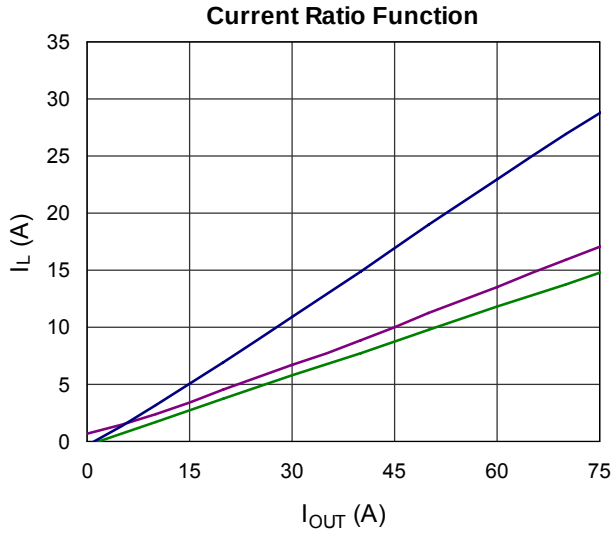


Figure 11

Dead Zone Elimination

RT9246A samples and holds inductor valley current by time-sharing sourcing a current I_X to R_{COMM}. At light load condition when averaged inductor current is smaller than half of peak-to-peak inductor ripple current, voltage V_X across the sensing capacitor is negative at valley. It needs a negative I_X to sense the voltage. However, RT9246A CANNOT provide a negative I_X and consequently cannot sense negative valley inductor current. This results in dead zone of load line performance as shown in Figure 12. Therefore a technique as shown in Figure 13 is required to eliminate the dead zone of load line at light load condition.

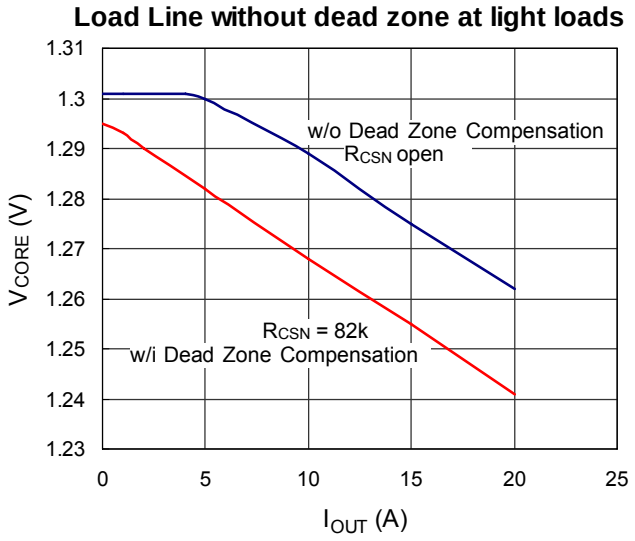


Figure 12

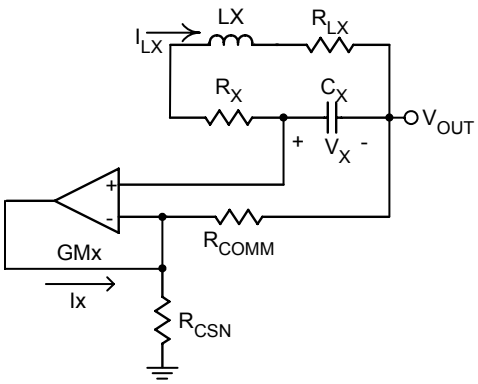


Figure13. Application circuit of GM

Referring to Figure 13, I_X is expressed as:

$$I_X = \frac{V_{OUT}}{R_{CSN}} + \frac{I_{LX_V} \times R_{LX}}{R_{CSN}} + \frac{I_{LX_V} \times R_{LX}}{R_{COMM}} \quad (1)$$

where I_{LX_V} is the valley of inductor current. To make sure RT9246A could sense the valley current, right hand side of Equation (1) should always be positive:

$$\frac{V_{OUT}}{R_{CSN}} + \frac{I_{LX_V} \times R_{LX}}{R_{CSN}} + \frac{I_{LX_V} \times R_{LX}}{R_{COMM}} \geq 0 \quad (2)$$

Since $R_{CSN} >> R_{COMM}$ in practical application, Equation (2) could be simplified as:

$$\frac{V_{OUT}}{R_{CSN}} \geq \left| \frac{I_{LX_V} \times R_{LX}}{R_{COMM}} \right|$$

For example, assuming the negative inductor valley current is –5A at no load, then for

R_{COMM} = 330Ω, R_{ADJ} = 160Ω, V_{OUT} = 1.300V

$$\frac{1.3V}{R_{CSN}} \geq \left| \frac{-5A \times 1m\Omega}{330\Omega} \right|$$

$R_{CSN} \leq 85.8k\Omega$

Choose R_{CSN} = 82kΩ

Figure 12 shows that dead zone of load line at light load is eliminated by applying this technique.

Error Amplifier Characteristic

For fast response of converter to meet stringent output current transient response, RT9246A provides large slew rate capability and high gain-bandwidth performance.

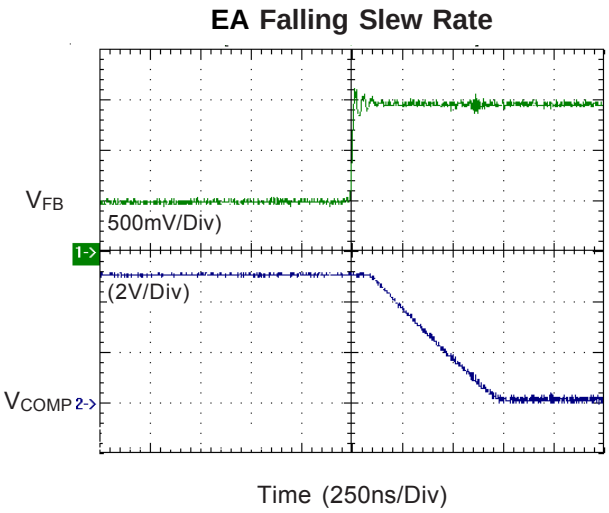


Figure 14. EA Rising Transient with 10pF Loading; Slew Rate=8V/us

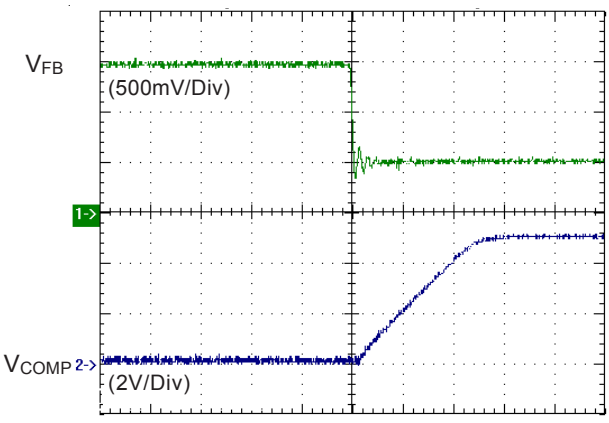


Figure 15. EA Falling Transient with 10pF Loading; Slew Rate=8V/us

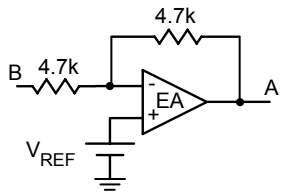


Figure 16. Gain-Bandwidth Measurement by signal A divided by signal B

Design Procedure Suggestion

a. Output filter pole and zero (Inductor, output capacitor value & ESR).

b. Error amplifier compensation & sawtooth wave amplitude (compensation network).

Current Loop Setting

a. GM amplifier S/H current (current sense component DCR, ISPX and ICOMMON pin external resistor value).

b. Over-current protection trip point (R_{IMAX} resistor).

VRM Load Line Setting

a. Droop amplitude (ADJ pin resistor).

b. No load offset (R_{CSN})

c. DAC offset voltage setting (VOSS pin and compensation network resistor RB1)

Power Sequence & SS

DVD pin external resistor and SS pin capacitor.

PCB Layout

a. Sense for current sense GM amplifier input.

b. Refer to layout guide for other items.

Voltage Loop Setting

Design Example

Given:

Apply for four phase converter

V_{IN} = 12V

V_{CORE} = 1.5V

$I_{LOAD(MAX)}$ = 100A

V_{DROOP} = 100mV at full load (1mΩ Load Line)

OCP trip point set at 35A for each channel (S/H)

DCR = 1mΩ of inductor at 25°C

L = 1.5µH

C_{OUT} = 8000µF with 5mΩ equivalent ESR.

1. Compensation Setting

a. Modulator Gain, Pole and Zero:

From the following formula:

Modulator Gain = V_{IN}/V_{RAMP} = 12/1.9 = 6.3 (i.e 16dB)

where V_{RAMP} : ramp amplitude of saw-tooth wave

LC Filter Pole = 1.45kHz and

ESR Zero = 3.98kHz

b. EA Compensation Network:

Select R1 = 4.7k, R2 = 15k, C1 = 12nF, C2 = 68pF and use the Type 2 compensation scheme shown in Figure 17. By calculation, the F_Z = 0.88kHz, F_P = 322kHz and Middle Band Gain is 3.19 (i.e 10.07dB).

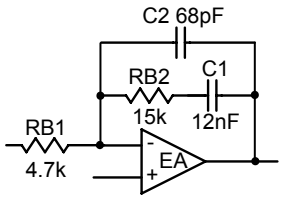


Figure 17. Type 2 compensation network of EA

Layout Guide

Place the high-power switching components first, and separate them from sensitive nodes.

1. Most critical path:

   The current sense circuit is the most sensitive part of the converter. The current sense resistors tied to ISP1,2,3 and ICOMMON should be located not more than 0.5 inch from the IC and away from the noise switching nodes. The PCB trace of sense nodes should be parallel and as short as possible. R&C filter of choke should place close to PWM and the R & C connect directly to the pin of each output choke, use 10 mil differencial pair, and 20 mil gap to other phase pair. Less via as possible.

2. Switching ripple current path:

   a. Input capacitor to high side MOSFET.

   b. Low side MOSFET to output capacitor.

   c. The return path of input and output capacitor.

   d. Separate the power and signal GND.

   e. The switching nodes (the connection node of high/low side MOSFET and inductor) is the most noisy points.Keep them away from sensitive small-signal node.

   f . Reduce parasitic R, L by minimum length, enough copper thickness and avoiding of via.

3. MOSFET driver should be closed to MOSFET.

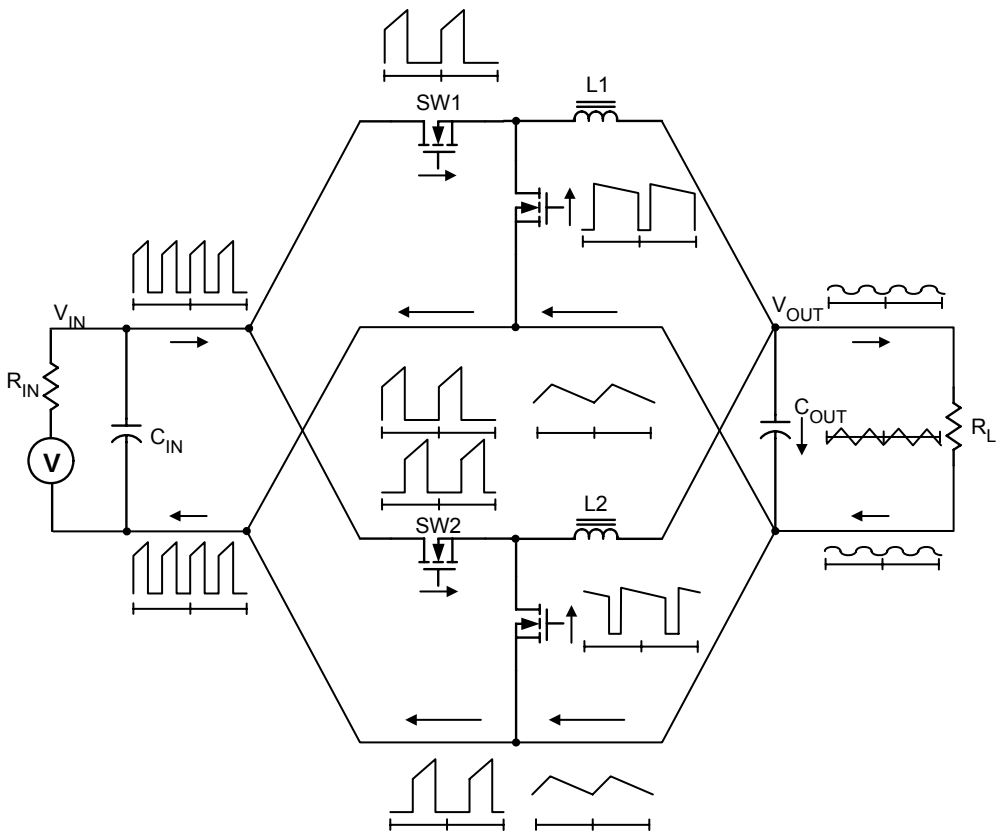
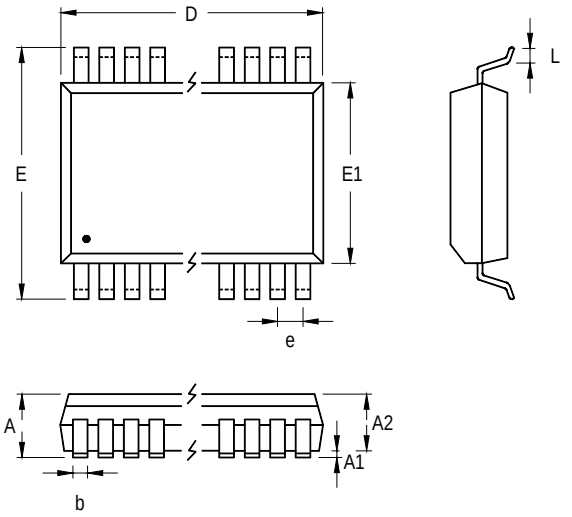


Figure 18. Power Stage Ripple Current Path

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.850	1.200	0.033	0.047
A1	0.050	0.152	0.002	0.006
A2	0.800	1.050	0.031	0.041
b	0.178	0.305	0.007	0.012
D	9.601	9.804	0.378	0.386
e	0.650		0.026	
E	6.300	6.500	0.248	0.256
E1	4.293	4.496	0.169	0.177
L	0.450	0.762	0.018	0.030

28-Lead TSSOP Plastic Package

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