4A, 1MHz, Synchronous Step-Down Converter

General Description

The RT8078A is a high efficiency synchronous, step-down DC/DC converter. It's input voltage range from 2.7V to 5.5V that provides an adjustable regulated output voltage from 0.6V to V_{IN} while delivering up to 4A of output current. The internal synchronous low on-resistance power switches increase efficiency and eliminate the need for an external Schottky diode. The switching frequency is fixed internally at 1MHz. The 100% duty cycle provides low dropout operation, hence extending battery life in portable systems. Current mode operation with internal compensation allows the transient response to be optimized over a wide range of loads and output capacitors. The RT8078A is operated in PWM mode to achieve high efficiency for a wide load range. The RT8078A is available in WDFN-10L 3x3 and SOP-8 (Exposed Pad) packages.

Ordering Information

RT8078A□□

Package Type
QW : WDFN-10L 3x3 (W-Type)
SP : SOP-8 (Exposed Pad-Option 2)

Lead Plating System
G : Green (Halogen Free and Pb Free)
Z : ECO (Ecological Element with Halogen Free and Pb free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

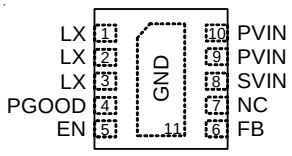
- **High Efficiency : Up to 95%**
- **Fixed Frequency : 1MHz**
- **No Schottky Diode Required**
- **Internal Compensation**
- **0.6V Reference Allows Low Output Voltage**
- **PWM Mode Operation**
- **Low Dropout Operation : 100% Duty Cycle**
- **OCP, UVP, OVP, OTP**
- **RoHS Compliant and Halogen Free**

Applications

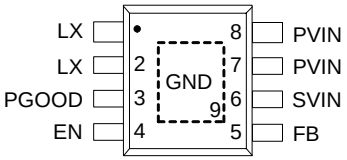
- Portable Instruments
- Battery Powered Equipment
- Notebook Computers
- Distributed Power Systems
- IP Phones
- Digital Cameras

Pin Configurations

(TOP VIEW)



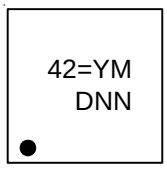
WDFN-10L 3x3



SOP-8 (Exposed Pad)

Marking Information

RT8078AGQW



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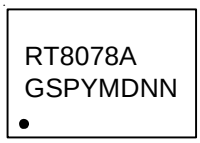
RT8078AGSP



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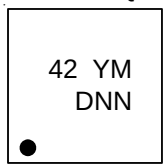

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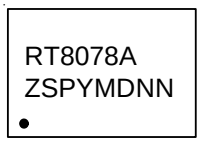
RT8078AZSP



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Typical Application Circuit

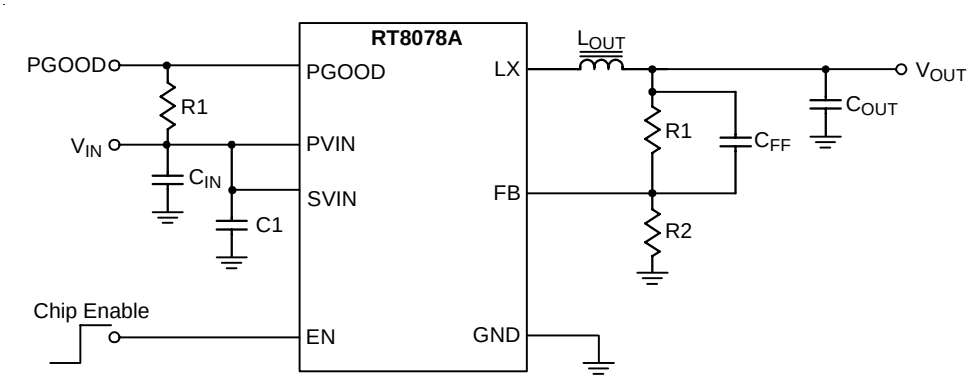


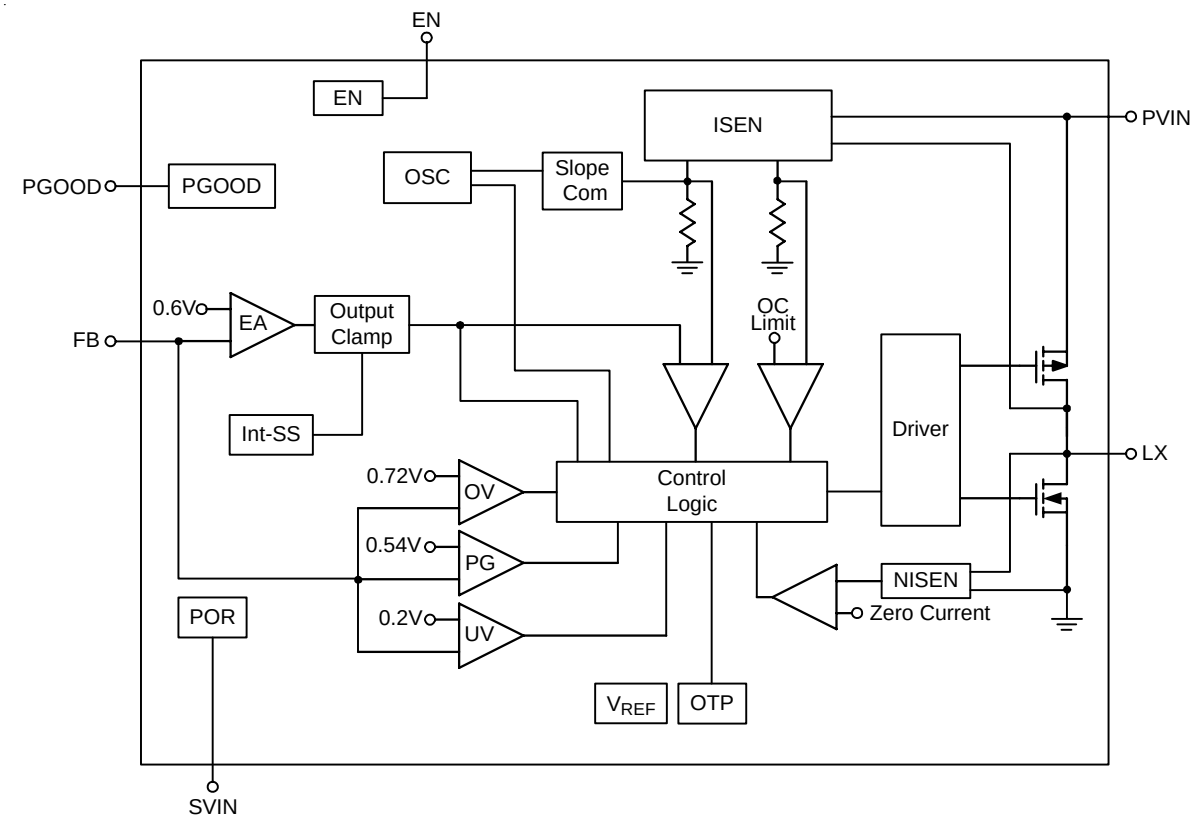
Table 1. Recommended Component Selection

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{FF} (pF)	L (µH)	C_{OUT} (µF)
3.3	229.5	51	22	2	22 x 2
2.5	161.5	51	22	2	22 x 2
1.8	102	51	22	1.5	22 x 2
1.5	76.5	51	22	1.5	22 x 2
1.2	51	51	22	1.5	22 x 2
1.0	34	51	22	1.5	22 x 2

Functional Pin Description

Pin No.		Pin Name	Pin Function
WDFN-10L 3x3	SOP-8 (Exposed Pad)		
1, 2, 3	1, 2	LX	Switch Node. Connect this pin to the inductor.
4	3	PGOOD	Power Good Indicator. This pin is an open drain logic output that is pulled to ground when the output voltage is less than 90% of the target output voltage. Hysteresis = 5%.
5	4	EN	Enable Control. Pull high to turn on. Do not float.
6	5	FB	Feedback Pin. This pin receives the feedback voltage from a resistive voltage divider connected across the output.
7	--	NC	No Internal Connection.
8	6	SVIN	Signal Input Pin. Decouple this pin to GND with at least 1μF ceramic cap.
9,10	7,8	PVIN	Power Input Pin. Decouple this pin to GND with at least 4.7μF ceramic cap.
11 (Exposed Pad)	9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Function Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, PVIN, SVIN ---------- –0.3V to 6.5V
- LX Pin Voltages ---------- –0.3V to (V_{IN} + 0.3V)
- Other I/O Pin Voltage ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  - WDFN-10L 3x3 ---------- 1.429W
  - SOP-8 (Exposed Pad) ---------- 1.333W
- Package Thermal Resistance (Note 2)
  - WDFN-10L 3x3, θ_{JA} ---------- 70°C/W
  - WDFN-10L 3x3, θ_{JC} ---------- 8.2°C/W
  - SOP-8 (Exposed Pad), θ_{JA} ---------- 75°C/W
  - SOP-8 (Exposed Pad), θ_{JC} ---------- 15°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Mode) ---------- 2kV
  - MM (Machine Mode) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage, PVIN, SVIN ---------- 2.7V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.3V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Feedback Reference Voltage		V_{REF}		0.594	0.6	0.606	V
Feedback Leakage Current		I_{FB}		--	0.1	0.4	μA
DC Bias Current			Active , V_{FB} = 0.58V, Not Switching	--	110	--	μA
			Shutdown	--	--	1	
Output Voltage Line Regulation			V_{IN} = 2.7V to 5.5V I_{OUT} = 0A	--	0.3	--	%/V
Output Voltage Load Regulation			I_{OUT} = 0A to 4A	–2	--	2	%
Switch Leakage Current				--	--	1	μA
Switching Frequency				0.8	1	1.2	MHz
Switch On Resistance, High		$R_{DS(ON)_P}$	V_{IN} = 5V	--	69	--	mΩ
Switch On Resistance, Low		$R_{DS(ON)_N}$	V_{IN} = 5V	--	49	--	mΩ
P-MOSFET Current Limit		I_{LIM}		4.4	--	--	A
Under Voltage Lockout Threshold		V_{UVLO}	V_{IN} Rising	--	2.4	--	V
			V_{IN} Falling	--	2.2	--	
EN Input Threshold Voltage	Logic-High	V_{IH}		1.6	--	--	V
	Logic-Low	V_{IL}		--	--	0.4	

To be continued

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
EN Pull Low Resistance			--	500	--	kΩ
Over Temperature Protection	T_{SD}		--	150	--	°C
Over Temperature Protection Hysteresis	ΔT_{SD}		--	20	--	°C
Soft-Start Time	t_{SS}		500	--	--	μs
V_{OUT} Discharge Resistance			--	100	--	Ω
V_{OUT} Over Voltage Protection (Latch-Off, Delay Time = 10μs)			--	120	--	%
V_{OUT} Under Voltage Lock Out (Latch-Off)			--	33	--	%
Power Good		Measured FB, With Respect to V_{REF}	--	90	--	%
Power Good Hysteresis			--	5	--	%

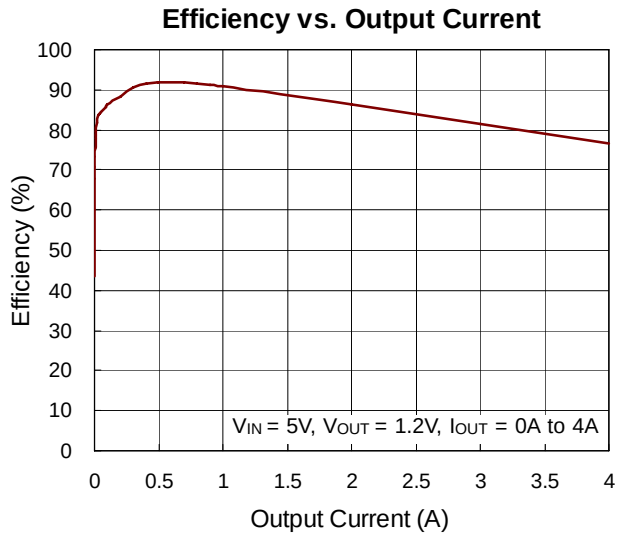
Note 1. Stresses listed as the above "Absolute Maximum Ratings" may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

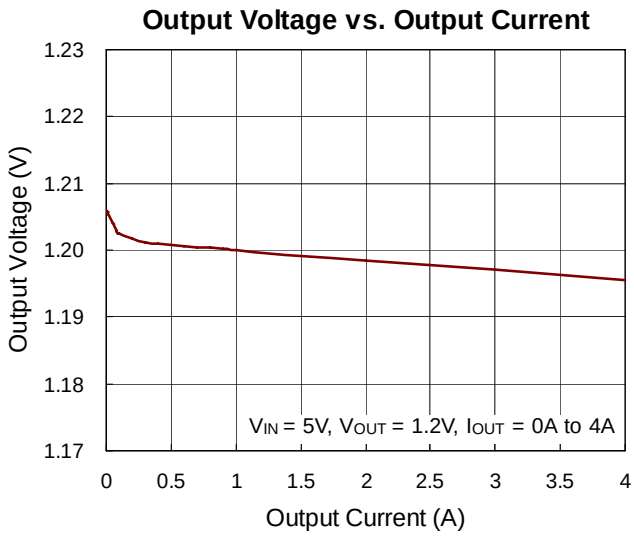
Note 2. θ_{JA} is measured in natural convection at T_A = 25°C on a high effective thermal conductivity four-layer test board of JEDEC 51-7 thermal measurement standard. The measurement case position of θ_{JC} is on the exposed pad of the packages.

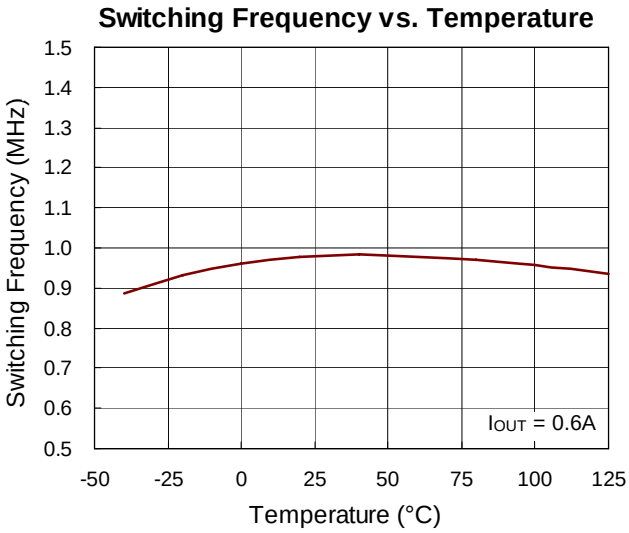
Note 3. Devices are ESD sensitive. Handling precaution is recommended.

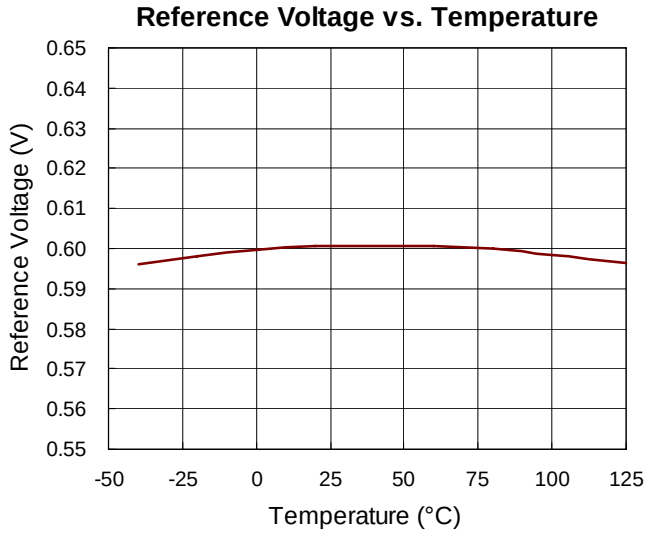
Note 4. The device is not guaranteed to function outside its operating conditions.

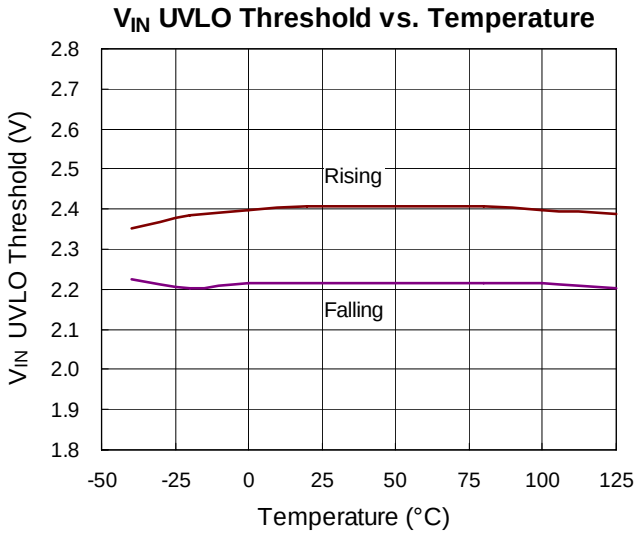
Typical Operating Characteristics

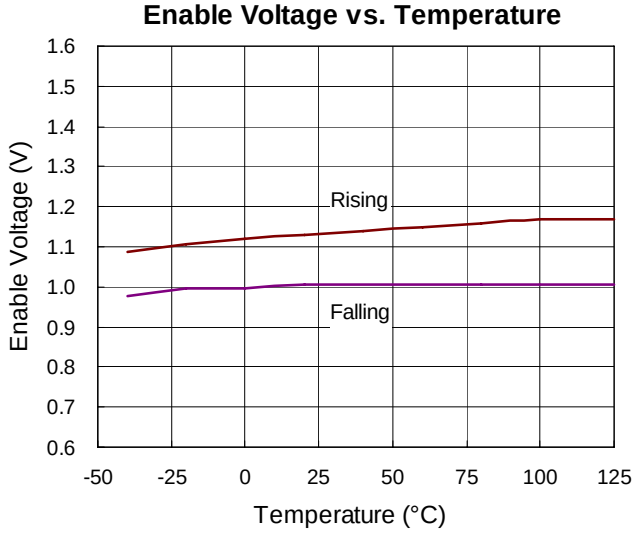




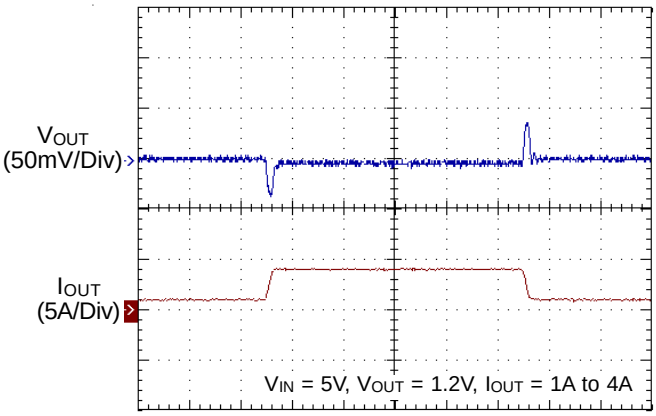




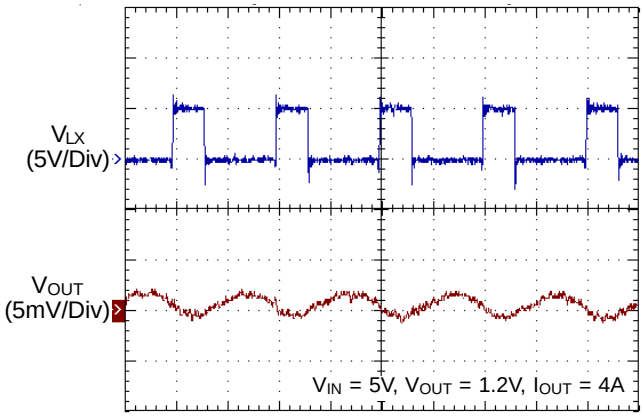




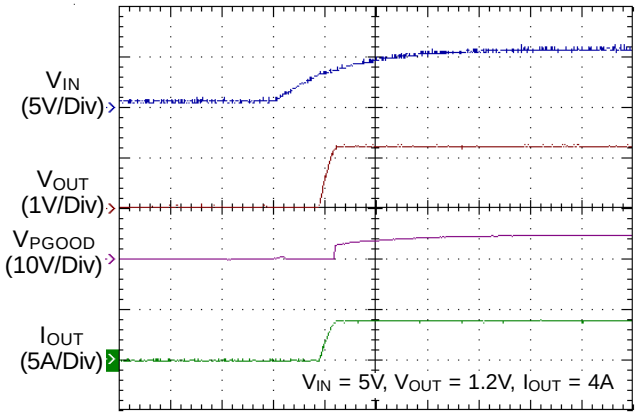
Load Transient Response



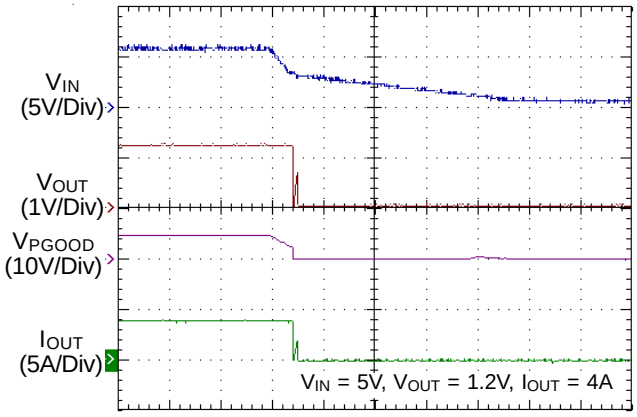
Switching



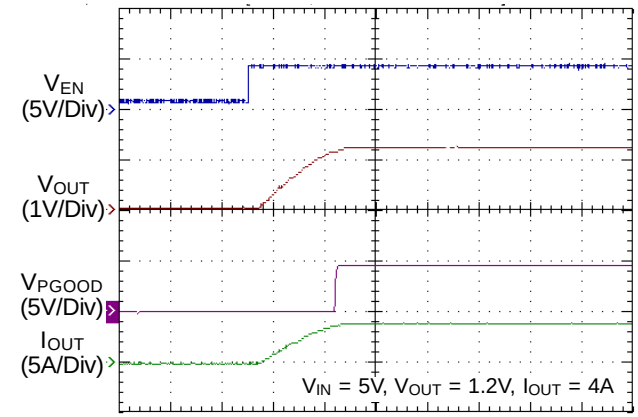
Power On from V_{IN}



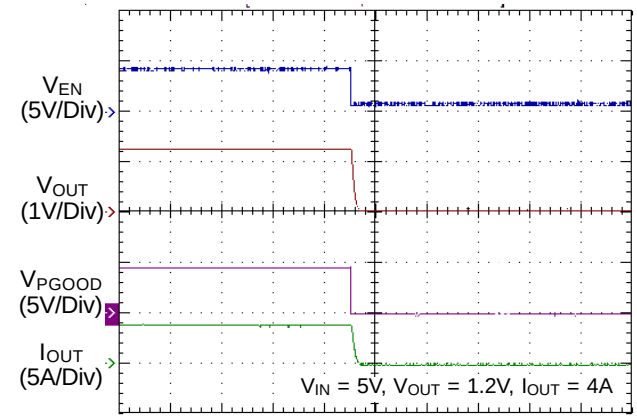
Power Off from V_{IN}



Power On from EN



Power Off from EN



Application Information

The RT8078A is a single-phase buck PWM converter. It provides single feedback loop, current mode control with fast transient response. An internal 0.6V reference allows the output voltage to be precisely regulated for low output voltage applications. A fixed switching frequency (1MHz) oscillator and internal compensation are integrated to minimize external component count.

Main Control Loop

During normal operation, the internal high side power switch (P-MOSFET) is turned on at the beginning of each clock cycle. Current in the inductor increases until the peak inductor current reaches the value defined by the output voltage (V_{COMP}) of the error amplifier. The error amplifier adjusts its output voltage by comparing the feedback signal from a resistive voltage divider on the FB pin with an internal 0.6V reference. When the load current increases, it causes a reduction in the feedback voltage relative to the reference. The error amplifier raises its output voltage until the average inductor current matches the new load current. Once the high side power MOSFET shuts off, the synchronous power switch (N-MOSFET) turns on until the beginning of the next clock cycle.

Output Voltage Setting

The output voltage is set by an external resistive voltage divider according to the following equation :

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

where V_{REF} equals 0.6V (typ.).

The resistive voltage divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 1.

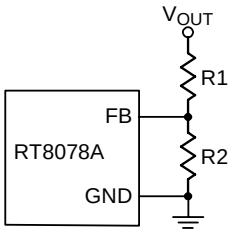


Figure 1. Setting the Output Voltage

Soft-Start

The IC contains an internal soft-start function to prevent large inrush current and output voltage overshoot when the converter starts up. Soft-start automatically begins once the chip is enabled. During soft-start, the internal soft-start capacitor becomes charged and generates a linear ramping up voltage across the capacitor. This voltage clamps the voltage at the FB pin, causing the duty pulse width to increase slowly and in turn reduce the output surge current. Finally, the internal 0.6V reference takes over the loop control once the internal ramping-up voltage becomes higher than 0.6V. The minimum soft-start time for this IC is set at 500µs.

Power Good Output

The power good output is an open-drain output and requires a pull up resistor. When the output voltage is 85% below its set voltage, PGOOD will be pulled low. It is held low until the output voltage returns to within the allowed tolerances once more. During soft-start, PGOOD is actively held low and only allowed to transition high after soft-start is over and the output voltage has reached 90% of its set voltage.

Inductor Selection

For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance.

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

Having a lower ripple current reduces not only the ESR losses in the output capacitors but also the output voltage ripple. Highest efficiency operation is achieved by reducing ripple current at low frequency, but a large inductor is required to attain this goal.

For ripple current selection, the value of $\Delta I_L = 0.4(I_{MAX})$ is a reasonable starting point. The largest ripple current occurs at the highest V_{IN}. To guarantee that the ripple current stays below a specified maximum value, the inductor should be chosen according to the following equation :

$$L = \left[\frac{V_{OUT}}{f \times \Delta I_{L(MAX)}}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. However, care must be taken when these capacitors are used at the input and output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN} large enough to damage the part.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing sub-harmonic oscillations at duty cycles greater than 50%. It is accomplished internally by adding a compensating ramp to the inductor current signal. Normally, the maximum inductor peak current is reduced when slope compensation is added. In this IC, however, separated inductor current signal is used to monitor over current condition and this keeps the maximum output current relatively constant regardless of duty cycle.

Over Voltage Protection

The IC provides over voltage protection once the output voltage exceeds 120% of V_{OUT}, The OVP function latches off the switching operation and can only be released by toggling EN threshold or cycling V_{IN}. There is a 10μs delay built into the over voltage protection circuit to prevent false transition.

Under Voltage Lockout Threshold

The IC includes an input Under Voltage Lockout Protection (UVLO). If the input voltage exceeds the UVLO rising threshold voltage, the converter resets and prepares the PWM for operation. If the input voltage falls below the UVLO falling threshold voltage during normal operation, the device stops switching. The UVLO rising and falling threshold voltage includes a hysteresis to prevent noise-caused reset.

Thermal Shutdown

The device implements an internal thermal shutdown function when the junction temperature exceeds 150°C. The thermal shutdown disables the device until the junction temperature drops below the hysteresis (20°C typ.). Then, the device is re-enabled and automatically reinstates the power up sequence.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications of the RT8078A, the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For SOP-8 (Exposed Pad) packages, the thermal resistance, θ_{JA}, is 75°C/W on a standard JEDEC 51-7 four-layer thermal test board. For WDFN-10L 3x3 packages, the thermal resistance, θ_{JA}, is 70°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formulas :

$P_{D(MAX)}$ = (125°C – 25°C) / (75°C/W) = 1.333W for SOP-8 (Exposed Pad) package

$P_{D(MAX)}$ = (125°C – 25°C) / (70°C/W) = 1.429W for WDFN-10L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. For the RT8078A package, the derating curves in Figure 2 allow the designer to see the effect of rising ambient temperature on the maximum power dissipation.

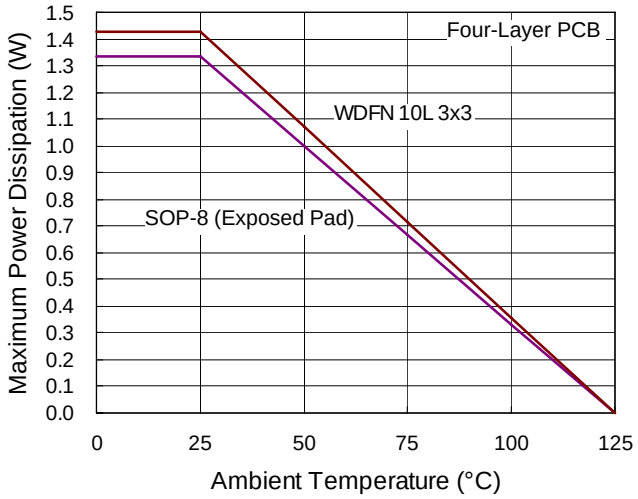


Figure 2. Derating Curves for the RT8078A Packages

Layout Considerations

Follow the PCB layout guidelines for optimal performance of the IC.

- Place the terminal of the input capacitor(s), C_{IN}, as close as possible to the VIN pin. This capacitor provides the AC current into the internal power MOSFETs.
- LX node experiences high frequency voltage swing and should be kept within a small area.
- Keep all sensitive small-signal nodes away from the LX node to prevent stray capacitive noise pick up.
- Connect the FB pin directly to the feedback resistors. The resistive voltage divider must be connected between V_{OUT} and GND.

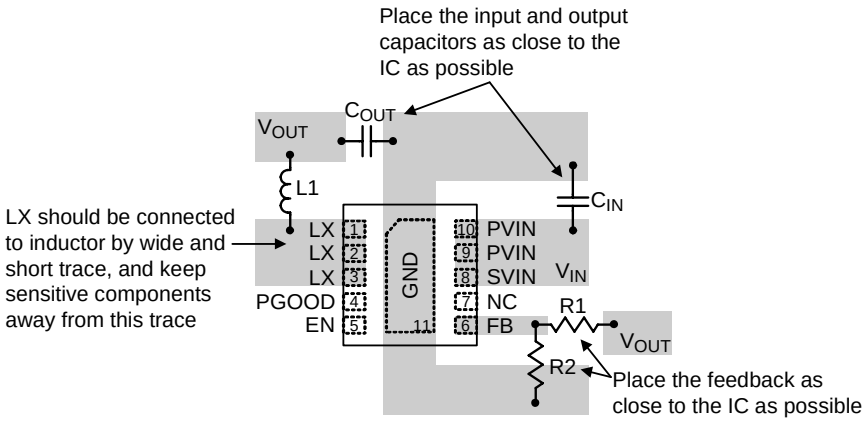


Figure 3. PCB Layout Guide for WDFN-10L 3x3

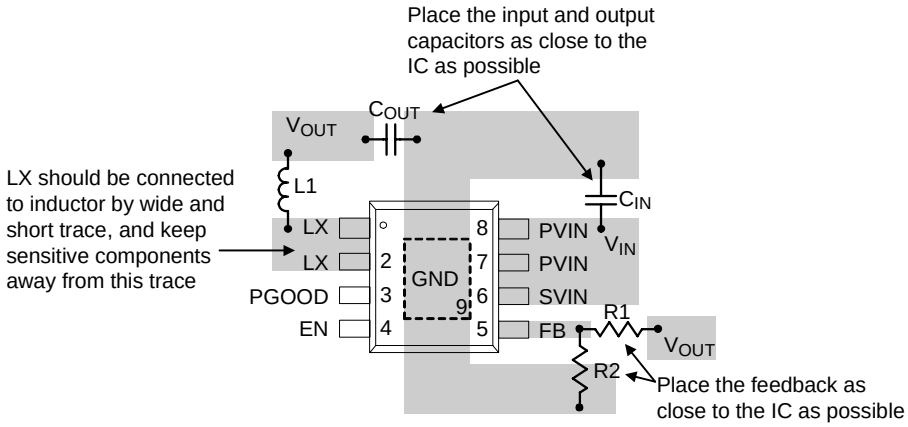
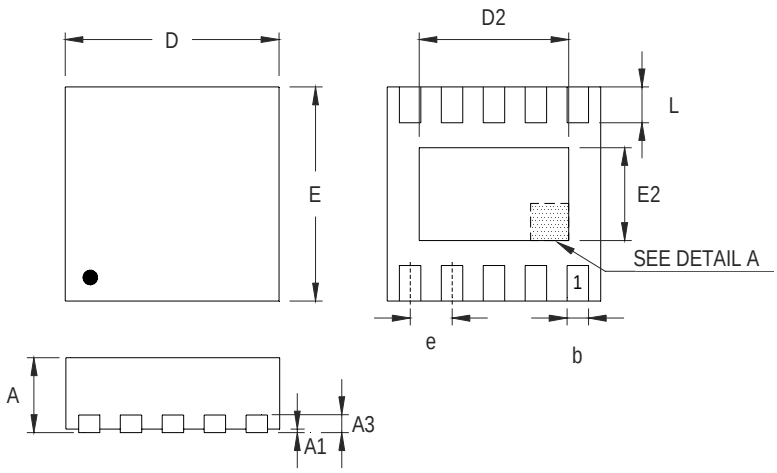
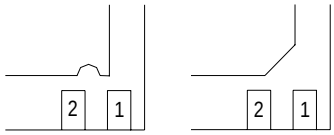


Figure 4. PCB Layout Guide for SOP-8 (Exposed Pad)

Outline Dimension





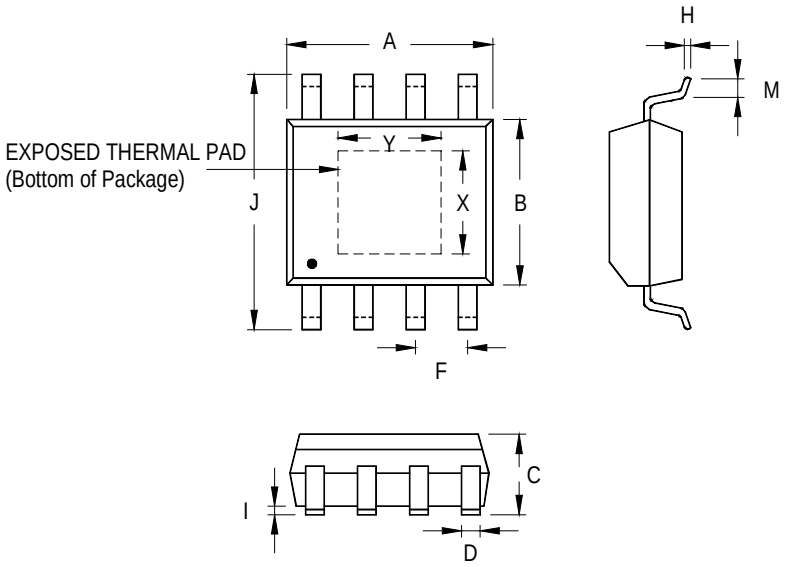
DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package



Symbol		Dimensions In Millimeters		Dimensions In Inches	
		Min	Max	Min	Max
A		4.801	5.004	0.189	0.197
B		3.810	4.000	0.150	0.157
C		1.346	1.753	0.053	0.069
D		0.330	0.510	0.013	0.020
F		1.194	1.346	0.047	0.053
H		0.170	0.254	0.007	0.010
I		0.000	0.152	0.000	0.006
J		5.791	6.200	0.228	0.244
M		0.406	1.270	0.016	0.050
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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