Transistor

# 4V Drive Nch MOS FET

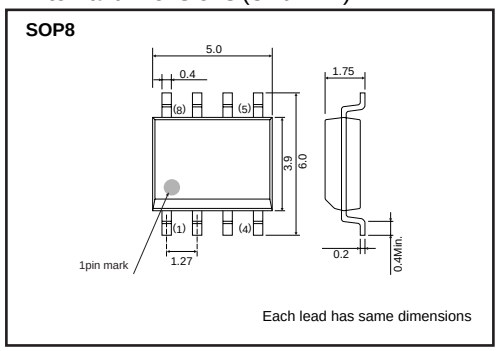
## RSS095N05

### ●Structure
Silicon N-channel
MOS FET

### ●Features
1) Built-in G-S Protection Diode.
2) Small Surface Mount Package (SOP8).

### ●Applications
Power switching , DC / DC converter , Inverter

### ●External dimensions (Unit : mm)




### ●Packaging dimensions

| Package | Taping |
|---|---|
| Code | TB |
| Basic ordering unit(pieces) | 2500 |

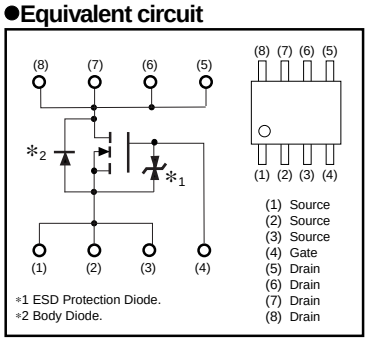
### ●Absolute maximum ratings (Ta=25°C)

| Parameter | | Symbol | Limits | Unit |
|---|---|---|---|---|
| Drain-source voltage | | $V_{DSS}$ | 45 | V |
| Gate-source voltage | | $V_{GSS}$ | 20 | V |
| Drain current | Continuous | $I_D$ | ±9.5 | A |
| | Pulsed | $I_{DP}$ *1 | ±38 | A |
| Source current (Body diode) | Continuous | $I_S$ | 1.6 | A |
| | Pulsed | $I_{SP}$ *1 | 38 | A |
| Total power dissipation | | $P_D$ *2 | 2 | W |
| Chanel temperature | | $T_{ch}$ | 150 | °C |
| Range of Storage temperature | | $T_{stg}$ | -55 to +150 | °C |

*1 PW≤10μs、Duty cycle≤1%

*2 Mounted on a ceramic board

### ●Equivalent circuit




* A protection diode is included between the gate and the source terminals to protect the diode against static electricity when the product is in use.Use a protection circuit when the fixed voltage are exceeded.

### ●Thermal resistance

| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Chanel to ambient | $R_{th(ch-a)}$ * | 62.5 | °C/W |

* Mounted on a ceramic board

●**Electrical characteristics** (Ta=25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Gate-source leakage | $I_{GSS}$ | – | – | 10 | μA | $V_{GS}$=20V, $V_{DS}$=0V |
| Drain-source breakdown voltage | $V_{(BR)\ DSS}$ | 45 | – | – | V | $I_D$= 1mA, $V_{GS}$=0V |
| Zero gate voltage drain current | $I_{DSS}$ | – | – | 1 | μA | $V_{DS}$= 45V, $V_{GS}$=0V |
| Gate threshold voltage | $V_{GS\ (th)}$ | 1.0 | – | 2.5 | V | $V_{DS}$= 10V, $I_D$= 1mA |
| Static drain-source on-state resistance | $R_{DS\ (on)}$* | – | 11 | 16 | mΩ | $I_D$= 9.5A, $V_{GS}$= 10V |
| | | – | 14 | 20 | mΩ | $I_D$= 9.5A, $V_{GS}$= 4.5V |
| | | – | 15 | 21 | mΩ | $I_D$= 9.5A, $V_{GS}$= 4V |
| Forward transfer admittance | $\|Y_{fs}\|$ * | 10.0 | – | – | S | $V_{DS}$= 10V, $I_D$= 9.5A |
| Input capacitance | $C_{iss}$ | – | 1830 | – | pF | $V_{DS}$= 10V |
| Output capacitance | $C_{oss}$ | – | 410 | – | pF | $V_{GS}$=0V |
| Reverse transfer capacitance | $C_{rss}$ | – | 210 | – | pF | f=1MHz |
| Turn-on delay time | $t_{d\ (on)}$ * | – | 20 | – | ns | $V_{DD}$≒ 25V |
| Rise time | $t_r$ * | – | 35 | – | ns | $I_D$= 5.0A |
| Turn-off delay time | $t_{d\ (off)}$ * | – | 78 | – | ns | $V_{GS}$= 10V<br>$R_L$=5Ω |
| Fall time | $t_f$ * | – | 31 | – | ns | $R_G$=10Ω |
| Total gate charge | $Q_g$ * | – | 18.9 | 26.5 | nC | $V_{DD}$≒ 25V $V_{GS}$= 5V |
| Gate-source charge | $Q_{gs}$ * | – | 4.9 | – | nC | $I_D$= 9.5A |
| Gate-drain charge | $Q_{gd}$ * | – | 7.2 | – | nC | $R_L$=2.6Ω $R_G$=10Ω |

*Pulsed

**Body diode characteristics** (Source-Drain) (Ta=25°C)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Forward voltage | $V_{SD}$* | – | – | 1.2 | V | $I_S$= 9.5A, $V_{GS}$=0V |

*Pulsed

## ●Electrical characteristic curves

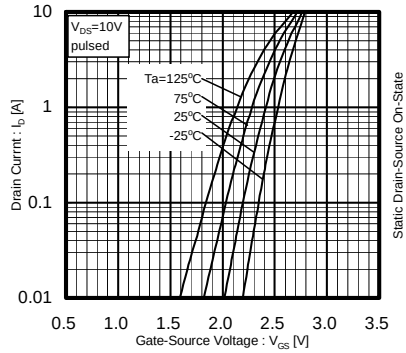



Fig.1 Typical Transfer Characteristics

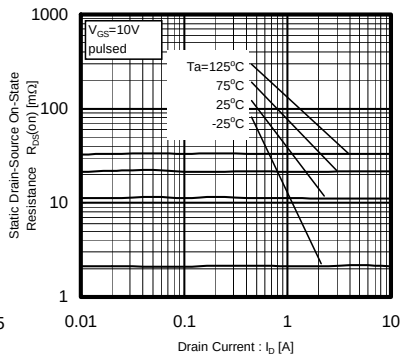



Fig.2 Static Drain-Source On-State Resistance vs. Drain Current (1)

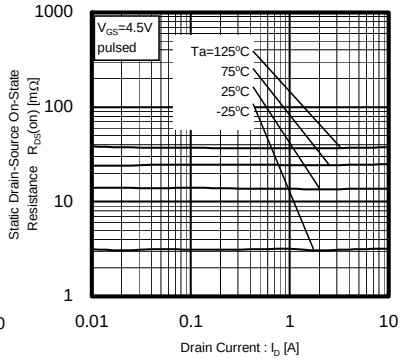



Fig.3 Static Drain-Source On-State Resistance vs. Drain Current (2)

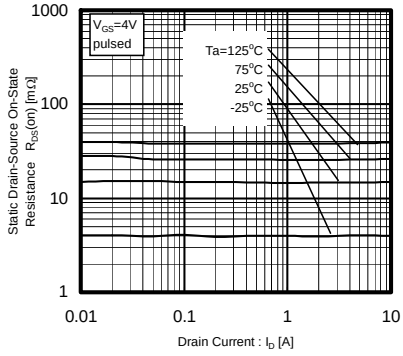



Fig.4 Static Drain-Source On-State Resistance vs. Drain Current (3)

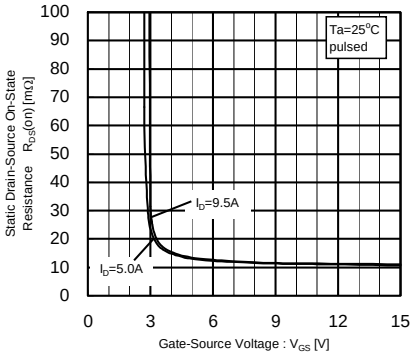



Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

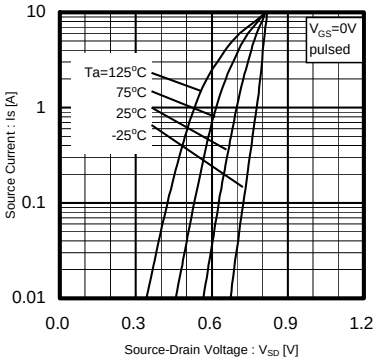



Fig.6 Source-Current vs. Source-Drain Voltage

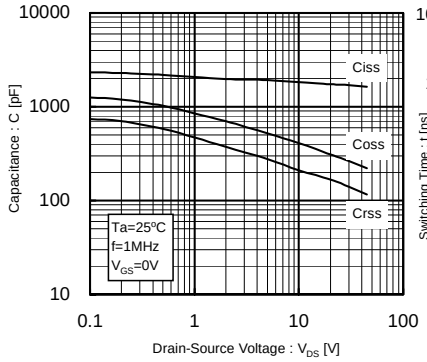



Fig.7 Typical capacitance vs. Source-Drain Voltage

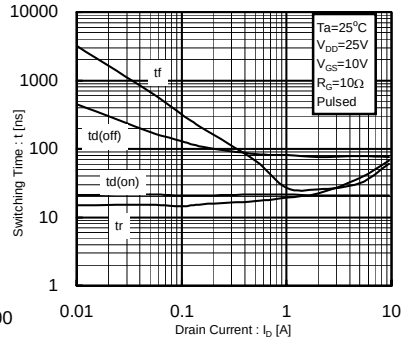



Fig.8 Switching Characteristics

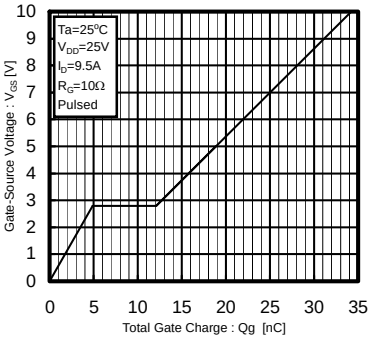



Fig.9 Dynamic Input Characteristics

●**Measurement circuits**

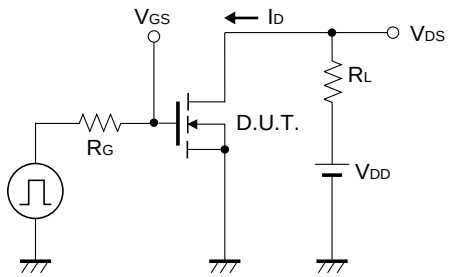



Fig.10 Switching Time Test Circuit

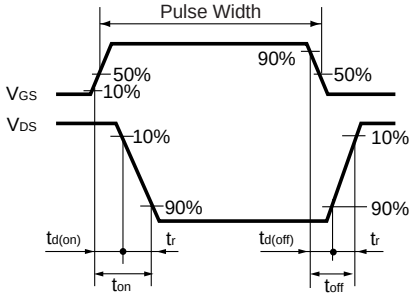



Fig.11 Switching Time Waveforms

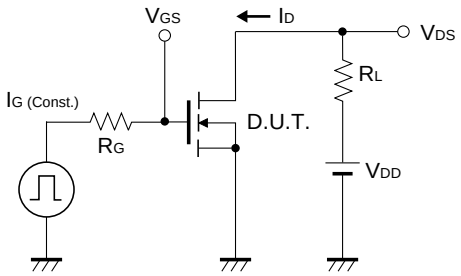



Fig.12 Gate Charge Test Circuit

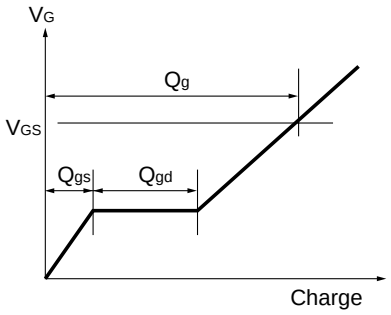



Fig.13 Gate Charge Waveform

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