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RFHA1025

280W GaN Wideband Pulsed Power Amplifier



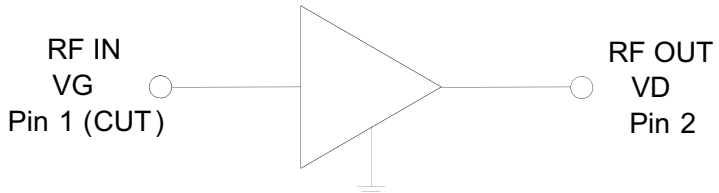
Package: Flanged Ceramic, 2-Pin

Features

- Wideband Operation: 0.96GHz to 1.215GHz
- Advanced GaN HEMT Technology
- Advanced Heat-Sink Technology
- Supports Multiple Pulse Conditions
  - 10% to 20% Duty Cycle
  - 100µs to 1ms Pulse Width
- Integrated Matching Components for High Terminal Impedances
- 50V Operation Typical Performance
  - Output Pulsed Power 280W
  - Pulse Width 100µS, Duty Cycle 10%
  - Small Signal Gain 17dB
  - High Efficiency 55%
  - -40°C to 85°C Operating Temperature

Applications

- Radar
- Air Traffic Control and Surveillance
- General Purpose Broadband Amplifiers



Functional Block Diagram

Product Description

The RFHA1025 is a 50V 280W high power discrete amplifier designed for L-band pulsed radar, air traffic control and surveillance and general purpose broadband amplifier applications. Using an advanced high power density gallium nitride (GaN) semiconductor process, these high performance amplifiers achieve high output power, high efficiency and flat gain over a broad frequency range in a single package. The RFHA1025 is a matched power transistor packaged in a hermetic, flanged ceramic package. The package provides excellent thermal stability through the use of advanced heat sink and power dissipation technologies. Ease of integration is accomplished through the incorporation of single, optimized matching networks that provide wideband gain and power performance in a single amplifier.

Ordering Information

RFHA1025S2	2-Piece sample bag
RFHA1025SB	5-Piece bag
RFHA1025SQ	25-Piece bag
RFHA1025SR	50 Pieces on 7" short reel
RFHA1025TR13	250 Pieces on 13" reel
RFHA1025PCBA-410	Fully assembled evaluation board 0.96GHz to .215GHz;50V

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☑ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ BiFET HBT
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ SOI

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Absolute Maximum Ratings

Parameter	Rating	Unit
Drain Voltage (V_D)	150	V
Gate Voltage (V_G)	-8 to 2	V
Gate Current (I_G)	155	mA
Ruggedness (VSWR)	10:1	
Storage Temperature Range	-55 to +125	°C
Operating Temperature Range (T_C)	-40 to +85	°C
Operating Junction Temperature (T_J)	250	°C
Human Body Model	Class 1B	
MTTF (T_J < 200°C, 95% Confidence Limits)*	1.8E + 07	Hours
MTTF (T_J < 250°C, 95% Confidence Limits)*	1.1E + 05	Hours
Thermal Resistance, R_{TH} (junction to case): T_C = 85 °C, DC bias only T_C = 85 °C, 100µs pulse, 10% duty cycle T_C = 85°C, 1ms pulse, 10% duty cycle	 0.90 0.18 0.34	°C/W

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

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RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

* MTTF - median time to failure for wear-out failure mode (30% I_{DSS} degradation) which is determined by the technology process reliability. Refer to product qualification report for FIT(random) failure rate.
Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values.
Bias Conditions should also satisfy the following expression: $P_{DISS} < (T_J - T_C)/R_{TH\ J-C}$ and $T_C = T_{CASE}$

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Recommended Operating Conditions					
Drain Voltage (V_{DSQ})		50		V	
Gate Voltage (V_{GSQ})	-8	-3	-2	V	
Drain Bias Current		440		mA	
Frequency of Operation	960		1215	MHz	
DC Functional Test					
$I_{G\ (OFF)}$ – Gate Leakage			2	mA	V_G = -8V, V_D = 0V
$I_{D\ (OFF)}$ – Drain Leakage			2.5	mA	V_G = -8V, V_D = 50V
$V_{GS\ (TH)}$ – Threshold Voltage		-3.5		V	V_D = 50V, I_D = 40mA
$V_{DS\ (ON)}$ – Drain Voltage at High Current		0.28		V	V_G = 0V, I_D = 1.5A
RF Functional Test					[1], [2]
Small Signal Gain		17		dB	f = 960MHz, P_{IN} = 28dBm
Power Gain	13	14.2		dB	f = 960MHz, P_{IN} = 41dBm
Input Return Loss		-7.5	-5	dB	
Output Power	54	55.2		dBm	
Drain Efficiency	50	55		%	
Small Signal Gain		17		dB	f = 1215MHz, P_{IN} = 28dBm
Power Gain	13	13.6		dB	f = 1215MHz, P_{IN} = 41dBm
Input Return Loss		-7	-5	dB	
Output Power	54	54.6		dBm	
Drain Efficiency	50	59		%	

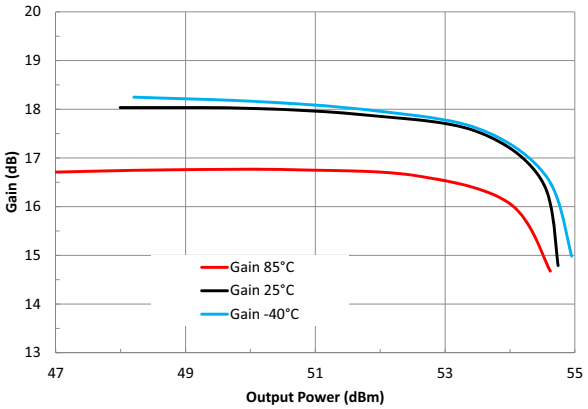
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
RF Typical Performance					[1], [2]
Frequency Range	960		1215	MHz	
Small Signal Gain		17		dB	P_{IN} = 28dBm
Power Gain		14		dB	P_{OUT} = 54.5dBm
Gain Variation with Temperature				dB/ °C	At peak output power
Output Power (P_{SAT})		54.5		dBm	Peak output power
		280		W	
Drain Efficiency		55		%	At peak output power

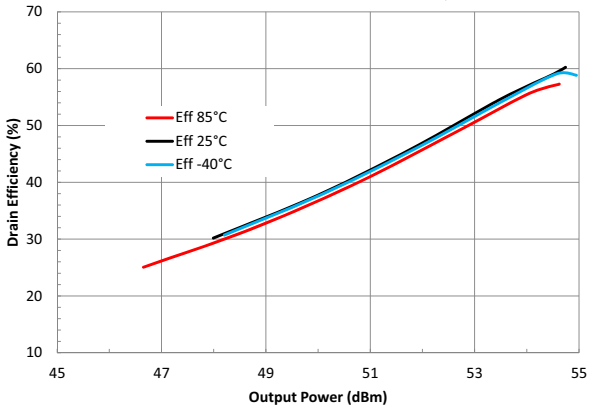
[1] Test Conditions: PW = 100µs, DC = 10%, V_{DSQ} = 50V, I_{DQ} = 440mA, T = 25 °C.
[2] Performance in a standard tuned test fixture.

Typical Performance in Standard Fixed Tuned Test Fixture (T = 25°C, unless noted)

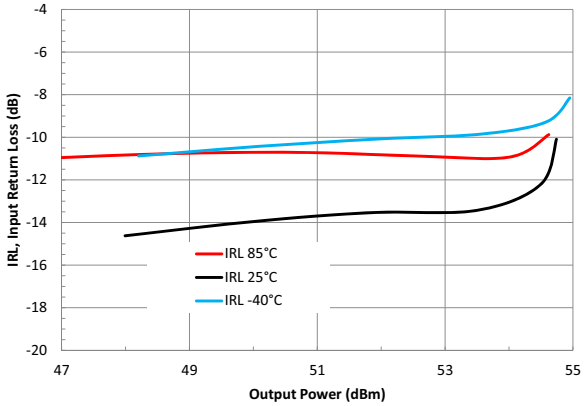
Gain versus Output Power (f = 1100MHz)
(Pulsed 10% duty cycle, PW=100µs, V_D = 50V, I_{DQ} = 440mA)



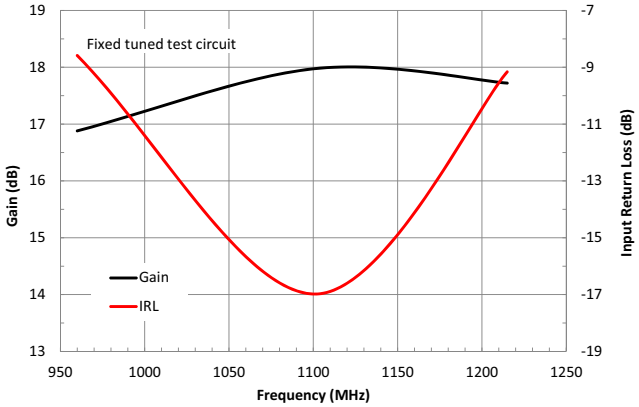
Efficiency versus Output Power (f = 1100MHz)
(Pulsed 10% duty cycle, PW = 100µS, V_D = 50V, I_{DQ} = 440mA)



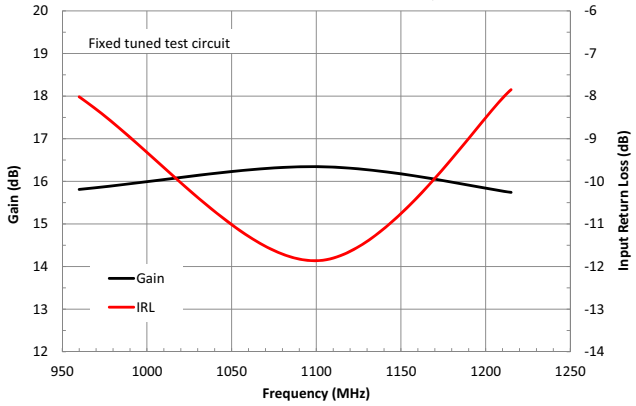
Input Return Loss versus Output Power (f = 1100MHz)
(Pulsed 10% duty cycle, PW = 100µS, V_D = 50V, I_{DQ} = 440mA)



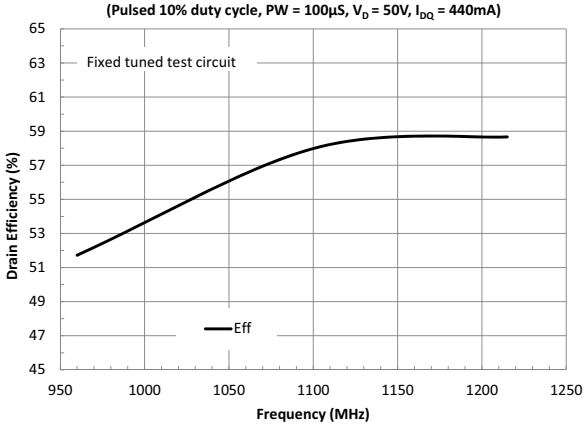
Small Signal Performance versus Frequency, P_{OUT} = 45dBm
(Pulsed 10% duty cycle, PW = 100µs, V_D = 50V, I_{DQ} = 440mA)



Gain/IRL versus Frequency, P_{OUT} = 54.5dBm
(Pulsed 10% duty cycle, PW=100µs, V_D = 50V, I_{DQ} = 440mA)

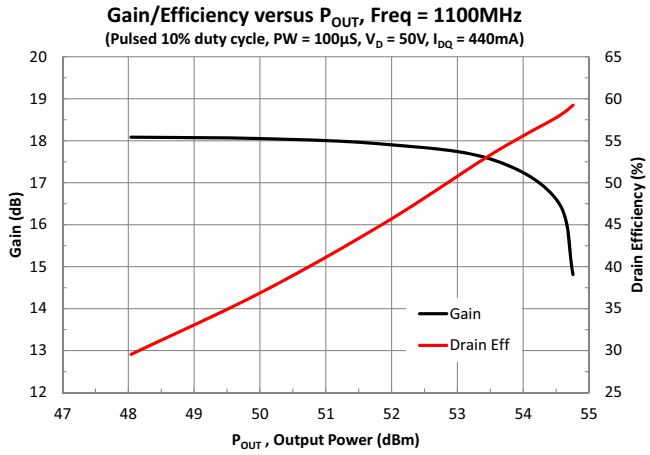


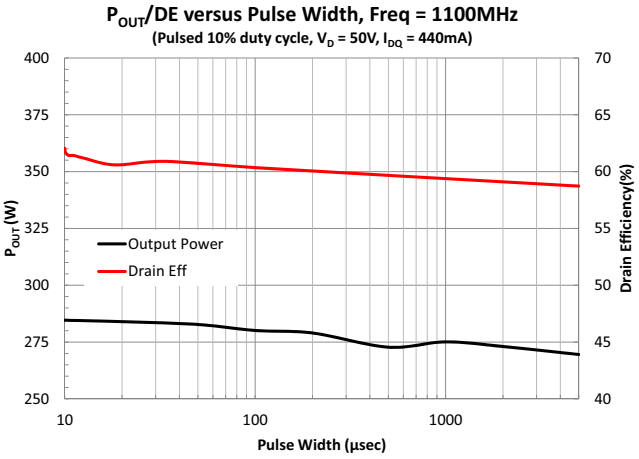
Drain Efficiency versus Frequency, P_{OUT} = 54.5dBm
(Pulsed 10% duty cycle, PW = 100µS, V_D = 50V, I_{DQ} = 440mA)

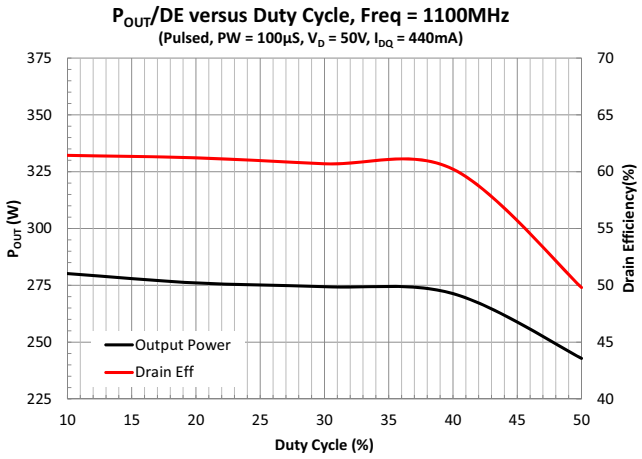


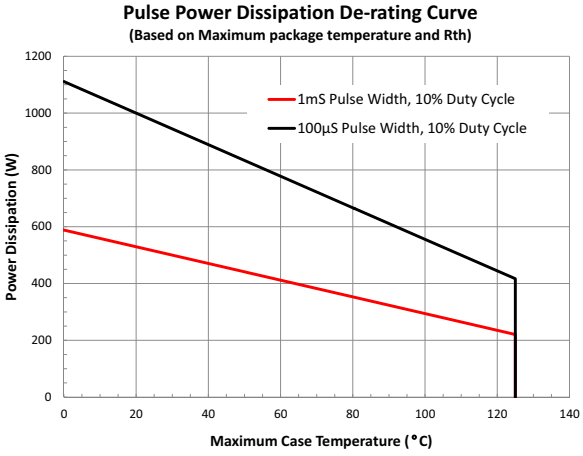
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Typical Performance in Standard Fixed Tuned Test Fixture (T = 25°C, unless noted)



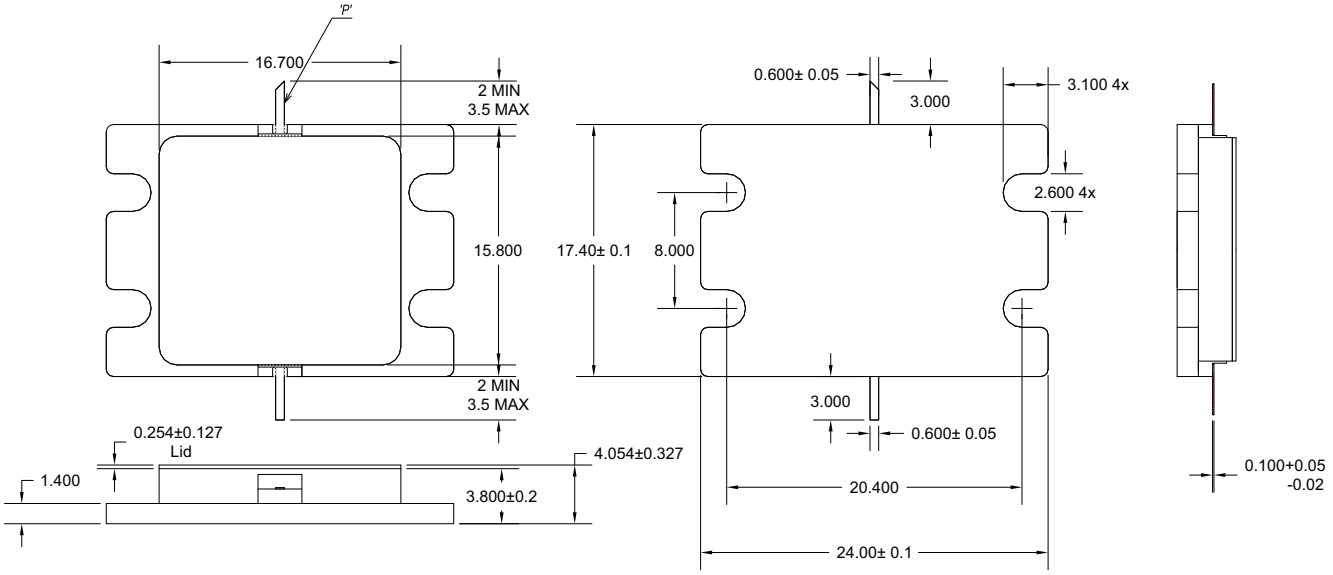






Package Drawing

(All dimensions in mm.)



Pin Names and Descriptions

Pin	Name	Description
1	RF IN VG	Gate – V_G RF Input
2	RF OUT VD	Drain – V_D RF Output
3	GND BASE	Source – Ground Base

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Bias Instruction for RFHA1025 Evaluation Board

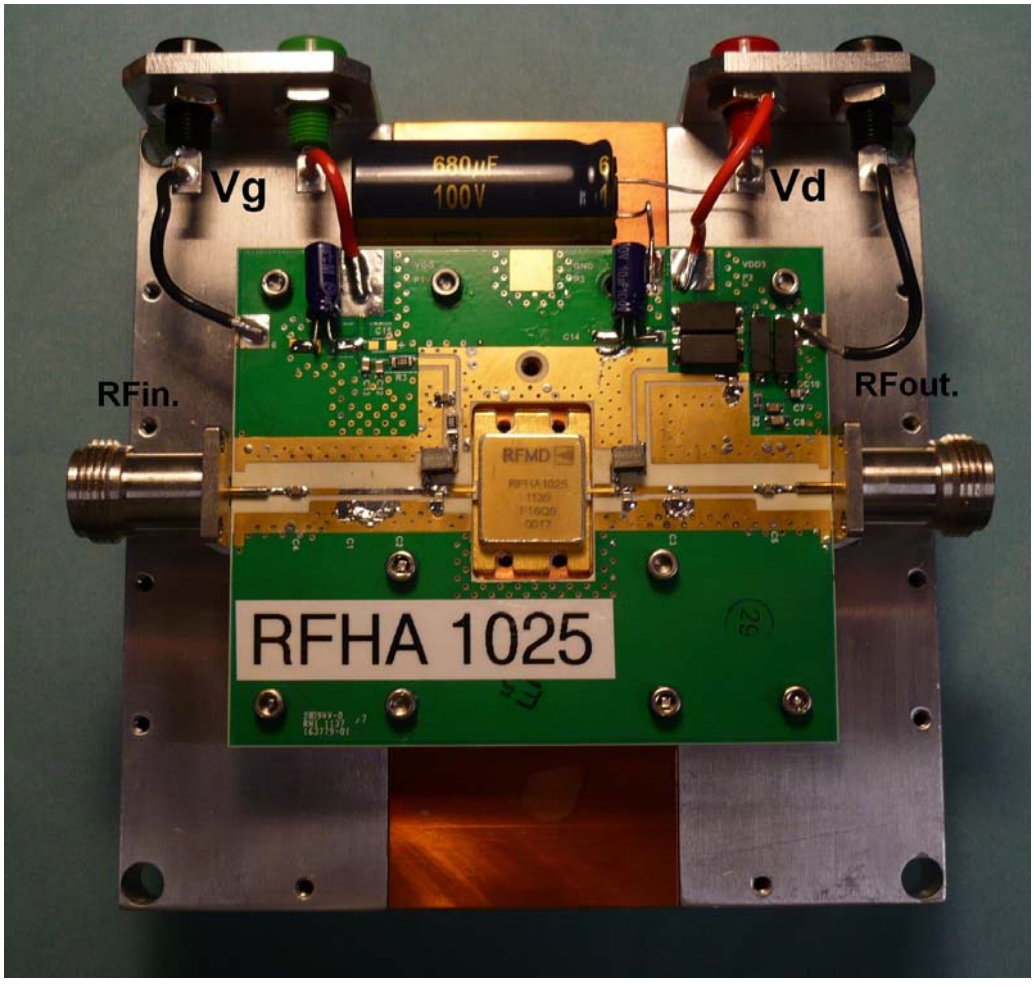
ESD Sensitive Material. Please use proper ESD precautions when handling devices of evaluation board. Evaluation board requires additional external fan cooling. Connect all supplies before powering evaluation board.

1. Connect RF cables at RFIN and RFOUT.
2. Connect ground to the ground supply terminal, and ensure that both the VG and VD grounds are also connected to this ground terminal.
3. Apply -8V to VG.
4. Apply 50V to VD.
5. Increase V_G until drain current reaches 440mA or desired bias point.
6. Turn on the RF input.

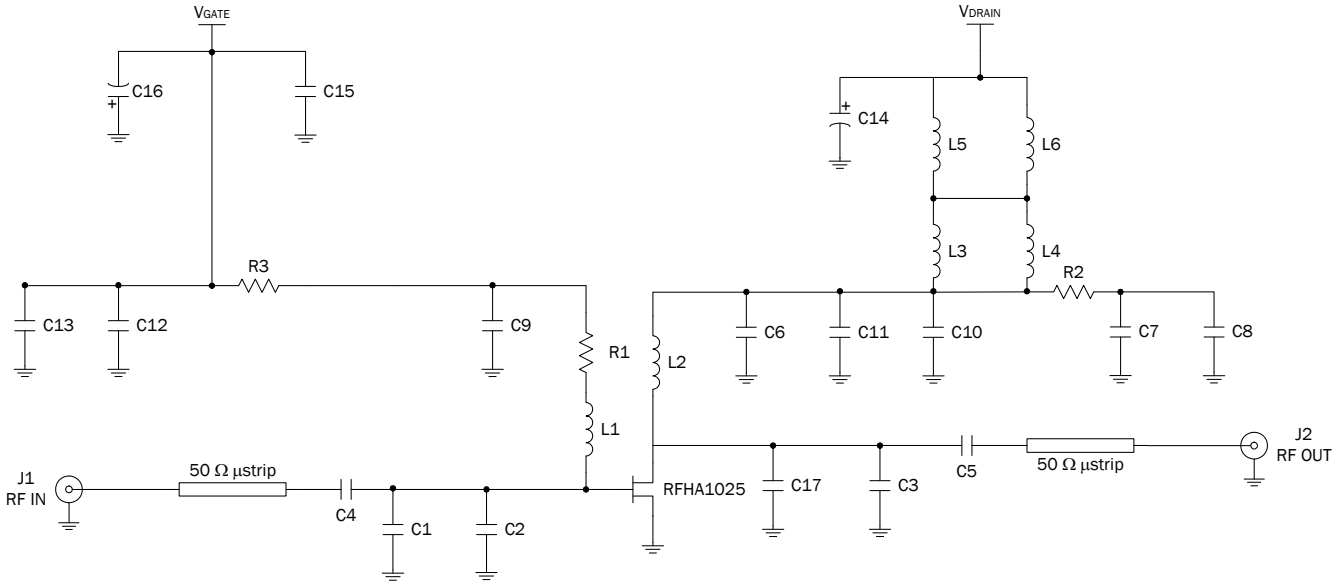
IMPORTANT NOTE: Depletion mode device; when biasing the device, V_G must be applied before V_D. When removing bias, V_D must be removed before V_G is removed. Failure to follow this sequence will cause the device to fail.

NOTE: For optimal RF performance, consistent and optimal heat removal from the base of the package is required. A thin layer of thermal grease should be applied to the interface between the base of the package and the equipment chassis. It is recommended that a small amount of thermal grease is applied to the underside of the device package. Even application and removal of excess thermal grease can be achieved by spreading the thermal grease using a razor blade. The package should then be bolted to the chassis and input and output leads soldered to the circuit board

.



Evaluation Board Schematic

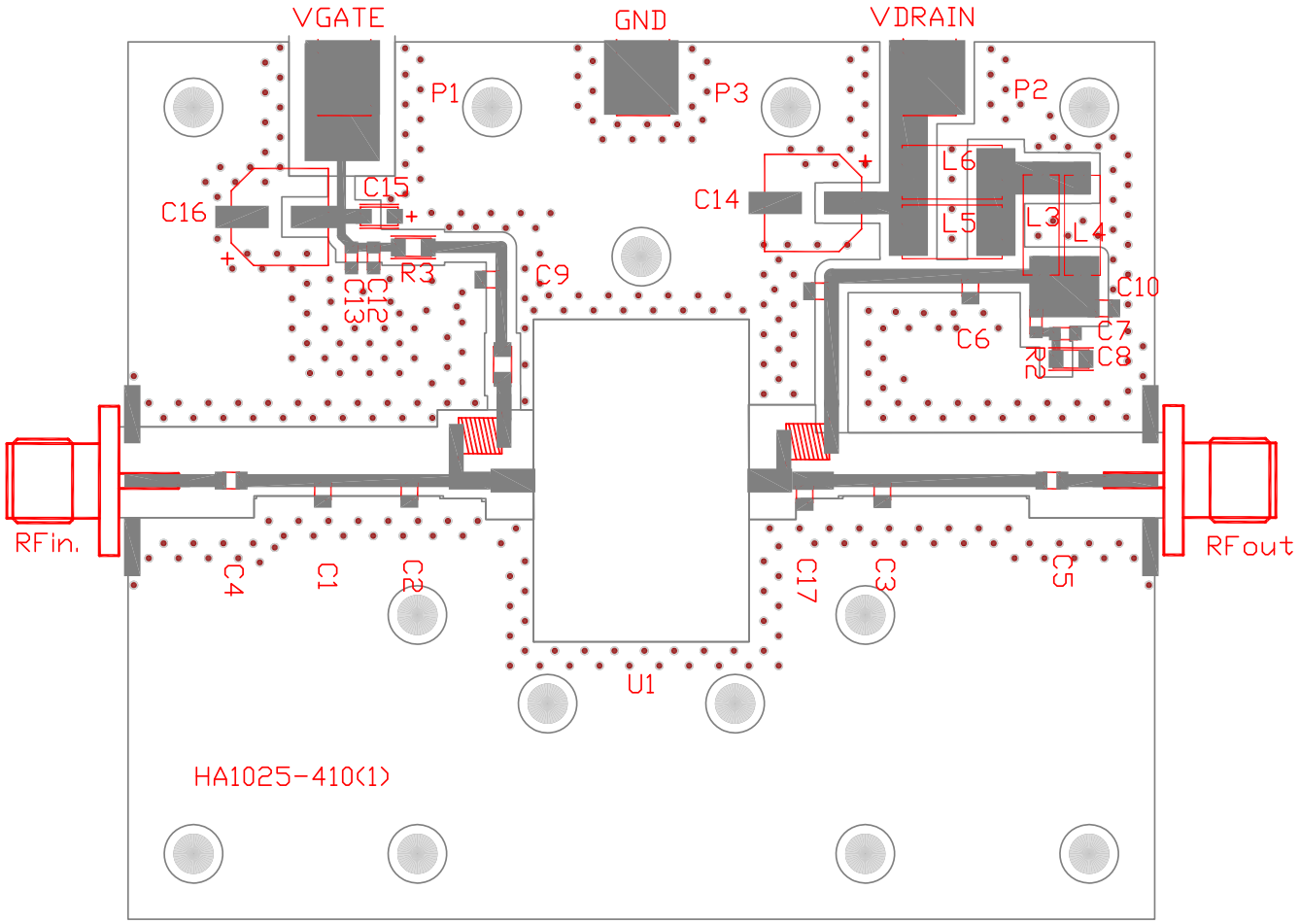


Evaluation Board Bill of Materials

Component	Value	Manufacturer	Part Number
R1,R3	10Ω	Panasonic	ERJ-8GEYJ100V
R2	51Ω	Panasonic	ERJ-8GEYJ510
C6	82pF	ATC	ATC800A820JT
C4, C5, C9, C10	100pF	ATC	ATC800A101JT
C2, C3	2pF	ATC	ATC800A2R0BT
C17	0.2pF	ATC	ATC800A0R2BT
C12	10000pF	Panasonic	ECJ-2VB1H103K
C13	0.1μF	Panasonic	ECJ-2VB1H104K
C7	10000pF	Panasonic	ECJ-2VB2A103K
C8	0.1μF	Panasonic	ECJ-2VB2A104K
C14, C16	10μF	Panasonic	ECA-2AM100
L1,L2	68nH	Coilcraft	1812SMS-68NJLB
L5, L6	115Ω, 10A	Steward	28F0181-1SR-10
L3, L4	75Ω, 10A	Steward	35F0121-1SR-10
C1, C11, C15	NOT POPULATED	-	-

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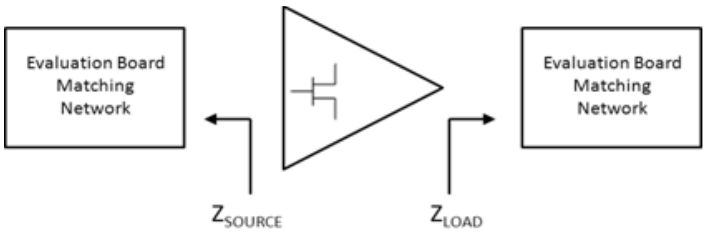
Evaluation Board Layout



Device Impedances

Frequency (MHz)	Z Source (Ω)	Z Load (Ω)
960MHz	68 - j10	63 – j20
1100MHz	55 + j30	65 + j32
1215MHz	30 + j20	40 + j30

NOTE: Device impedances reported are the measured evaluation board impedances chosen for a tradeoff of efficiency and peak power performance across the entire frequency bandwidth.



Device Handling/Environmental Conditions

RFMD does not recommend operating this device with typical drain voltage applied and the gate pinched off in a high humidity, high temperature environment.

GaN HEMT devices are ESD sensitive materials. Please use proper ESD precautions when handling devices or evaluation boards.

GaN HEMT Capacitances

The physical structure of the GaN HEMT results in three terminal capacitors similar to other FET technologies. These capacitances exist across all three terminals of the device. The physical manufactured characteristics of the device determine the value of the C_{DS} (drain to source), C_{GS} (gate to source) and C_{GD} (gate to drain). These capacitances change value as the terminal voltages are varied. RFMD presents the three terminal capacitances measured with the gate pinched off (V_{GS} = -8V) and zero volts applied to the drain. During the measurement process, the parasitic capacitances of the package that holds the amplifier is removed through a calibration step. Any internal matching is included in the terminal capacitance measurements. The capacitance values presented in the typical characteristics table of the device represent the measured input (C_{ISS}), output (C_{OSS}), and reverse (C_{RSS}) capacitance at the stated bias voltages. The relationship to three terminal capacitances is as follows:

$$C_{ISS} = C_{GD} + C_{GS}$$

$$C_{OSS} = C_{GD} + C_{DS}$$

$$C_{RSS} = C_{GD}$$

DC Bias

The GaN HEMT device is a depletion mode high electron mobility transistor (HEMT). At zero volts V_{GS} the drain of the device is saturated and uncontrolled drain current will destroy the transistor. The gate voltage must be taken to a potential lower than the source voltage to pinch off the device prior to applying the drain voltage, taking care not to exceed the gate voltage maximum limits. RFMD recommends applying V_{GS} = -5V before applying any V_{DS}.

RF Power transistor performance capabilities are determined by the applied quiescent drain current. This drain current can be adjusted to trade off power, linearity, and efficiency characteristics of the device. The recommended quiescent drain current (I_{DQ}) shown in the RF typical performance table is chosen to best represent the operational characteristics for this device, considering manufacturing variations and expected performance. The user may choose alternate conditions for biasing this device based on performance tradeoffs.

Mounting and Thermal Considerations

The thermal resistance provided as R_{TH} (junction to case) represents only the packaged device thermal characteristics. This is measured using IR microscopy capturing the device under test temperature at the hottest spot of the die. At the same time, the package temperature is measured using a thermocouple touching the backside of the die embedded in the device heatsink but sized to prevent the measurement system from impacting the results. Knowing the dissipated power at the time of the measurement, the thermal resistance is calculated.

In order to achieve the advertised MTTF, proper heat removal must be considered to maintain the junction at or below the maximum of 200°C. Proper thermal design includes consideration of ambient temperature and the thermal resistance from ambient to the back of the package including heatsinking systems and air flow mechanisms. Incorporating the dissipated DC power, it is possible to calculate the junction temperature of the device.

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