RF6886

3.6V, 100MHz TO 1000MHz LINEAR POWER AMPLIFIER

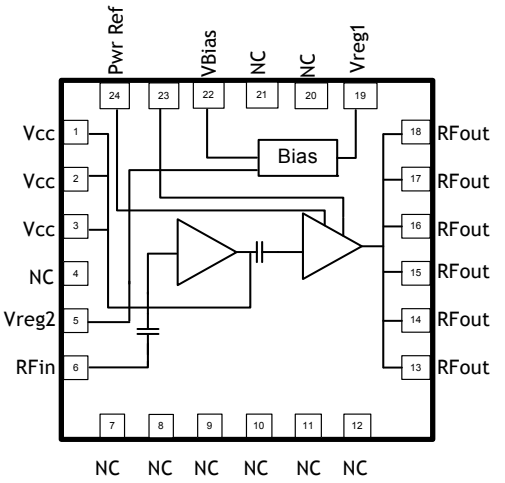
Package: QFN, 24-Pin, 4mmx4mm

Features

- 100MHz to 1000MHz
- Single 3.6V Power Supply
- 34dBm OP1dB
- 36.5dBm Saturated Output Power
- >50% Efficiency

Applications

- CDMA/GSM/EDGE Repeater Final Amplifier
- 450MHz and 865MHz to 955MHz ISM Band Amplifier
- General Purpose High Power Amplifier
- TETRA Handheld/Walkie-Talkie Final Amplifier
- HPA Driver



Functional Block Diagram

Product Description

The RF6886 is a linear, high power, high efficiency amplifier designed to use as a final stage/driver in linear or saturated transmit applications. The device is manufactured on an advanced InGaP HBT process and is provided in a 24-pin leadless chip carrier with backside ground. External matching allows for use in standard bands from 100MHz to 1000MHz.

Ordering Information

RF6886SR	7" Reel with 100 pieces
RF6886SQ	Sample bag with 25 pieces
RF6886TR7	7" Reel with 750 pieces
RF6886TR13	13" Reel with 2500 pieces
RF6886PCK-410	865MHz to 955MHz PCBA with 5-piece sample bag
RF6886PCK-411	433MHz to 470MHz PCBA with 5-piece sample bag

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ BiFET HBT
☑ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
VC2 Collector Quiescent Bias Current (I_{CQ2})	350	mA
VC1 Collector Quiescent Bias Current (I_{CQ1})	150	mA
Maximum Supply Current ($I_{CC1}+I_{CC2}$)	3100	mA
Device Voltage (V_D)	4.0	V
Power Dissipation	5	W
Operating Lead Temperature ($T_{AMBIENT}$)	-40 to +85	°C
Max RF Input 50Ω Output Load	12	dBm
Max RF Output 50Ω Load	38	dBm
Output Load VSWR	See Theory of Operation Section	
Storage Temperature Range	-40 to +150	°C
Operating Junction Temperature (T_J)	150	°C
ESD Rating - Human Body Model (HBM)	Class 1A	V
Moisture Sensitivity Level (MSL)	MSL1	

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Typical Electrical Specifications for 433MHz to 470MHz					See 433MHz to 470MHz Evaluation Board Schematic
Operating Frequency	433	450	470	MHz	V_{CC}=3.6V, V_{REG1}=V_{REG2}=3.1V, I_{CQ} total=390mA
OP1dB		34.5		dBm	
Small SIgnal Gain		33		dB	
Saturated Output Power (P_{SAT})		36.8		dBm	
Saturated Efficiency		55		%	
Saturated Output Power (P_{SAT})		36.3		dBm	V_{CC}=3.3V, V_{REG1}=V_{REG2}=3.1V, I_{CQ} total=380mA
Saturated Efficiency		54.5		%	
Saturated Output Power (P_{SAT})		35.2		dBm	V_{CC}=3.0V, V_{REG1}=V_{REG2}=3.1V, I_{CQ} total=370mA
Saturated Efficiency		53		%	
TETRA ADJ Channel Power		-38		dBc	V_{CC}=3.6V, V_{REG1}=V_{REG2}=2.7V, I_{CQ} total=187mA
TETRA ALT Channel Power		-53		dBc	TETRA: PAR=2.6dB, P_{OUT}=32dBm, 24.3kHz channel BW, ADJ offset=25kHz, ALT offset=50kHz
CDMA ADJ Channel Power		-50		dBc	CDMA: PAR=4.5dB, P_{OUT}=32dBm, 1.23MHz channel BW, ADJ CH offset/BW=750kHz/30kHz, ALT CH offset/BW=1.98MHz/30kHz
CDMA ALT Channel Power		-67		dBc	

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
					See 865MHz to 955MHz Evaluation Board Schematic. T_A=25 °C
Operating Frequency	865	900	955	MHz	V_{CC}=3.6V, V_{REG1}=V_{REG2}=3.1V, I_{CQ} total=390mA
OP1dB		33.5		dBm	
Small SIgnal Gain		31.0		dB	
Saturated Output Power (P_{SAT})		36.2		dBm	
Saturated Efficiency	50	54		%	
Saturated Output Power (P_{SAT})		35.5		dBm	V_{CC}=3.3V, V_{REG1}=V_{REG2}=3.1V I_{CQ} total=380mA
Saturated Efficiency		53.5		%	
Saturated Output Power (P_{SAT})		34.4		dBm	V_{CC}=3.0V, V_{REG1}=V_{REG2}=3.1V I_{CQ} total=370mA
Saturated Efficiency		52.5		%	
CDMA ADJ Channel Power		-52		dBc	CDMA: PAR=4.5dB, P_{OUT}=31.5dBm, 1.23MHz channel BW, ADJ CH offset/BW=750kHz/30kHz, ALT CH offset/BW=1.98MHz/30kHz
CDMA ALT Channel Power		-66		dBc	
Quiescent Current (I_{CQ})	340	390	420	mA	V_{CC}=3.6V, V_{REG1}=V_{REG2}=3.1V
Leakage Current			10	uA	V_{CC}=3.6V, V_{REG1}=V_{REG2}=0V
Current at V_{REG1} and V_{REG2} (I_{REG1} and I_{REG2})		3		mA	V_{CC}=3.6V, V_{REG1}=V_{REG2}=3.1V. $V_{REG1/2}$ supplied through 220Ω bias resistance (see evaluation board schematic).
Thermal Resistance, R_{TH}		11		°C/W	

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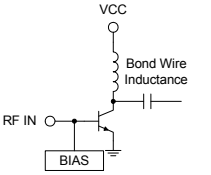
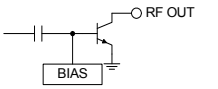
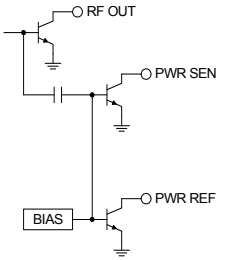
Pin	Function	Description	Interface Schematic
1, 2, 3	VCC1	Inter-stage match and bias for first stage output. Connect inter-stage matching capacitor to pin with a short trace. Connect low frequency bypass capacitor to this pin with a long trace. See evaluation board layout for detail.	
5	VREG2	This pin requires a regulated supply to set output stage DC bias.	
6	RF IN	RF Input. An external blocking capacitor is required if this pin is connected to DC path.	
4, 7-12, 20, 21	NC	No Connect.	
13, 14, 15, 16, 17, 18	RF OUT	RF Output and bias for the output stage. The power supply for the output transistor needs to be supplied to this pin. This can be done through an RF inductor that supports the required DC currents.	
19	VREG1	This pin requires a regulated supply to set driver stage DC bias.	
22	VCC BIAS	Bias circuitry supply voltage.	
23	PWR SENSE	PWR SEN and PWR REF pins can be used in conjunction with an external feedback path to provide an RF power control function for the RF6886. The power control function is based on sampling the RF drive to the final stage of the RF6886.	
24	PWR REF	Same as pin 23.	
Pkg Base	GND	Ground connection. The backside of the package should be connected to the ground plane through a short path, i.e., vias under the device are required.	

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Theory of Operation

This section provides specific guidelines for operation of RF6886.

Applications can generally be placed into two categories:

1. High power applications
   - Output power ranging between 34.5 - 36.5dBm
   - Efficiency >50% in band of interest
2. Linear applications
   - RF6886 shows linearity along the lines of a handset power amplifier in terms of adjacent channel power (ACP) performance, with the distinct advantage of obtaining ACP compliance at >2x comparative output power. Resultant output power for linear operation will depend on the waveform being considered.

All pertinent specifications and performance curves are seen in the tabular and graph sections of the data sheet. The first standard evaluation board has been matched for 865MHz to 955MHz. Operation with V_{CC}=3.6V shows output power >36dBm and efficiency >50%. For reduced power ranges, efficiency is maintained, with no change to output match, by lowering V_{CC}. See data for 3.3/3.0V in the tables provided. The standard evaluation board also demonstrates impressive linearity, shown with conventional CDMA modulation.

The same data set format is also provided for the 433MHz to 470MHz evaluation board. Nominal data is taken with V_{CC}=3.6V and V_{REG1}/2=3.1V. For linear operation, it has been shown that reducing V_{REG1}/2 to 2.7 - 2.8V enhances performance. This can be explained by observing how the compression characteristic behaves. Operation with VREG=3.1V shows gradual (soft) compression once power exceeds 31dBm. With VREG reduced to 2.7 - 2.8V, small signal gain drops by 1 - 2dB. Self bias is now more prominent at 31dBm, and gain expansion offsets slow compression. The result is flattening of the gain characteristic, extending effective compression point out in power. Waveform distortion is reduced as compared to the VREG=3.1V case, and adjacent channel power improves. The sole advantage in using VREG=3.1V would be a slightly higher value for saturated output power.

Low thermal resistance enables reliable high power operation, provided that output load is set to achieve efficiency equal to or better than that seen on the RFMD evaluation boards.

The maximum rating for output load VSWR on page 2 calls out requirement for discussion in this section. RF6886 has shown excellent performance into 50Ω, but any system using it as a final amplifier will have to take VSWR variation into account. Test on properly matched evaluation board has shown that rated output power is obtained with 10dBm at RF input. Practically speaking then, at or near 10dBm would be a maximum reasonable limit for input power. When considering VSWR variation, ruggedness is one of the main considerations. Ruggedness here, being the worse case VSWR which can be tolerated for a transient period without damage to the device. The following maximum VSWR limits apply:

V_{CC}	Freq	P_{OUT} into 50Ω Load (Across Band)	Maximum Practical Input Drive	Maximum Output VSWR (Survival)
V	MHz	dBm	dBm	
3.6	865 to 955	36.2 to 35.2	10	3.5:1
3.3		35.5 to 34.4	10	5.0:1
3		34.4 to 33.4	8	5.0:1
3.6	433 to 470	37 to 36.4	10	3.5:1
3.3		36.3 to 35.6	10	5.0:1
3		35.2 to 34.5	8	5.0:1

In each case, VSWR was tested over phase, with device on/off cycle done several times at phase angle where current was maximum. Test showed that the best off/on sequence for RF6886 is as follows:

Turn on:

1. Apply V_{CC}
2. Apply $V_{REF1/2}$
3. Apply drive at RF input

Turn off:

1. Remove drive at RF input
2. Bring down voltage at $V_{REF1/2}$
3. Bring down V_{CC} (not necessary in system of course)

Many systems will use closed loop power control. When taking output VSWR variation into account, the limits in table above still apply, with same practical maximum limit on RF drive. At some phase angles, higher output powers will not be attainable. Thus, a limit on maximum drive should be taken into account to prevent overdrive of the device by power control circuit.

The VSWR limits set here apply to the most demanding case, where input drive is set for maximum output power. For example, Pout >36dBm, V_{CC}=3.6V, Pin=10dBm. It is entirely conceivable that the amplifier be used in a linear application at backed off power. In that case, it follows that a higher VSWR could be tolerated. As an example, consider 32dBm output power with V_{CC}=3.6V. Test showed that power control loop would achieve 32dBm from 865MHz to 955MHz over phase into 5:1 VSWR. The increased VSWR specification as compared to the 3:5:1 limit in table comes about for the following reason:

The harshest condition is encountered at phase angle where 10dBm drive results in forward power >38.5dBm and current > >3000mA. A power control loop sensing forward (coupled) power would back input drive down in this case and prevent damage. That provided it reacts quickly enough. The more limiting factor in this case, phase angle for lowest power presents a situation where target power cannot be achieved. That even if drive is allowed to go beyond practical maximum. But because the amplifier was seen to achieve 32dBm over phase along with ruggedness, the increased VSWR specification becomes reasonable in the presence of power control and lower output power requirement. So, a multitude of scenarios could exist, with test being required to determine allowable VSWR specification.

Power control can be implemented via several different methodologies, using circuitry external to RF6886. One method already touched upon, sampling forward coupled output power and feedback to adjust at one of two points in the system:

1. With constant drive level at RF6886 input, adjust voltage level at V_{REG1} and/or V_{REG2}. $V_{REG1/2}$ can be tied together, or one of the two can be kept constant with the other adjusted.
2. With $V_{REF1/2}$ constant, RF drive at device input can be adjusted via feedback to a system control point behind RF6886.

Two RF6886 output pins are also available for use in a power control scheme, PWR SENSE (pin 23) and PWR REF (pin 24). Viewing the evaluation board schematics, it can be seen that both pins are tied to V_{CC} through 390Ω resistors. Both pins sink current, resulting in following voltages at respective board connectors:

V_PWR REF = V_{CC} - 390*I_PWR_REF
V_PWR SENSE = V_{CC} - 390*I_PWR_SENSE

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V_PWR_REF output pin yields a voltage proportional to DC component of total output stage drive current, while V_PWR_SENSE output pin does likewise for DC + RF components. Subtraction between these voltages gives result proportional to RF current only, and therefore output power as well. Graphs of Log 10 (V_PWR REF - V_PWR SENSE) vs. RF6886 power out are shown for two scenarios:

1. RF drive at device input = constant 10dBm, with ramp at $V_{REG1/2}$.
2. $V_{REG1/2}$ = constant 3.1V, with RF drive ramp from 0 - 10dBm.

In both cases, it can be seen that output power versus Log of this difference maintains a linear relationship up to 33.5dBm. Non-linear behavior past 33.5dBm is caused by 2 contributors:

1. Compression beginning to take effect at RF6886 1st and/or 2nd stage.
2. PWR_REF and PWR_SENSE transistor collector voltage reduction and associated compression. Note that changing 390Ω value will influence curve shape and shift graphs up/down on y-axis.

As an additional exercise to investigate #2 above, like graphs are shown for 180Ω pull up resistor vs. 390Ω. With 180Ω in place, internal PWR_REF and PWR_SENSE transistors retain higher collector voltage, and do not enter into compression. As a result, we see altered curves as compared to 390Ω case. Log (V_PWR_REF - V_PWR_SENSE) continue to increase, with increasing slope, vs. output power. One other interesting data point, the curve for ramp at $V_{REG1/2}$ now closely resembles that for ramp at RF input.

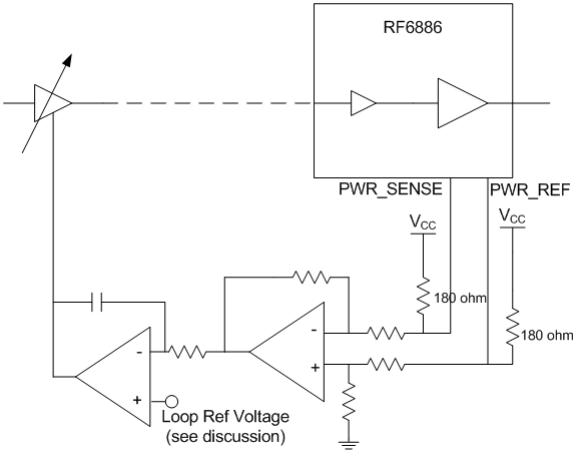
The curves will remain consistent for a given frequency and temperature provided the following remain constant:

1. REF/SENSE resistance (Does not change value in design. This only noted for clarity)
2. Output load VSWR

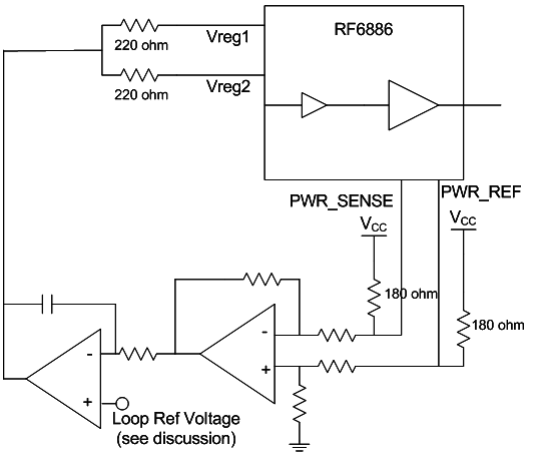
Practically speaking then, this method offers a relatively simple approach, with presumably less accuracy as compared to closed loop control which couples forward power at output. In the coupled power method, VSWR variation will of course also impact accuracy.

Here are general schematics for approaches utilizing PWR_REF/PWR_SENSE pins in described power control schemes:

Approach 1:

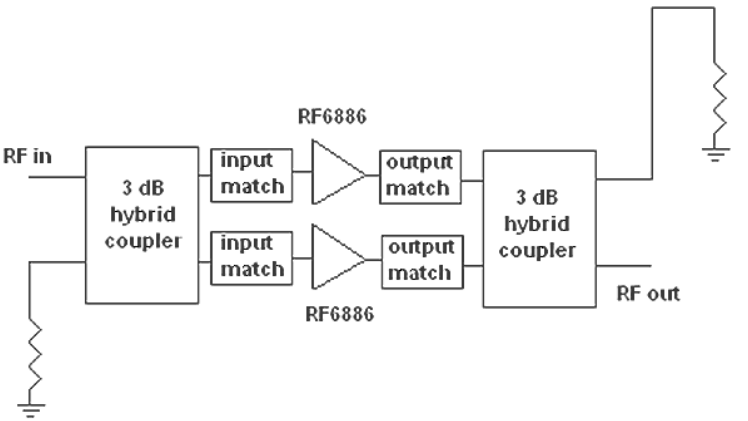


Approach 2:



Approach #1 feeds back to variable gain stage behind RF6886. Approach #2 utilizes feedback to $V_{REG1/2}$ pins of RF6886. Recall Log of the Loop Reference Voltage is shown in graphs for both methods. In the circuits shown above, no Log function is performed. Data for V_delta = (V_PWR_REF - V_PWR_SENSE) vs. Output Power out is collected, and Loop Reference Voltage is set to V_delta(s) for corresponding Output Power(s). Data can be collected at selected frequency and temperature points, depending on accuracy desired in a particular application.

Next, a discussion covering RF6886 used in balanced configuration. The application as depicted here:



This configuration can be implemented with readily available surface mount hybrid couplers, and offers significant performance and reliability advantages. Use single ended RF6886 3.6V specifications for reference:

1. >38.5dBm output power
2. Linear performance with 2.5dB increase in power for equivalent adjacent channel power specification
3. Immunity to antenna VSWR variation

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One key consideration will be output side isolated port 50Ω termination resistance. In the case where output VSWR deviates significantly from 50Ω, reflected power will be absorbed in the isolated port. This will require placement of resistor bank capable of handling power dissipation while fault condition exists.

Finally, consider the maximum allowable operating device voltage, listed at 4.0V in the table on page 2. Operating with V_{CC}=4.0 V enables higher compression point, which becomes attractive in two types of applications:

1. High power, high efficiency
2. Linear, requiring specification compliance at higher power level

Viewing curves in the graph section, it can be seen that device junction temperature stays below 150 °C (85 °C ambient) up to rated power levels. Junction temperature becomes a more critical specification with higher operating voltage. It should be stressed again here that a properly matched output load impedance is required to provide high efficiency. Load impedance has been measured on both standard evaluation boards. The table below contains that data:

Freq	Standard Evaluation Board Load Impedance	Freq	Standard Evaluation Board Load Impedance
MHz	A+jBΩ	MHz	A+jBΩ
865	1.983+j 0.157	433	1.997-j 0.941
900	1.983+j 0.579	450	1.866-j 0.251
928	1.953+j 0.789	470	1.778-j 0.268
955	1.969+j 0.914		

In any application where greater than 3.6V operation is being considered, use of an isolator at RF6886 output is recommended. This, of course, excludes the balanced configuration already discussed. The recommendation would also hold for $V_{CC} \leq 3.6$V, in cases where potential output VSWR conditions exceed those outlined previously in this section.

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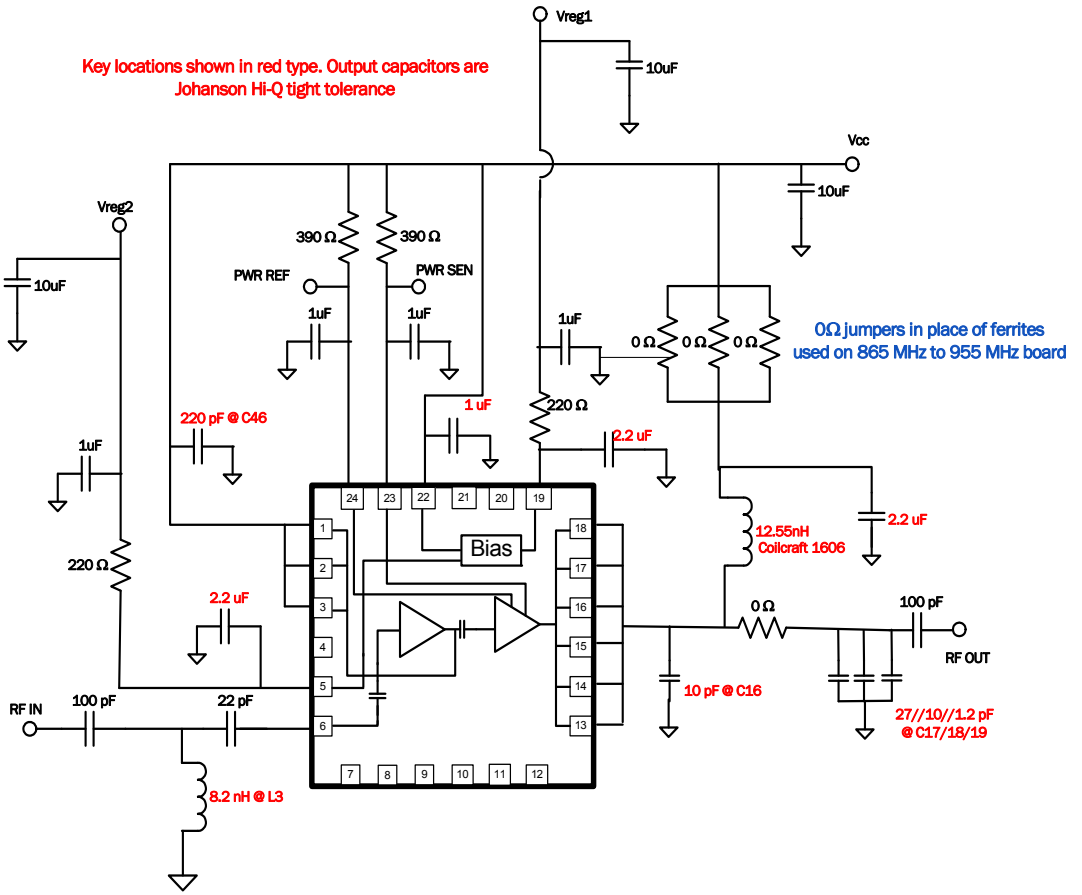
Evaluation Board Schematic

433MHz to 470MHz



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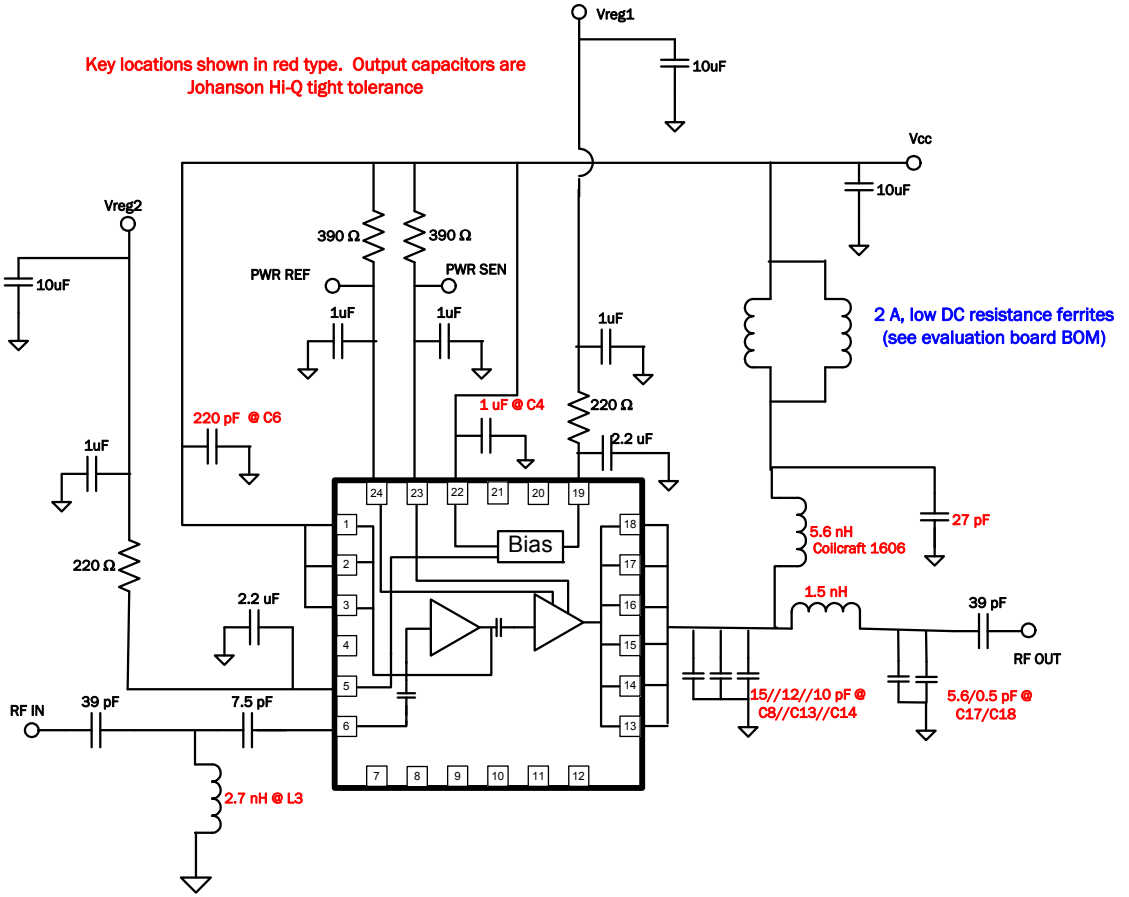
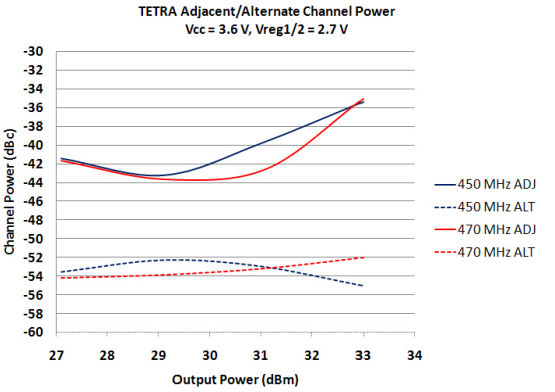
Evaluation Board Schematic

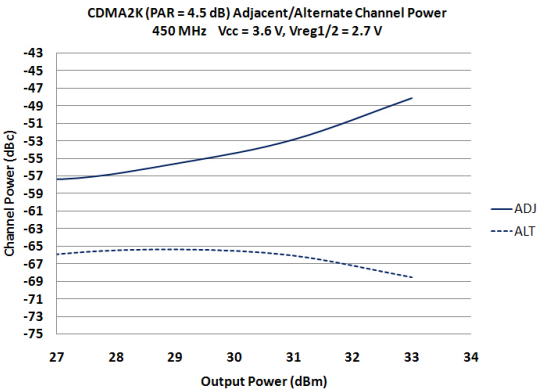
865MHz to 955MHz



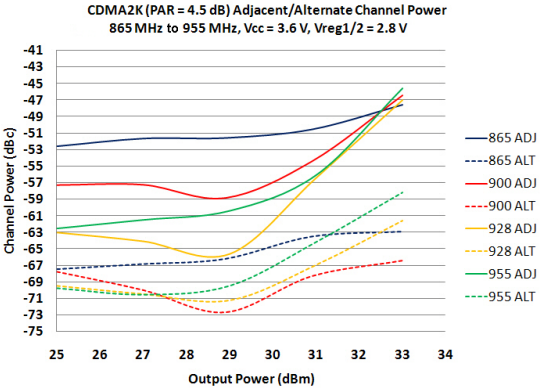
Typical Electrical Performance, 25°C:

433MHz to 470MHz Evaluation Board Schematic





865MHz to 955MHz Evaluation Board



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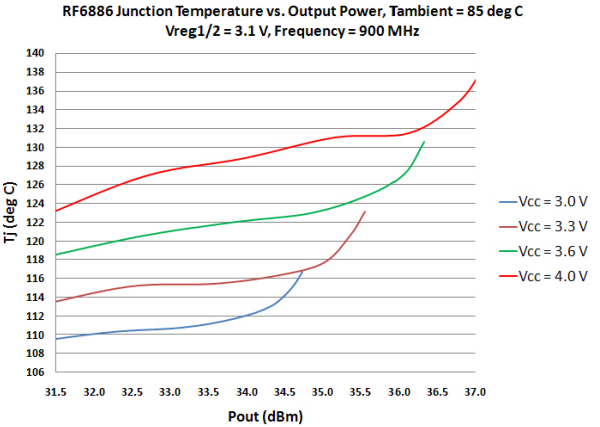
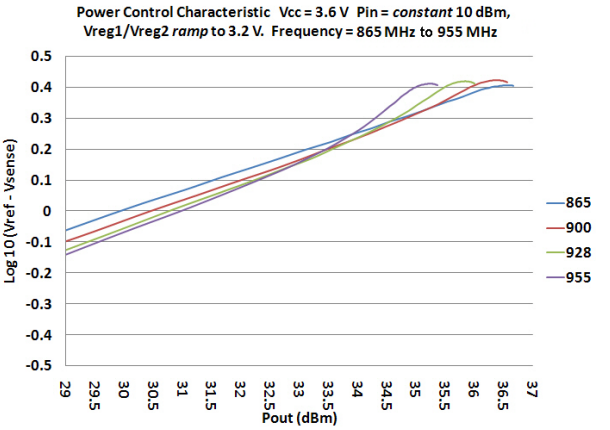
Thermal Performance, 900MHz, 85°C:

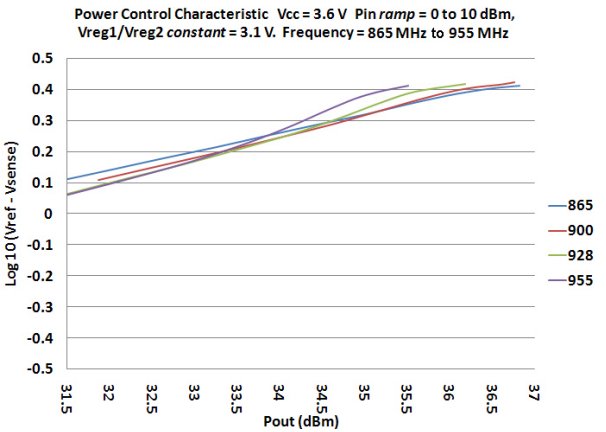


Power Control Performance, REF/SENSE Pull-Up Resistance=390Ω, 25°C:

865MHz to 955MHz Evaluation Board, Constant Power at RF IN, Ramp at $V_{REG1/2}$



865MHz to 955MHz Evaluation Board, Power Ramp at RF IN, Constant 3.1V at $V_{REG1/2}$



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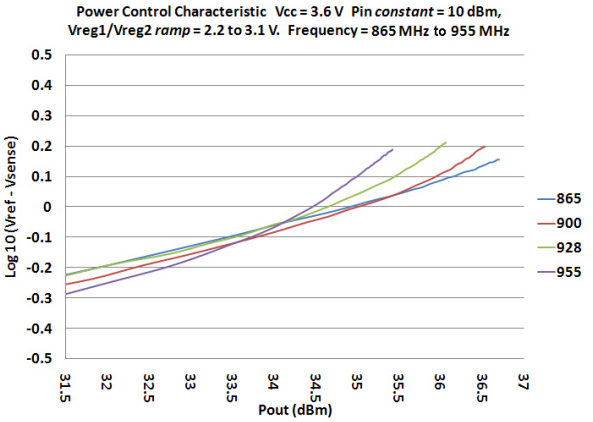
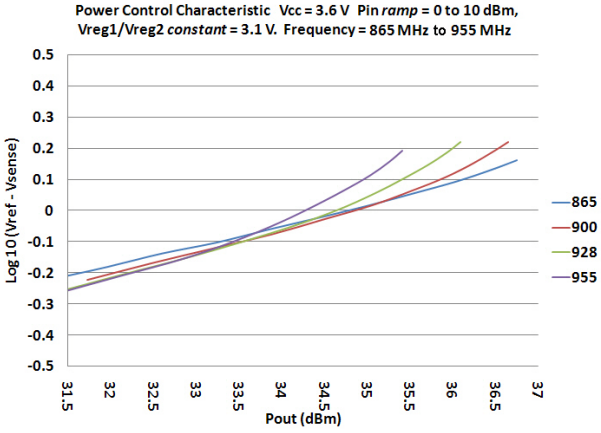
Power Control Performance, REF/SENSE Pull-Up Resistance=180Ω, 25°C:

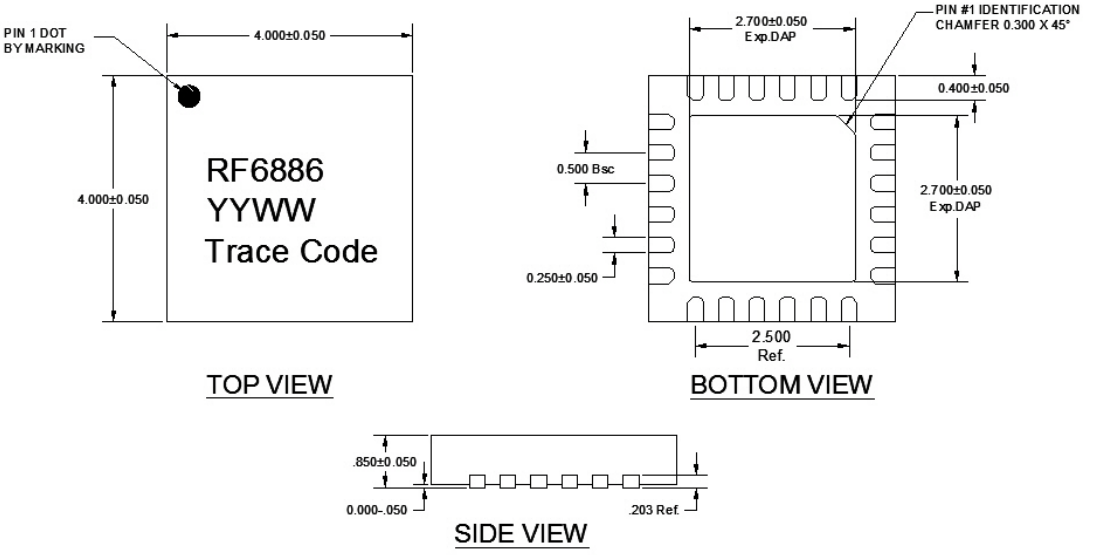
865MHz to 955MHz Evaluation Board, Constant Power at RF IN, Ramp at $V_{REG1/2}$



865MHz to 955MHz Evaluation Board, Power Ramp at RF IN, Constant 3.1V at $V_{REG1/2}$



Package Drawing



YYWW = Date Code, where YY=year, WW=week

Trace Code to be assigned by assembly SubCon

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