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RF5189

3V, 2.45GHz LINEAR POWER AMPLIFIER

RoHS Compliant & Pb-Free Product
Package Style: QFN, 12-Pin, 3 x 3

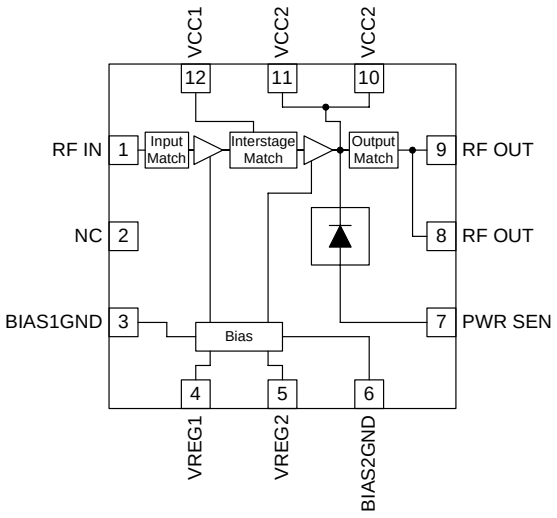


Features

- Single Power Supply 3.0V to 5.0V
- +30dBm Saturated Output Power
- 25dB Small Signal Gain
- High Linearity
- 2400MHz to 2500MHz Frequency Range

Applications

- IEEE802.11B WLAN Applications
- 2.5GHz ISM Band Applications
- Wireless LAN Systems
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment
- Spread-Spectrum and MMDS Systems



Functional Block Diagram

Product Description

The RF5189 is a linear, medium-power, high-efficiency amplifier IC designed specifically for battery-powered WLAN applications such as PC cards, mini PCI, and compact flash applications. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 2.5GHz WLAN and other spread-spectrum transmitters. The device is provided in a 12-pin QFN package with a backside ground. The RF5189 is designed to maintain linearity over a wide range of supply voltage and power output. The RF5189 is designed to reduce end-product BOM count by integrating all matching circuitry onto the chip.

Ordering Information

RF5189	3V, 2.45GHz Linear Power Amplifier
RF5189PCBA-41X	Fully Assembled Evaluation Board

Optimum Technology Matching® Applied

☑ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	
☐ InGaP HBT	☐ SiGe HBT	☐ Si BJT	

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +6.0	V_{DC}
Power Control Voltage (V_{REG})	-0.5 to 3.5	V
DC Supply Current	600	mA
Input RF Power	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Moisture sensitivity	JEDEC Level 2	

Caution! ESD sensitive device.

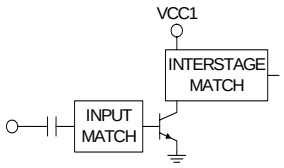
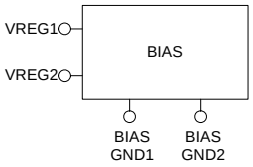
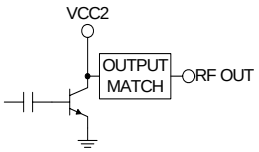
Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

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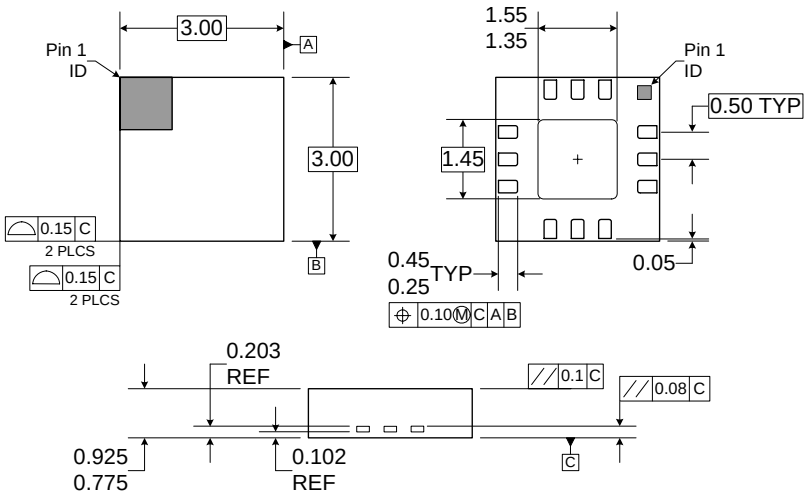
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall-11b Signal					T=25 °C, V_{CC}=3.0V, V_{REG}=2.7V, Freq=2450MHz
Frequency Range		2400 to 2500		MHz	
Maximum Linear Output Power					With 802.11B modulation (11Mbit/s) and meeting 802.11B spectral mask.
V_{CC}=3.0V	21	22		dBm	
V_{CC}=5.0V	24			dBm	
Linear Efficiency		24		%	
Small Signal Gain	23	25	27	dB	P_{IN}=-7dBm
Second Harmonic			-35	dBc	
802.11B Adjacent Channel Power		-38	-32	dBc	P_{OUT}=21dBm, V_{CC}=3.0V
Alternate Channel Power		-56	-52	dBc	P_{OUT}=21dBm, V_{CC}=3.0V
Isolation		30		dB	In "OFF" state, P_{IN}=-5.0dBm
Input Return Loss	9.5	15.0		dB	50Ω reference
Output VSWR	2:1	1.5:1			50Ω reference
Power Detect Voltage	1.7	2.1	2.4	V	P_0=21dBm
Power Down					
V_{REG} "ON"	2.1	2.7	3.0	V	Voltage supplied to control input; device is "ON"
V_{REG} "OFF"		0	0.5	V	Voltage supplied to control input; device is "OFF"
Power Supply					
Operating Voltage		3.0 to 5.0		V	
Current Consumption			10	μA	V_{REG}=0V
		100	160	mA	No RF input, V_{CC}=3.0V, and V_{REG}=2.7V
		220	270	mA	P_{OUT}=21dBm, V_{CC}=3.0V, and V_{REG}=2.7V
V_{REG} Current (Total)		5	10	mA	V_{CC}=3.0V
		10	15	mA	V_{CC}=5.0V

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Pin	Function	Description	Interface Schematic
1	RF IN	RF input. Input is matched to 50Ω and DC block is provided internally.	
2	NC	No connect. Recommend connecting to ground.	
3	BIAS1GND	Ground for first stage bias circuit. For best performance, keep traces physically short and connect immediately to ground plane.	See pin 4.
4	VREG1	First stage input bias. This pin requires a regulated supply to maintain nominal bias current.	
5	VREG2	Second stage input bias. This pin requires a regulated supply to maintain nominal bias current. Usually connected to VREG1.	See pin 4.
6	BIAS2GND	Ground for second stage bias circuit. For best performance, connect to ground with a choke inductor.	See pin 4.
7	PWR SEN	Provides an output voltage proportional to output RF level.	
8	RF OUT	RF output. Output is matched to 50Ω and DC block is provided internally.	
9	RF OUT	Same as pin 8.	See pin 8.
10	VCC2	Second stage output bias. Supply should be connected through a choke inductor sized appropriately to handle the output bias current.	See pin 8.
11	VCC2	Same as pin 10.	See pin 8.
12	VCC1	First stage output bias. This pin is sensitive to bypass capacitors placed close to it. Place an RF short approximately 200mils from this pin before any other supply connections.	See pin 1.
Pkg Base	GND	Ground connection. The backside of the package should be connected to the ground plane through a short path (i.e., vias under the device will be required).	

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Package Drawing



Dimensions in mm.

Shaded areas represent pin 1.

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Theory of Operation

The RF5189 is a two-stage device with a nominal gain of 25dB in the 2.4GHz to 2.5GHz ISM band. The RF5189 is designed primarily for IEEE802.11B WLAN applications where the available supply voltage and current are limited. This amplifier will operate to (and below) the lowest expected voltage made available by a typical PCMCIA slot in a laptop PC, and will maintain required linearity at decreased supply voltages.

The RF5189 requires only a single positive supply of 3.0V nominal (or greater) to operate to full specifications. Power control is provided through two bias control input pins (VREG1 and VREG2), but in most applications these are tied together and used as a single control input.

There is no external matching required on the input and output of the part, thus allowing minimal bill of material (BOM) parts count in end applications. Both the input and the output of the device are DC-blocked.

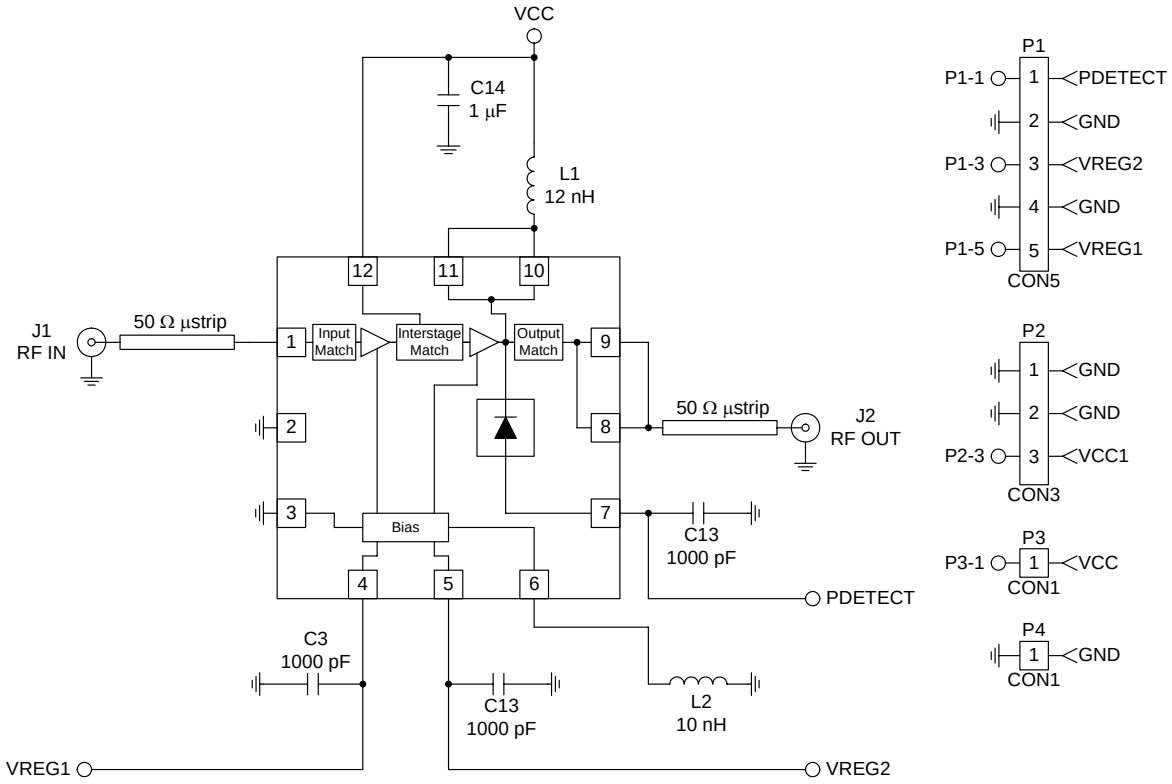
For best results, the PA circuit layout from the evaluation board should be copied as closely as possible, particularly the ground layout and ground vias. Other configurations may also work, but the design process is much easier and quicker if the layout is copied from the RF5189 evaluation board. Gerber files of our designs are available on request.

The RF5189 is not a difficult part to implement, but care in circuit layout and component selection is always advisable when designing circuits to operate at 2.5GHz. The choke inductors on VCC2 and BIAS2GND should be chosen so that they are parallel self-resonant at the frequency of operation. In addition, the supply side of the choke inductor on VCC2 should be bypassed with a capacitor that is series self-resonant at the frequency of operation.

In practice, VCC1 and the supply side of the choke on VCC2 will be tied to the same supply. It is important to isolate VCC1 from other RF and low-frequency bypass capacitors on this supply line. This can be accomplished using a suitably-long transmission line which is RF shorted on the other end as described above. Ideally the length of this line will be a quarter wavelength, but it only needs to be long enough so that the effects of other supply bypass capacitors on the VCC1 line are minimized. If board space is a concern, this isolation can also be accomplished with an RF choke inductor or ferrite bead.

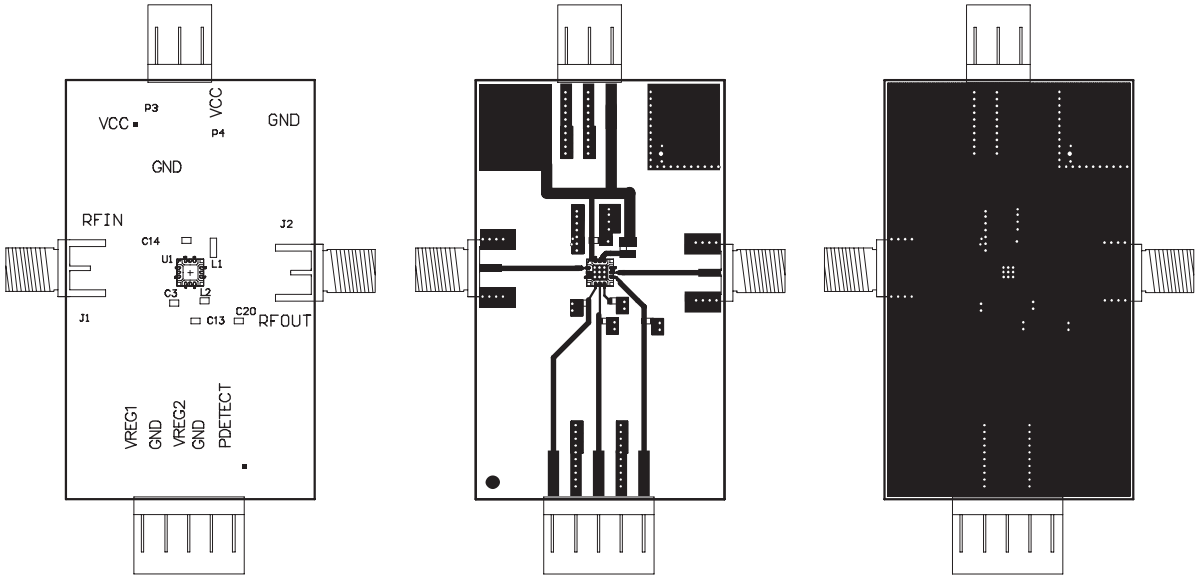
The RF5189 has primarily been characterized with a voltage on VREG1 and VREG2 of 2.7V_{DC}. However, the RF5189 will operate from a wide range of control voltages. If you prefer to use a control voltage that is significantly different than 2.7V_{DC}, contact RFMD Sales or Applications Engineering for additional data and guidance.

Evaluation Board Schematic

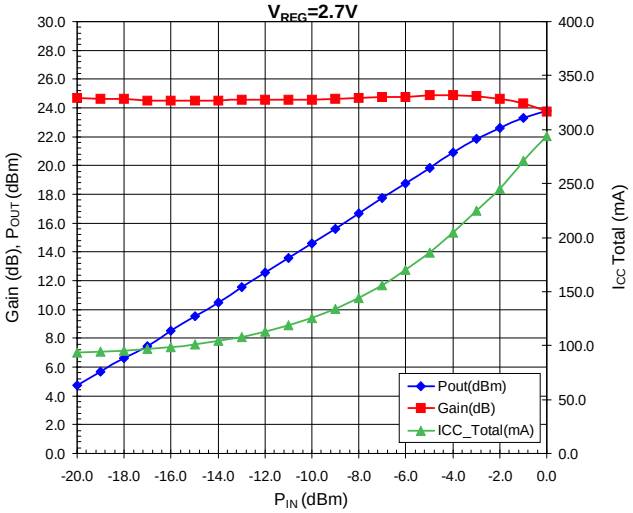


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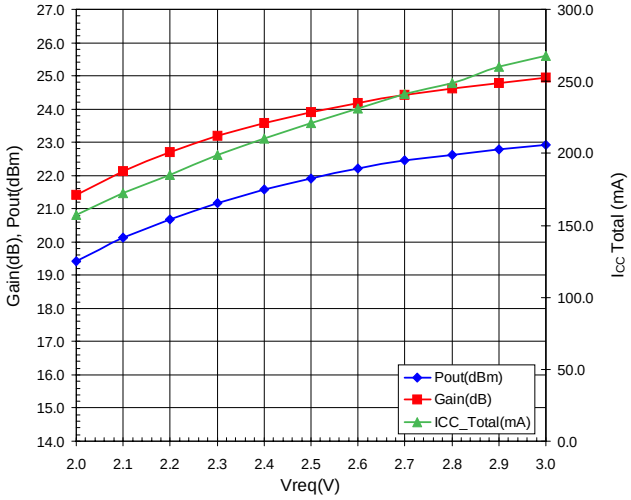
Evaluation Board Layout
Board Size 1.10" x 1.85"
Board Thickness 0.032", Board Material FR-4



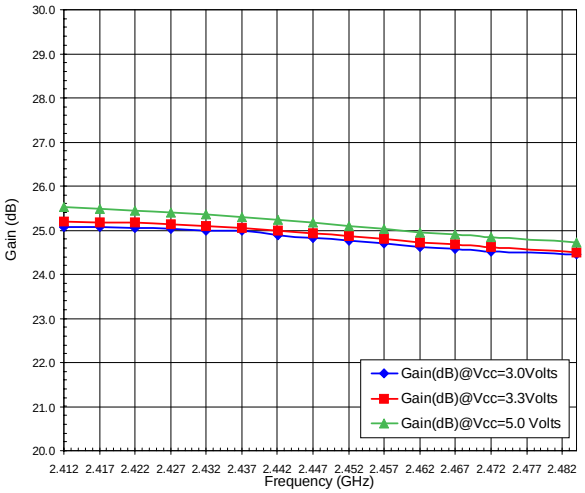
P_{OUT}, Gain, I_{CC} Total versus P_{IN} (Typical) @ V_{CC}=3.0V, V_{REG}=2.7V



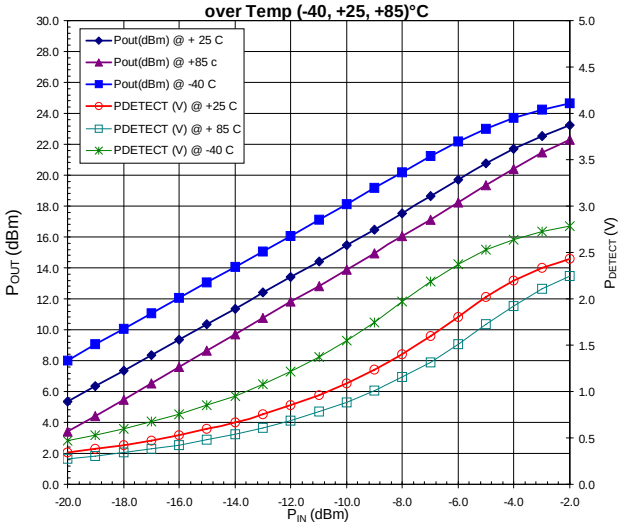
P_{OUT}, Gain, I_{CC} Total versus V_{REG} @ V_{CC}=3.0V



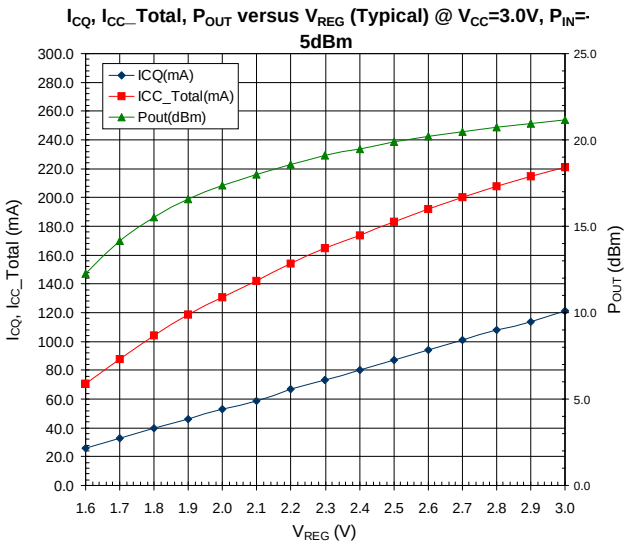
Channel Frequency versus Gain (Typical) for V_{CC}=3.0V, 3.3V, and 5.0V, V_{REG1}=V_{REG2}=2.7V and P_{OUT}=21dBm



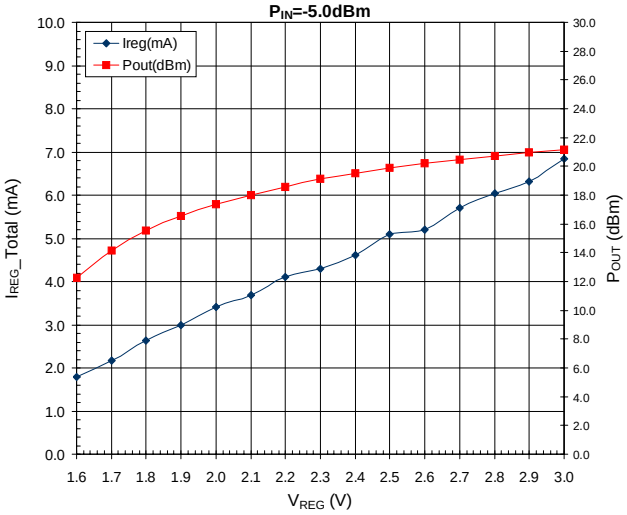
P_{OUT}, P_{DETECT} versus P_{IN} (Typical) @ V_{CC}=3.0, V_{REG}=2.7 over Temp (-40, +25, +85)°C



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I_{CQ}, I_{CC}_Total, P_{OUT} versus V_{REG} (Typical) @ V_{CC}=3.0V, P_{IN}=-5dBm



I_{REG}, P_{OUT} versus V_{REG} (Typical) @ V_{CC}=3.0V, P_{IN}=-5.0dBm

Spectral Mask (Typical): V_{CC}=3.0V, V_{REG1}=V_{REG2}=2.7V, P_{OUT}=18dBm, P_{IN}=-7.55dBm, and I_{CC}_Total=168mA

Spectral Mask (Typical): V_{CC}=3.0V, V_{REG1}=V_{REG2}=2.7V, P_{OUT}=21dBm, P_{IN}=-4.0dBm, and I_{CC}_Total=210mA

PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns are based on IPC-SM-782 standards when possible. The pad pattern shown has been developed and tested for optimized assembly at RFMD; however, it may require some modifications to address company specific assembly processes. The PCB land pattern has been developed to accommodate lead and package tolerances.

PCB Metal Land Pattern

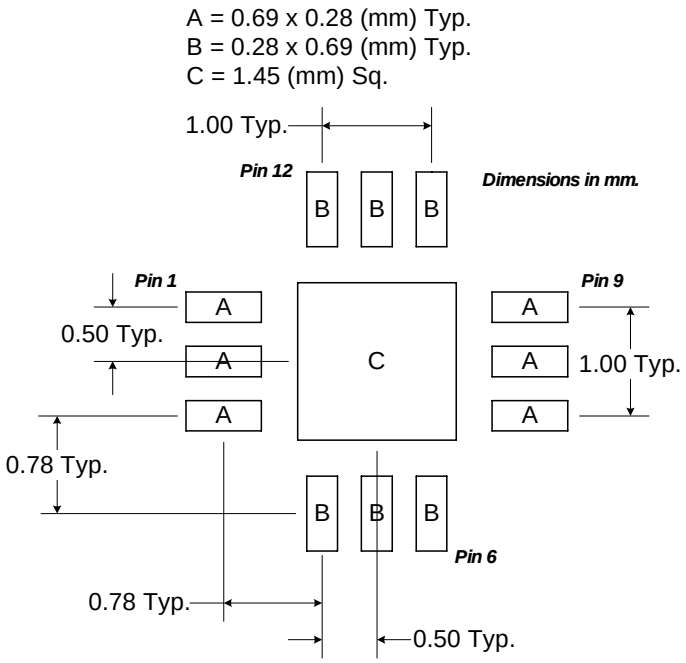


Figure 1. PCB Metal Land Pattern (Top View)

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PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB Metal Land Pattern with a 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

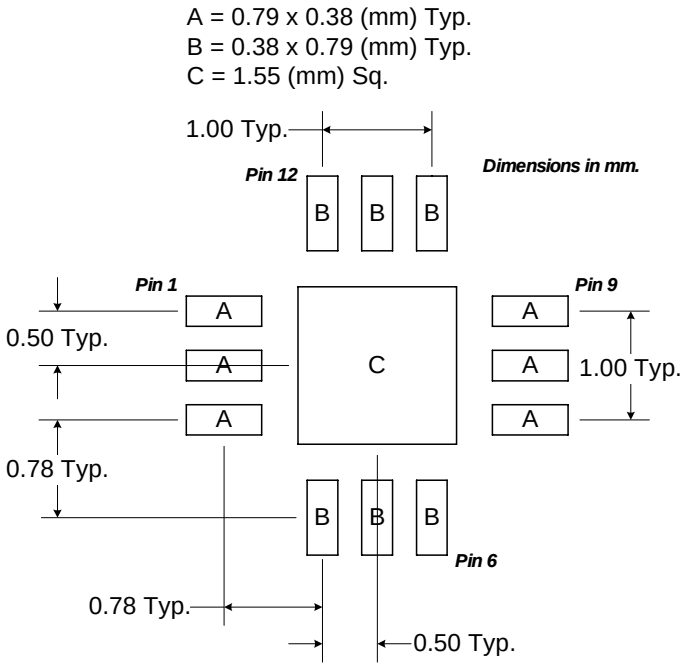


Figure 2. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB Metal Land Pattern has been designed with a thermal pad that matches the exposed die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

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