RF5112

3V TO 5V, 2.4GHz TO 2.5GHz LINEAR POWER AMPLIFIER

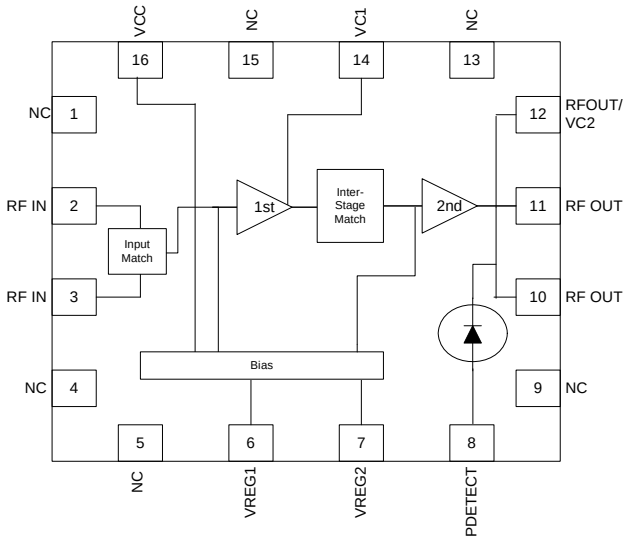
Package Style: QFN, 16-Pin, 3mmx3mmx0.9mm

Features

- Single Power Supply 3.0V to 5.0V
- +23dBm, <4% EVM, 250mA at V_{CC}=5.0V
- +21dBm, <4.0% EVM, 185mA at V_{CC}=3.3V
- 28dB Typical Small Signal Gain
- 50Ω Input and Interstage Matching
- 2400MHz to 2500MHz Frequency Range

Applications

- IEEE802.11b/g/n WiFi Applications
- 2.5GHz ISM Band Applications
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment
- Spread-Spectrum and MMDS Systems



Functional Block Diagram

Product Description

The RF5112 is a linear, medium-power, high-efficiency, two-stage amplifier IC designed specifically for battery-powered WiFi applications such as PC cards, mini PCI, and compact flash applications. The device is manufactured on an advanced InGaP Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in 2.5GHz OFDM and other spread-spectrum transmitters. The device is provided in a 3mmx3mmx0.9mm, 16-pin, QFN with a backside ground. The RF5112 is designed to maintain linearity over a wide range of supply voltage and power output.

Ordering Information

RF5112	Standard 25 piece bag
RF5112SR	Standard 100 piece reel
RF5112TR7	Standard 2500 piece reel
RF5112WL50PCK-41X	Fully Assembled Evaluation Board Kit (5.0V Tune)
RF5112WL33PCK-41X	Fully Assembled Evaluation Board Kit (3.3V Tune)

Optimum Technology Matching® Applied

☐ GaAs HBT	☐ SiGe BiCMOS	☐ GaAs pHEMT	☐ GaN HEMT
☐ GaAs MESFET	☐ Si BiCMOS	☐ Si CMOS	☐ RF MEMS
☑ InGaP HBT	☐ SiGe HBT	☐ Si BJT	☐ LDMOS

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	6.0	V
Power Control Voltage (V_{REG})	3.3	V
DC Supply Current	500	mA
Input RF Power	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C
Moisture Sensitivity	MSL2	

Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

RoHS status based on EUDirective2002/95/EC (at time of this document revision).

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Compliance					IEEE802.11b/g IEEE802.11n**
Typical Conditions					Temp=25°C, V_{REG} 1 and 2=2.85V, Freq=2.4Ghz to 2.5GHz, Duty Cycle=1 to 100% unless otherwise noted.
Frequency	2.40		2.5	GHz	
Output Power	TBD	21		dBm	V_{CC}=3.3V, V_{REG}=2.85V, 54Mbps, OFDM modulation
EVM		3.3	4.0	%	V_{CC}=3.3V, P_{OUT}=21dBm
Adjacent Channel Power					
ACP1		-34	-30	dBc	V_{CC}=3.3V, V_{REG}=2.85V, P_{OUT}=23.5dBm measured with the standard IEEE802.11b wave form at 1Mbps.
ACP2		-54	-50	dBc	V_{CC}=3.3V, V_{REG}=2.85V, P_{OUT}=23.5dBm measured with the standard IEEE802.11b wave form at 1Mbps.
Output Power	TBD	23		dBm	V_{CC}=5V, V_{REG}=2.85V, 54Mbps, OFDM modulation
EVM		3.3	4.0	%	P_{OUT}=23dBm, RMS, mean
Adjacent Channel Power					
ACP1		-34	-30	dBc	V_{CC}=5.0V, V_{REG}=2.85V, P_{OUT}=23.5dBm measured with the standard IEEE802.11b wave form at 1Mbps.
ACP2		-54	-50	dBc	V_{CC}=5.0V, V_{REG}=2.85V, P_{OUT}=23.5dBm measured with the standard IEEE802.11b wave form at 1Mbps.
Harmonics					
$2F_0$		-17	TBD	dBm/MHz	Measured at V_{CC}=3.3V, V_{REG}=2.85V at P_{OUT}=23dBm with 11b waveform at 1Mbps
$3F_0$		-35	TBD	dBm/MHz	Measured at V_{CC}=3.3V, V_{REG}=2.85V at P_{OUT}=23dBm with 11b waveform at 1Mbps
Harmonics					
$2F_0$		-7	TBD	dBm/MHz	Measured at V_{CC}=5.0V, V_{REG}=2.85V at P_{OUT}=25dBm with 11b waveform at 1Mbps
$3F_0$		-47	TBD	dBm/MHz	Measured at V_{CC}=5.0V, V_{REG}=2.85V at P_{OUT}=25dBm with 11b waveform at 1Mbps

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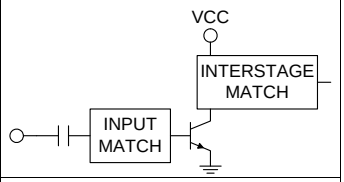
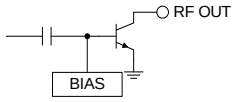
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Input return loss		-10		dB	
Gain	27.5	29	TBD	dB	At both V_{CC}=3.3V and 5.0V
Gain Variance			0.75	±dB	-40°C to +85°C
Power Detector (P_detect)	0.1		1.3	V	For P_{OUT}=0dBm to 23dBm with V_{CC}=3.3V, 11b
	0.1		2.5	V	For P_{OUT}=0dBm to 25dBm with V_{CC}=5.0V, 11b
Current					
Operating		185	TBD	mA	V_{CC}=3.3V, P_{OUT}=+21dBm
		250	TBD	mA	V_{CC}=5.0V, P_{OUT}=23dBm
Quiescent		95	TBD	mA	RF=OFF, V_{CC}=3.3V
		TBD	TBD	mA	RF=OFF, V_{CC}=5.0V
I_{REG}			10	mA	
Shutdown			10	μA	
Current					
Operating		100	TBD	mA	at +18dBm RF P_{OUT} and 54Mbps datarate at <2% EVM RMS, mean
Quiescent		75		mA	at +18dBm RF P_{OUT} and 54Mbps datarate at <2% EVM RMS, mean
I_{REG}			10	mA	at +18dBm RF P_{OUT} and 54Mbps datarate at <2% EVM RMS, mean
Shutdown			10	μA	at +18dBm RF P_{OUT} and 54Mbps datarate at <2% EVM RMS, mean
Power Supply	3.0	3.3	5	V_{DC}	Operating
V_{REG1}, V_{REG2} Input Voltage	2.75	2.85	3.0	V_{DC}	Operating
V_{REG1}, V_{REG2} Current					
		5	10	mA	V_{CC}=+3.3V_{DC}
		5	10	mA	V_{CC}=+5.0V_{DC}
Output VSWR			10:1		
Input Return Loss		-15	-10	dB	
Turn-on time*		.5	1.0	uSec	Output stable to within 90% of final gain

Pin	Function	Description	Interface Schematic
1	NC	Not connected. May be connected to ground (GND).	
2	RF IN	RF input. See evaluation board schematic for details.	
3	RF IN	RF input. See evaluation board schematic for details.	See pin 2.
4	NC	Not connected. May be connected to ground (GND).	
5	NC	Do not connect. **Note:** VCC voltage may be applied to this pin without damage to, or affecting the performance of, the RF5112.	
6	VREG1	Bias current control voltage for the first stage.	
7	VREG2	Bias current control voltage for the second stage. The VREG2 pin may be connected to VREG1 through an external resistor bridge.	
8	PDETECT (or N/C*)	Provides an output voltage proportional to the output RF level. *In applications where the PDETECT function is not desired, this pin may be left unconnected.	
9	NC	No-connect.	
10	RF OUT	RF output.	
11	RF OUT	Same as pin 10.	See pin 10.
12	VCC2	Power supply for second stage amplifier. Connect as shown on evaluation board schematic.	
13	NC	Not connected. May be connected to ground (GND).	
14	VCC1	Power supply for first stage amplifier. Connect as shown on evaluation board schematic.	
15	NC	Not connected. May be connected to ground (GND).	
16	VCC B	Supply voltage for the bias reference and control circuits. May be connected with VC1 and VC2 (single-supply voltage).	
Pkg Base	GND	The center metal base of the QFN package provides DC and RF ground as well as heat sink for the amplifier.	

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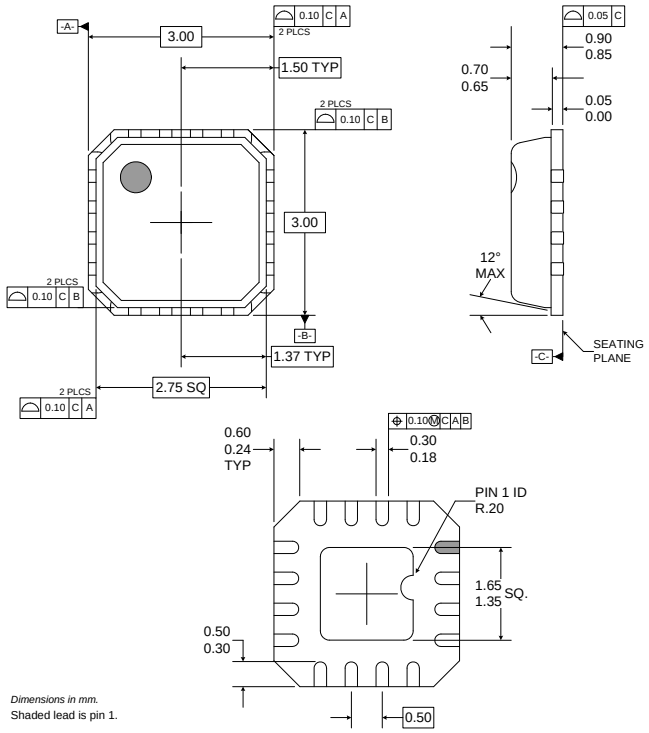
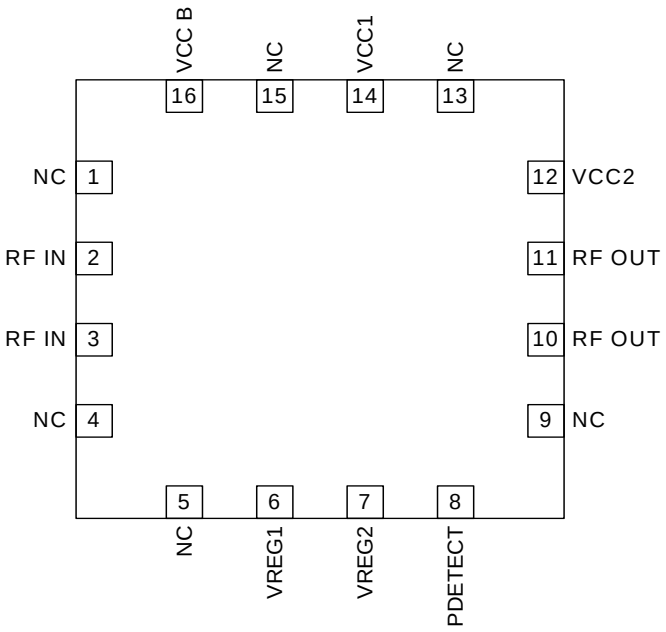
Package Drawing



Pin Out



Theory of Operation and Application Information

The RF5112 is a two-stage Power Amplifier designed primarily for IEEE802.11g/n WiFi applications where the available supply voltage and current are limited. This PA has a minimum gain of 28dB (29.5dB typical) in the 2.4GHz to 2.5GHz ISM band. The RF5112 has an integrated input and interstage match to 50Ω. Only the output stage requires matching. This amplifier will operate to and below the lowest expected voltage made available by a typical CardBus or PCMCIA card slot in a laptop personal computer.

The RF5112 operates from a single supply voltage of 3.0V to 5.0V to deliver specified performance. Power control is provided through two control pins (V_{REG1} and V_{REG2}). For the best performance and lower current, there is a 68Ω resistor (not required at 5V operation) placed in series with V_{REG2} control line. If customer desires, V_{REG1} and V_{REG2} can be connected together prior to the series resistor on V_{REG2} (see applications schematic for details).

The output match of the RF5112 provides flexibility to optimize performance on the customer board using minimum component count and the lowest cost bill of materials (BOM). The output match topology follows that of a low pass network and it incorporates a series capacitor as the last component which can also serve as a DC block. Depending on the voltage of operation, the output match will require either one or two shunt capacitors to optimize the return loss and bandwidth. In the case of a 3.3V operation, only one capacitor is required while the 5V operation requires two. The value of the shunt tuning capacitor in the 3.3V case is 2.2pF and its placement is approximately 112mils from the package RF output pin. This location is marked with the reference designator C10 on the evaluation board. For the 5V operation, the first tuning capacitor value is 1.5pF and its placement approximately 90mils from the package (reference designator C10). The second tuning cap value for the 5V operation is 1pF and its placement is approximately 200mils from the package (C11 reference designator). DC bias for the last stage is provided through an RF Choke connected directly at the node between the transistor's collector and output match. This inductor plays a small role on the output match performance so its value must be carefully chosen as to not detune the circuit or lower its Q. RFMD recommends to use a high-Q inductor with a range in value between 5.6nH to 7.5nH.

PCB layout and material will affect optimum value and placement for these tuning capacitors. For fastest implementation and best results when designing with the RF5112, RFMD recommends that the evaluation board be copied as close as possible in particular the grounds and distance of components from the package pins (refer to schematic for additional details). The initial PCB layout should include exposed ground area near the shunt tuning capacitors to allow fine tuning of the output match. Smith Chart-based design tools may be used to assist in determining the desired capacitor value and transmission line physical characteristics. Note that the use of a single capacitor output circuit match results in a more sensitive match and slightly reduced RF5112 bandwidth. In this configuration, the RF5112 will exhibit sufficient output spectrum bandwidth to meet IEEE802.11b/g requirements when matched properly.

Upon request, RFMD can provide Gerber files for the evaluation board and BOM. High-Q tuning components are not required in every RF5112 based design. However, it is a good practice and highly recommended to start the initial tune with high-Q components then substitute with standard parts and compare against the initial performance. RFMD experience indicates that yield improvements offset the cost difference between "High-Q" and "Low-Q" components.

The RF5112 had been primarily characterized with a V_{REG} voltage of 2.85V. However, the RF5112 will operate from a wide range of bias control voltages and within a wide range of frequencies (typically 1800MHz to 2800MHz). If a bias control voltage other than 2.85V is preferred or if a different frequency range (other than 2.4GHz to 2.5GHz) is desired, please contact RFMD Sales or Applications Engineering for assistance.

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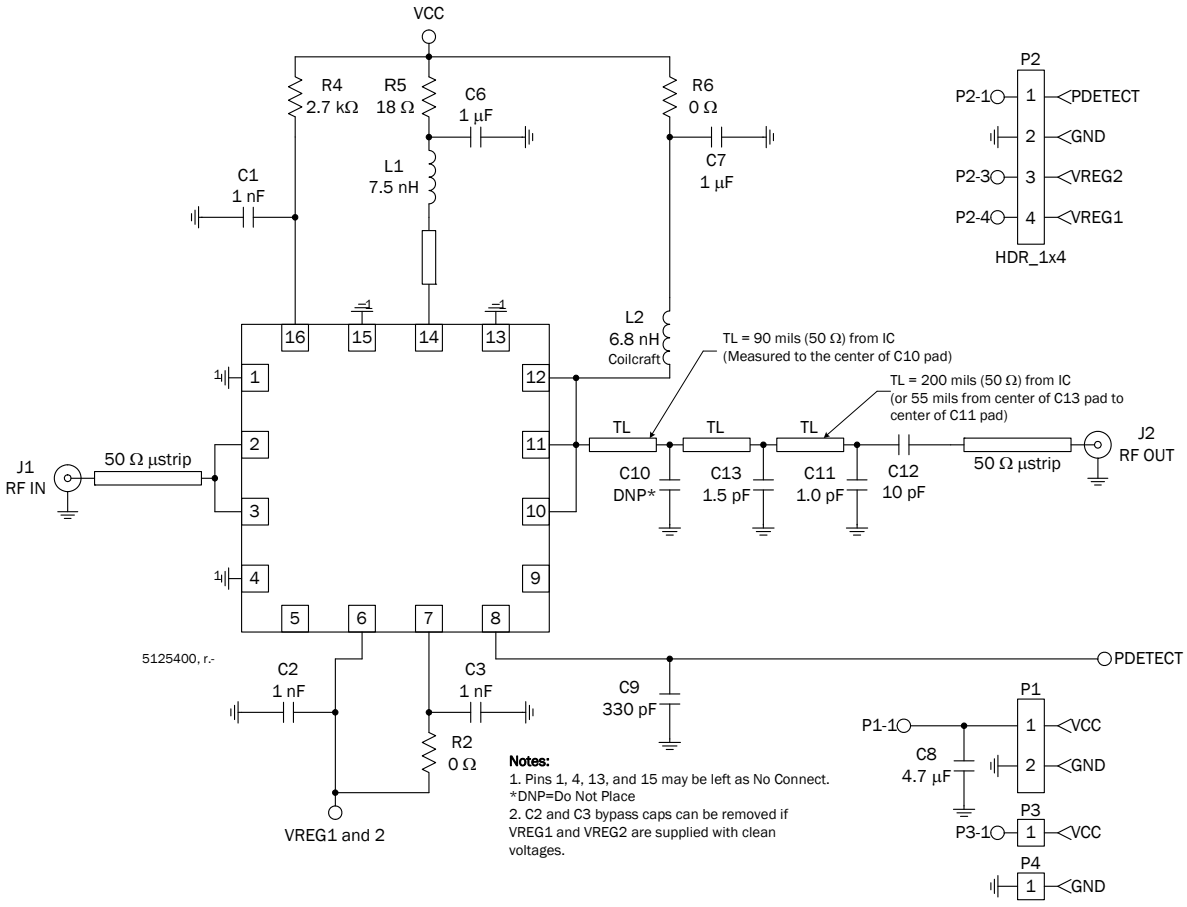
Evaluation Board Schematic - 5V



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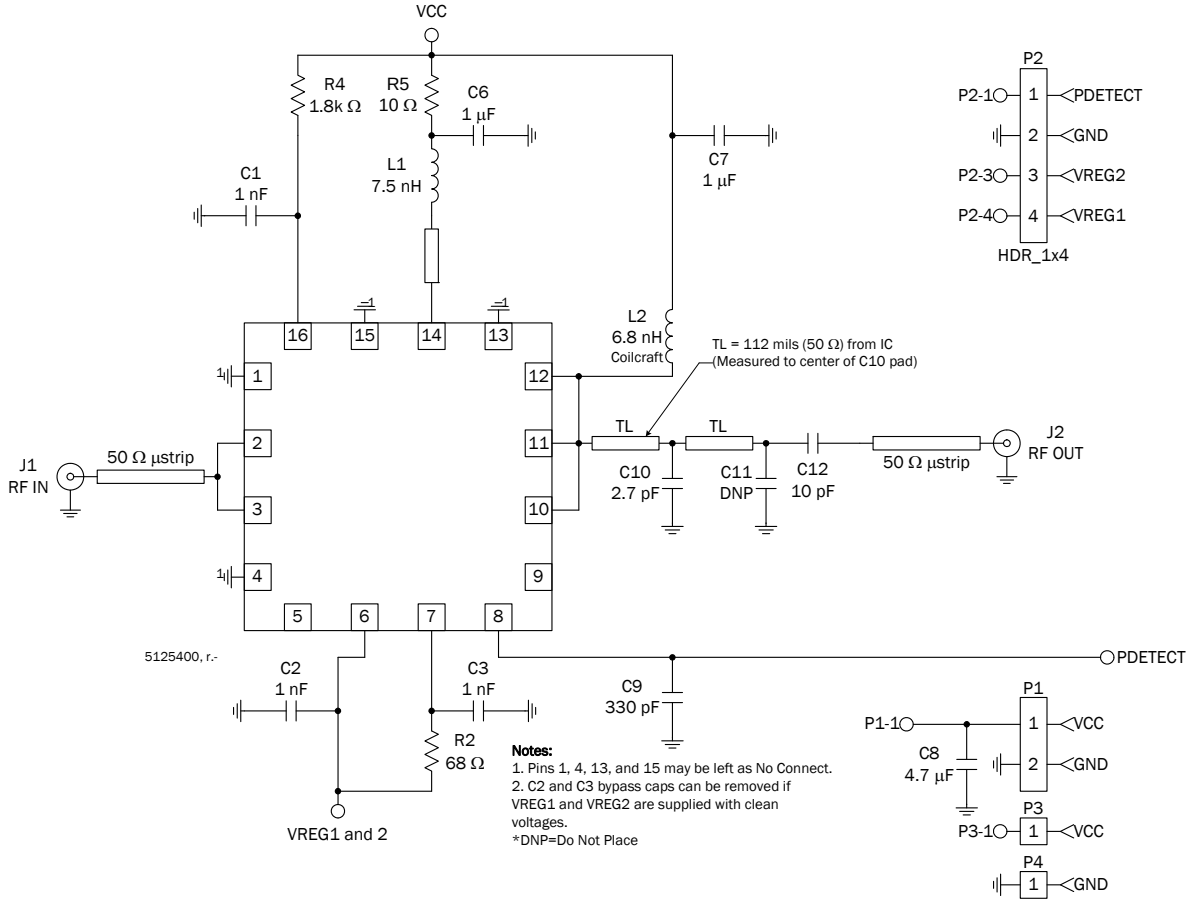
Evaluation Board Schematic - 3.3V



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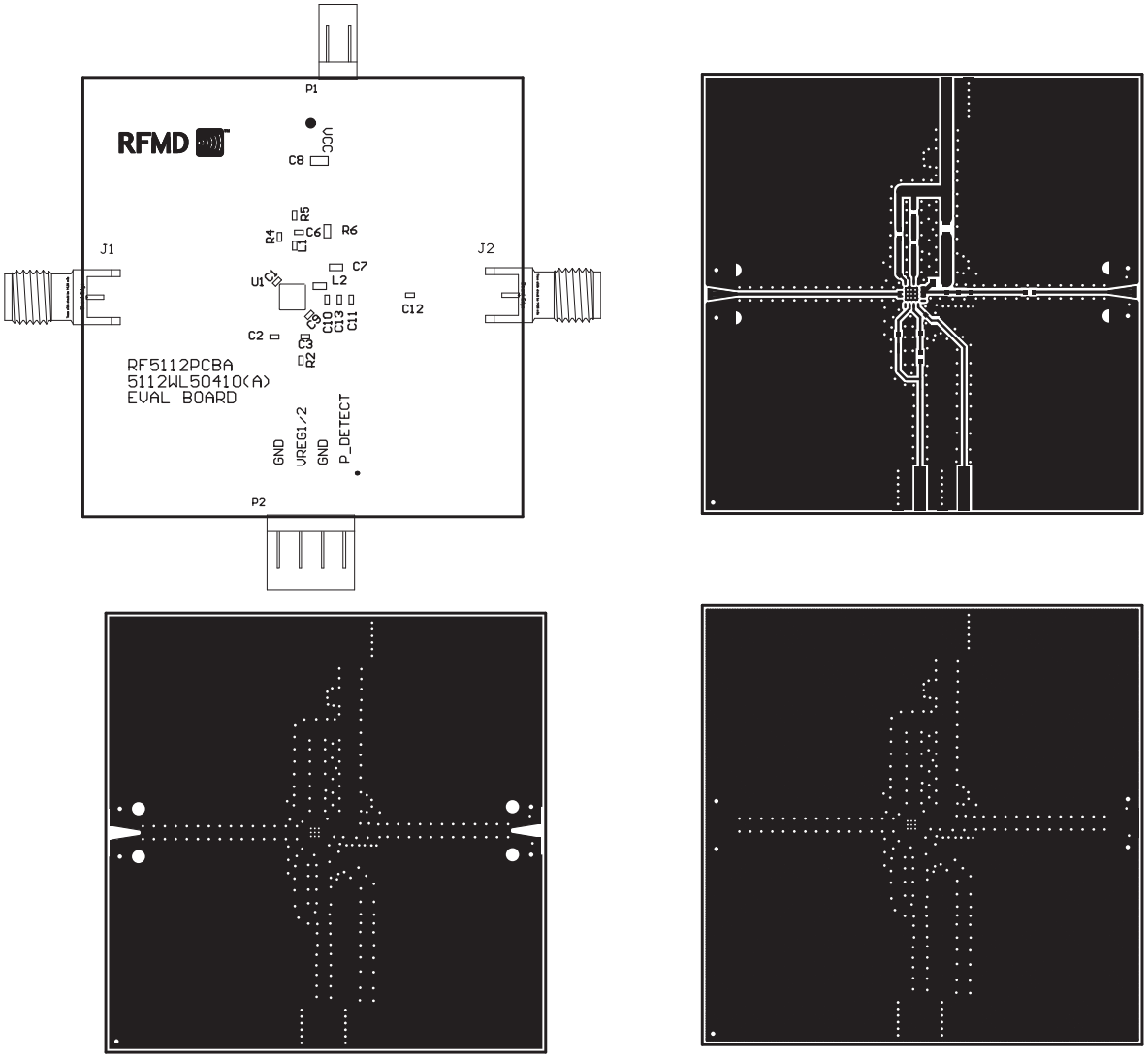
5.0V Evaluation Board Layout
Board Size 2.0” x 2.0”
Board Thickness 0.031”, Board Material FR-4, Multi-Layer



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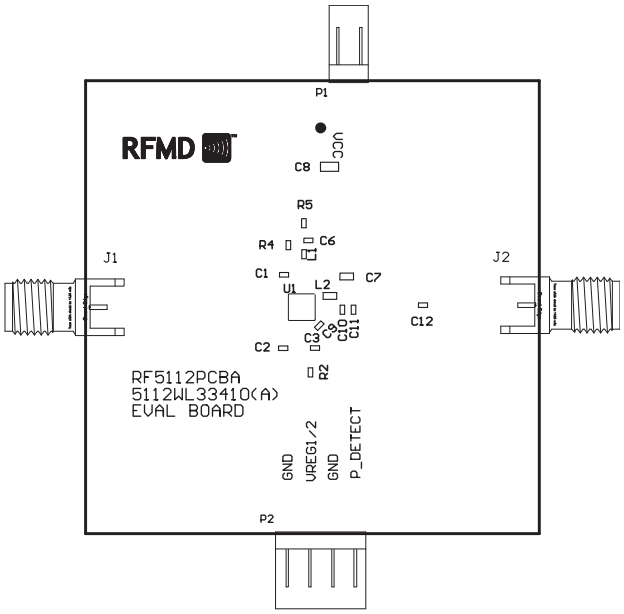
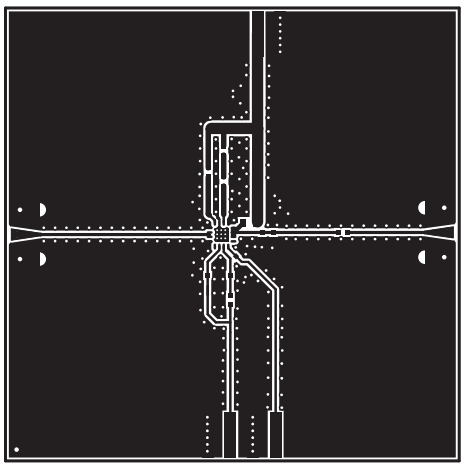
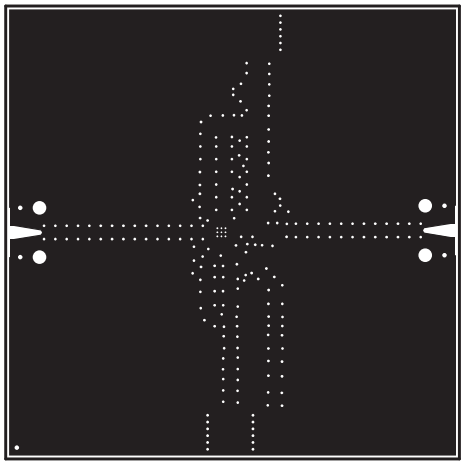
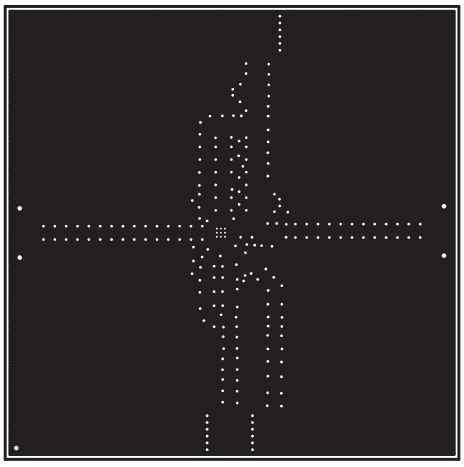
3.3V Evaluation Board Layout
Board Size 2.0” x 2.0”
Board Thickness 0.031”, Board Material FR-4, Multi-Layer









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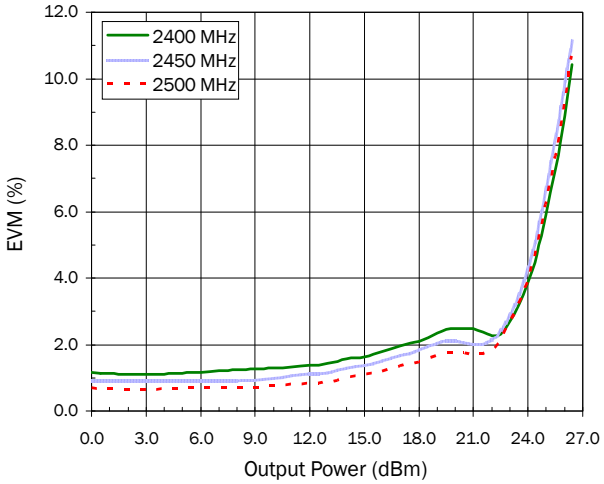
5V Operation Typical Performance

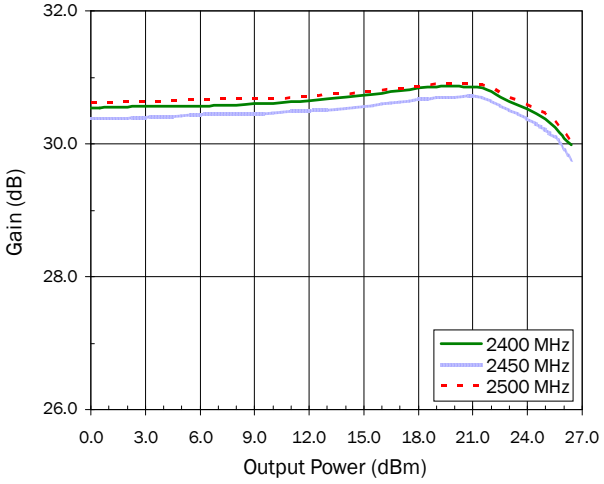
EVM versus Output Power over Frequency

V_{CC}=5.0V, OFDM 54Mbps, 50% Duty Cycle, Temp=25°C



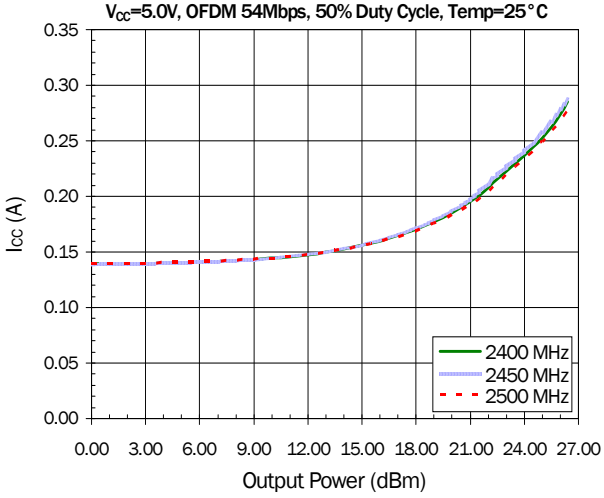
Gain versus Output Power over Frequency

V_{CC}=5.0V, OFDM 54Mbps, 50% Duty Cycle, Temp=25°C



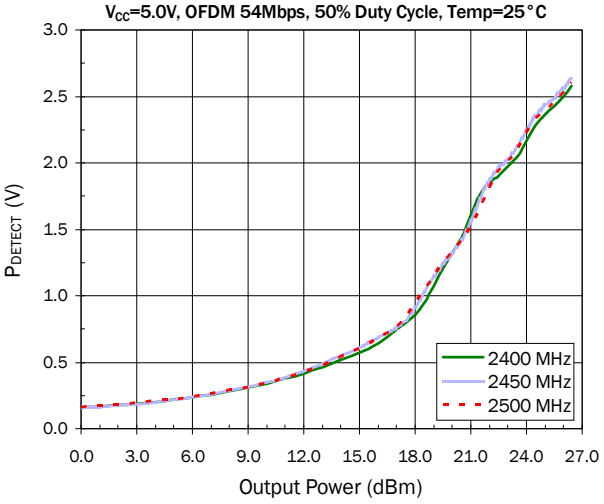
I_{CC} versus Output Power over Frequency

V_{CC}=5.0V, OFDM 54Mbps, 50% Duty Cycle, Temp=25°C



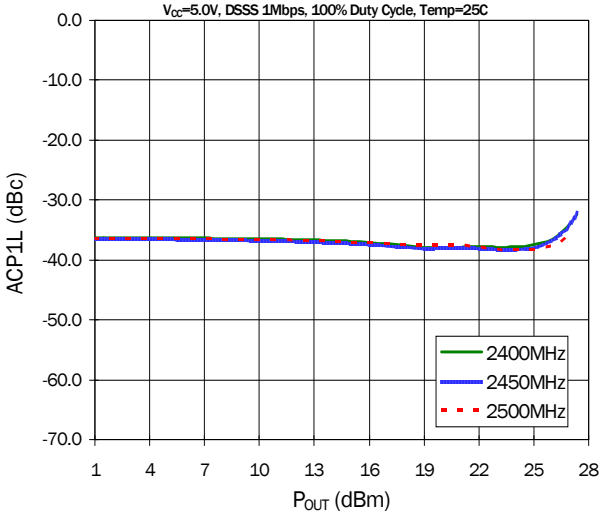
P_{DETECT} versus Output Power over Frequency

V_{CC}=5.0V, OFDM 54Mbps, 50% Duty Cycle, Temp=25°C

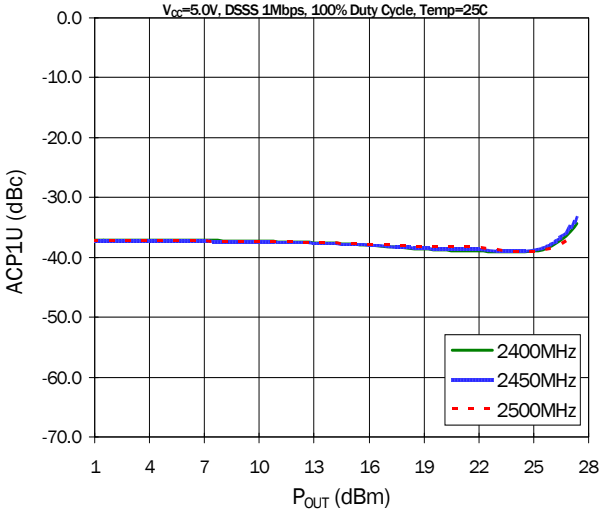


5V Operation Typical Performance

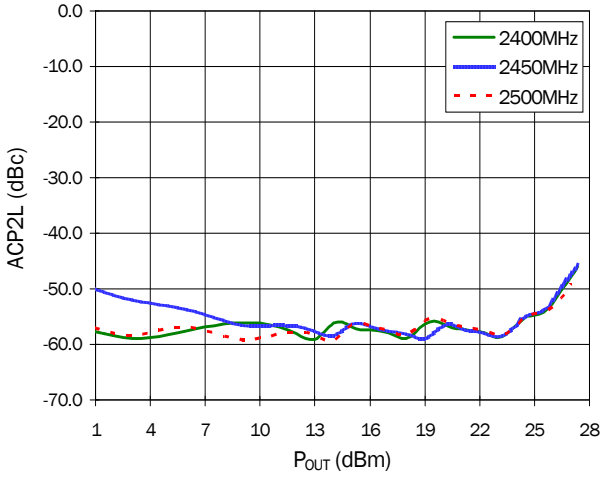
ACP1 (Lower) versus Output Power over Frequency
V_{CC}=5.0V, DSSS 1Mbps, 100% Duty Cycle, Temp=25C



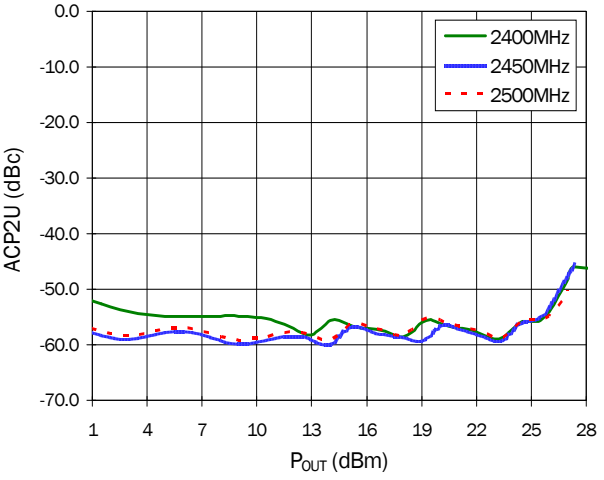
ACP1 (Upper) versus Output Power over Frequency
V_{CC}=5.0V, DSSS 1Mbps, 100% Duty Cycle, Temp=25C



ACP2 (Lower) versus Output Power over Frequency
V_{CC}=5.0V, DSSS 1Mbps, 100% Duty Cycle, Temp=25C



ACP2 (Upper) versus Output Power over Frequency
V_{CC}=5.0V, DSSS 1Mbps, 100% Duty Cycle, Temp=25C



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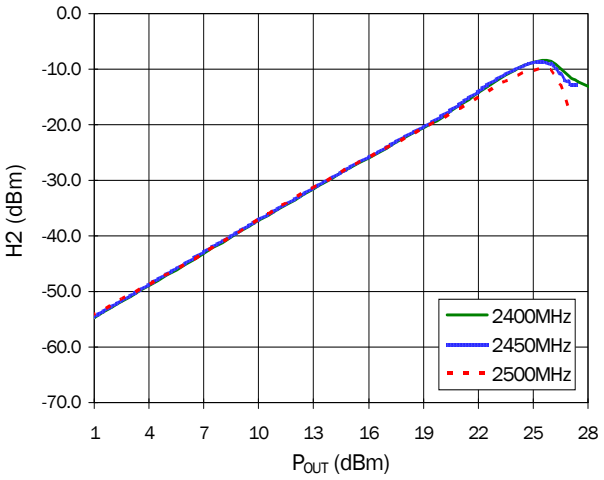
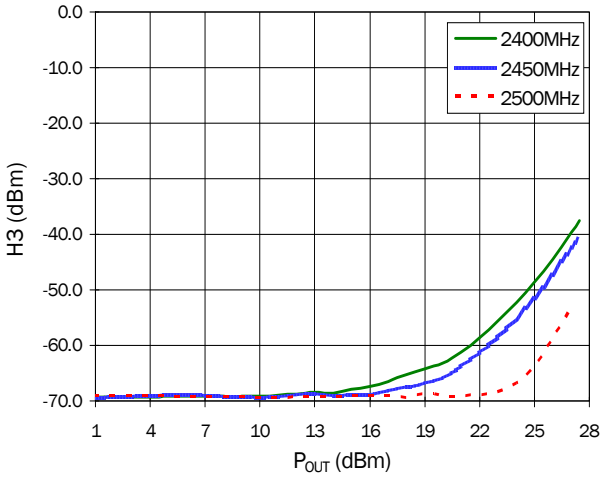
5V Operation Typical Performance

H2(dBm) versus Output Power over Frequency
V_{CC}=5.0V, DSSS 1Mbps, 100% Duty Cycle, Temp=25C



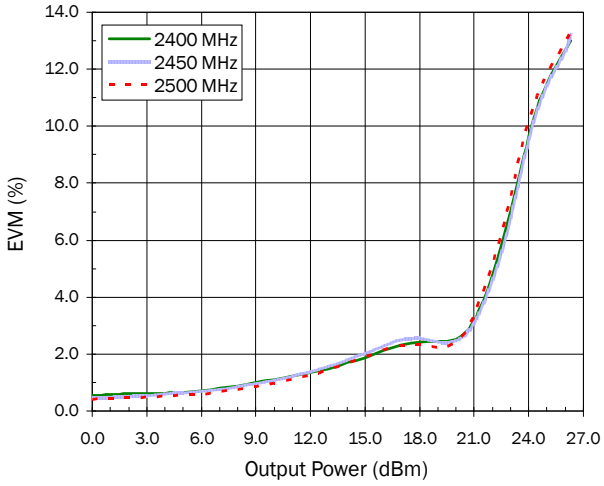
H3(dBm) versus Output Power over Frequency
V_{CC}=5.0V, DSSS 1Mbps, 100% Duty Cycle, Temp=25C



3.3V Operation Typical Performance

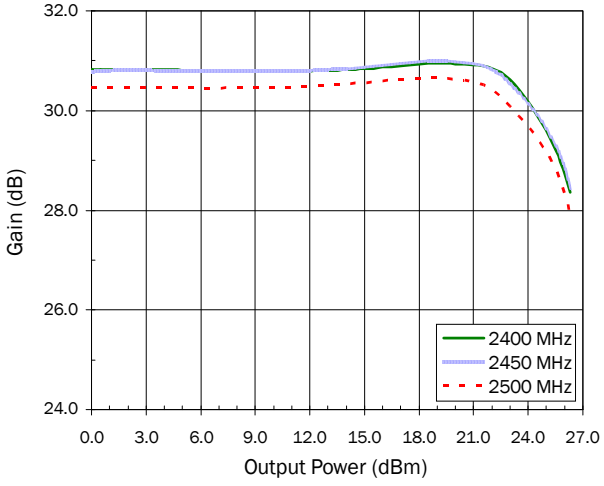
EVM versus Output Power over Frequency

V_{CC}=3.3V, OFDM 54Mbps, 50% Duty Cycle, Temp=25°C



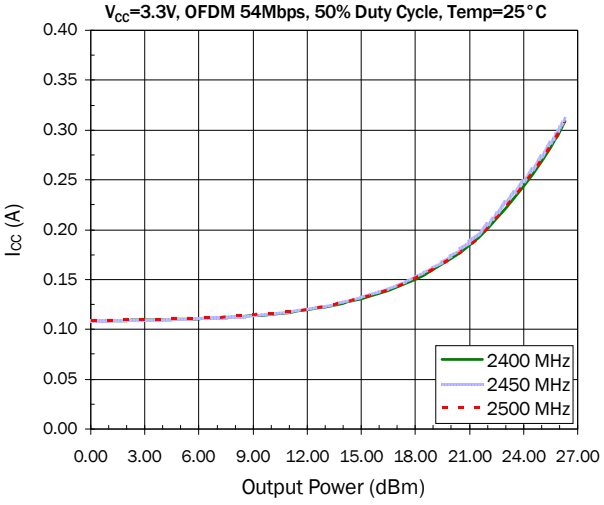
Gain versus Output Power over Frequency

V_{CC}=3.3V, OFDM 54Mbps, 50% Duty Cycle, Temp=25°C



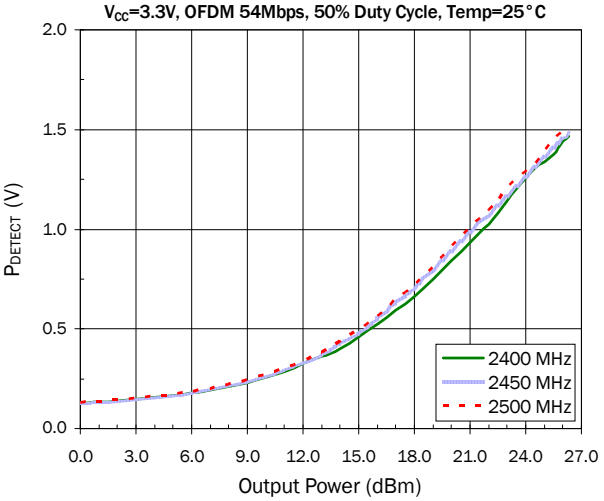
I_{CC} versus Output Power over Frequency

V_{CC}=3.3V, OFDM 54Mbps, 50% Duty Cycle, Temp=25°C



P_{DETECT} versus Output Power over Frequency

V_{CC}=3.3V, OFDM 54Mbps, 50% Duty Cycle, Temp=25°C



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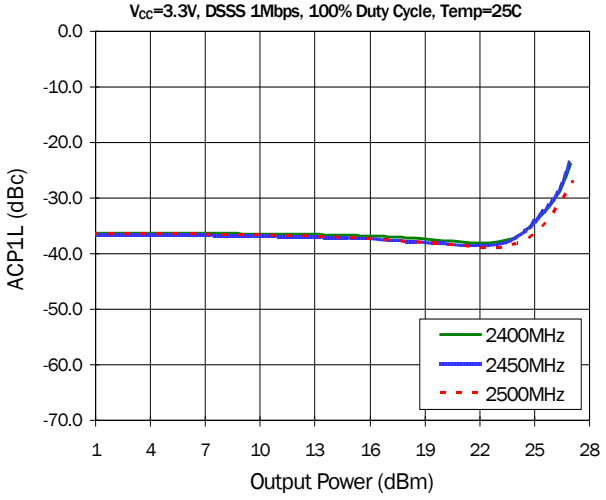
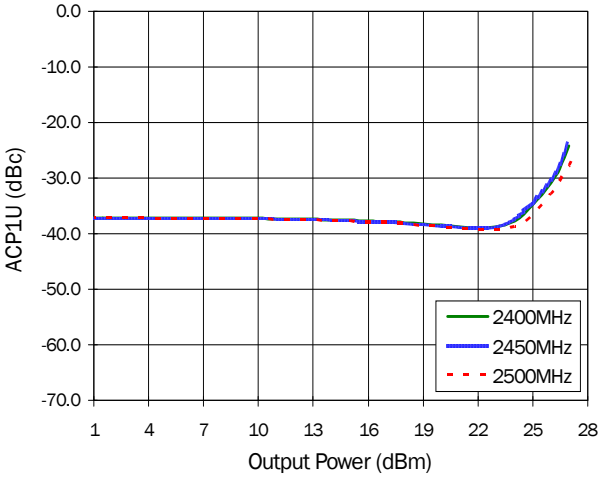
3.3V Operation Typical Performance

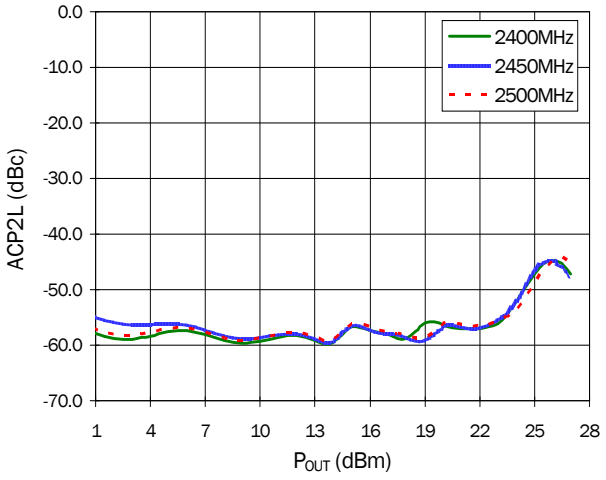
ACP1 (Lower) versus Output Power over Frequency
V_{CC}=3.3V, DSSS 1Mbps, 100% Duty Cycle, Temp=25C



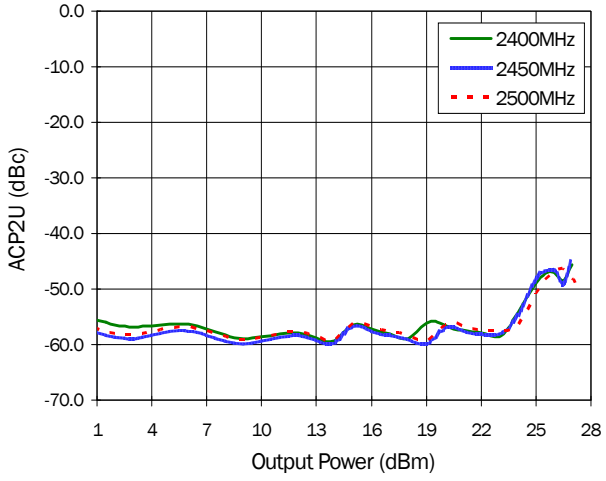
ACP1 (Upper) versus Output Power over Frequency
V_{CC}=3.3V, DSSS 1Mbps, 100% Duty Cycle, Temp=25C



ACP2 (Lower) versus Output Power over Frequency
V_{CC}=3.3V, DSSS 1Mbps, 100% Duty Cycle, Temp=25C

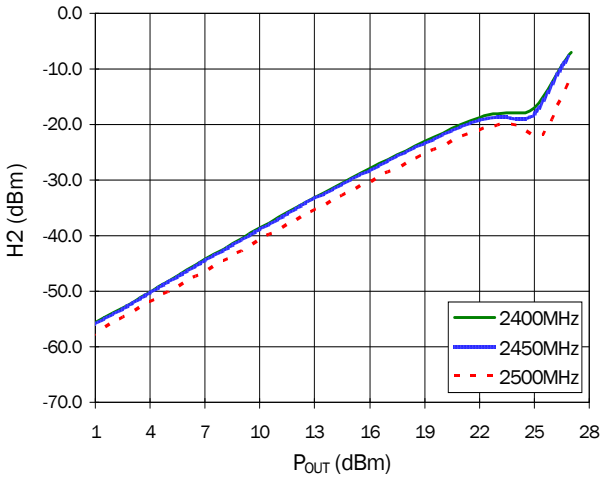


ACP2 (Upper) versus Output Power over Frequency
V_{CC}=3.3V, DSSS 1Mbps, 100% Duty Cycle, Temp=25C

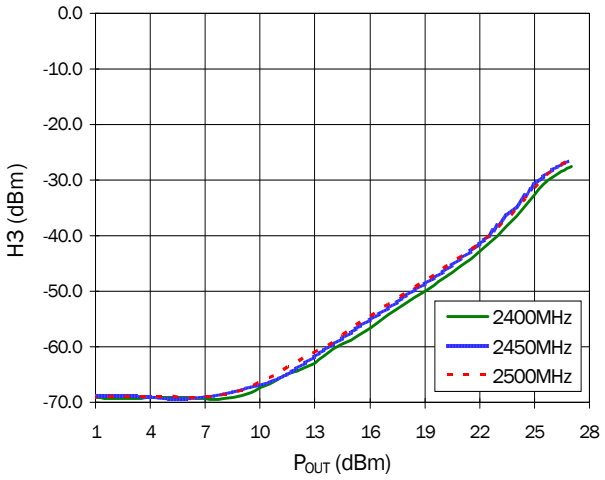


3.3V Operation Typical Performance

H2(dBm) versus Output Power over Frequency
V_{CC}=3.3V, DSSS 1Mbps, 100% Duty Cycle, Temp=25C



H3(dBm) versus Output Power over Frequency
V_{CC}=3.3V, DSSS 1Mbps, 100% Duty Cycle, Temp=25C



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PCB Design Requirements

PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

PCB Metal Land Pattern

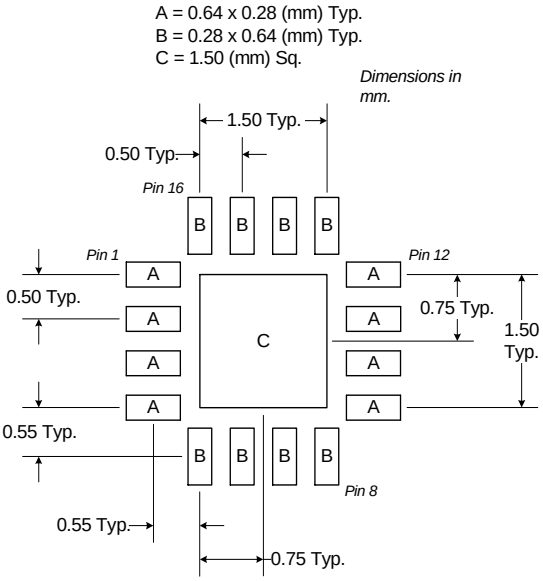

Figure 1. PCB Metal Land Pattern (Top View)

PCB Solder Mask Pattern

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.

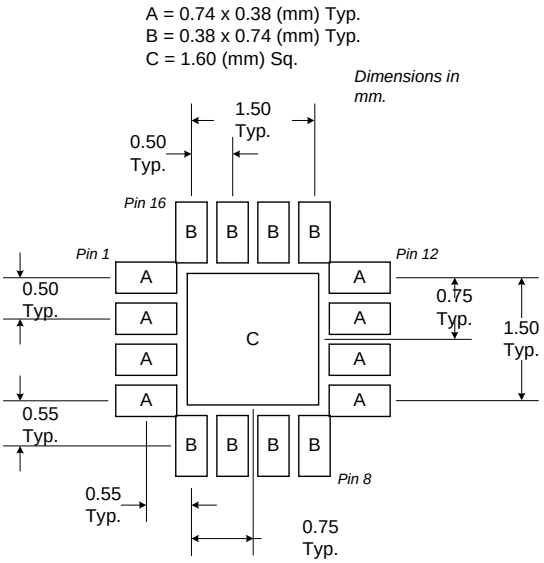

Figure 2. PCB Solder Mask Pattern (Top View)

Thermal Pad and Via Design

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

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RoHS* Banned Material Content

RoHS Compliant:	Yes
Package total weight in grams (g):	0.015
Compliance Date Code:	N/A
Bill of Materials Revision:	-
Pb Free Category:	e3

Bill of Materials	Parts Per Million (PPM)					
	Pb	Cd	Hg	Cr VI	PBB	PBDE
Die	0	0	0	0	0	0
Molding Compound	0	0	0	0	0	0
Lead Frame	0	0	0	0	0	0
Die Attach Epoxy	0	0	0	0	0	0
Wire	0	0	0	0	0	0
Solder Plating	0	0	0	0	0	0

This RoHS banned material content declaration was prepared solely on information, including analytical data, provided to RFMD by its suppliers, and applies to the Bill of Materials (BOM) revision noted above.

* DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL of 27 January 2003 on the restriction of the use of certain hazardous substances in electrical and electronic equipment