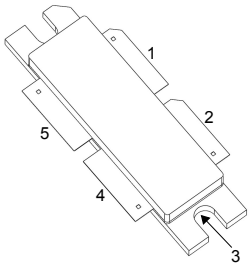
RF2L24280CB4

Datasheet

280 W, 28 V, 2.4 to 2.5 GHz RF power LDMOS transistor



D4E

Pin connection	
Pin	**Connection**
1	Drain A
2	Drain B
3	Source (bottom side)
4	Gate B
5	Gate A

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
RF2L24280CB4	2450 MHz	28 V	280 W	13 dB	60%

- High efficiency and linear gain operations
- Integrated ESD protection
- Internally matched pair transistors in push-pull configuration
- Large positive and negative gate-source voltage range for improved class C operation
- Excellent thermal stability, low HCI drift
- In compliance with the European directive 2002/95/EC

Applications

- Industrial, scientific and medical

Description

The RF2L24280CB4 is a 280 W, internally matched LDMOS FET, designed for multiple use especially RF energy applications including cooking, heating and medical in the frequency range from 2.4 to 2.5 GHz. It is qualified up to 32 V operation.

Product status link
RF2L24280CB4

Product summary	
Order code	RF2L24280CB4
Marking	2L24280
Package	D4E
Packing	Tray
Base/bulk quantity	20/100

1 Electrical ratings

Table 1. Absolute maximum ratings (T_C = 25 °C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	65	V
V_{GS}	Gate-source voltage	-6 to 10	V
V_{DD}	Maximum operating voltage	32	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}(1)	Thermal resistance, junction-to-case	0.2	°C/W

1. *T_C = 85 °C , T_J = 200 °C, DC test.*

Table 3. ESD protection

Symbol	Test methodology	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	2
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS002-2014)	C3

2 Electrical characteristics

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_{DS} = 100 µA	65	-		V
I_{DSS}	Zero gate voltage drain leakage current	V_{GS} = 0 V, V_{DS} = 28 V		-	1	µA
		V_{GS} = 0 V, V_{DS} = 50 V		-		
I_{GSS}	Gate-source leakage current	V_{GS} = -6/10 V, V_{DS} = 0 V		-	±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = 28 V, I_{DS} = 600 µA	1.5	-	2.5	V
$V_{GS(Q)}$	Gate quiescent voltage	V_{DS} = 2 V, I_{DS} = 20 mA	0.8	-	2.7	V
$V_{DS(on)}$	Static drain-source on-voltage	V_{GS} = 10 V, I_{DS} = 1 A	60	-	120	mV
$I_{DS(on)}$	Static drain-source on-current	V_{GS} = 10 V, V_{DS} = 100 mV	0.5	-	1.5	A
$R_{DS(on)}$	Drain-source on-state resistance	V_{GS} = 10 V, I_{DS} = 1 A		-	1	Ω

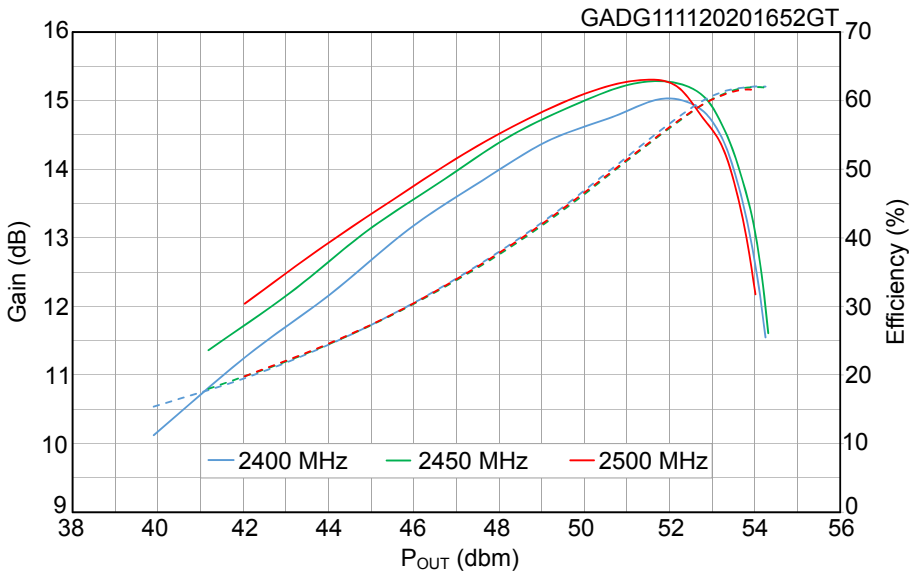
Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	Output power	f = 2450 MHz, pulsed CW, 2.5 dB compression	-	280		W
G_{PS}	Power gain		-	13		dB
η_D	Drain efficiency		-	60		%
VSWR	Load mismatch	P_{OUT} = 280 W, all phases	-		10:1	

Note: V_{DD} = 28 V, I_{DQ} = 10 mA, pulse width = 10 µs, duty cycle = 10%.

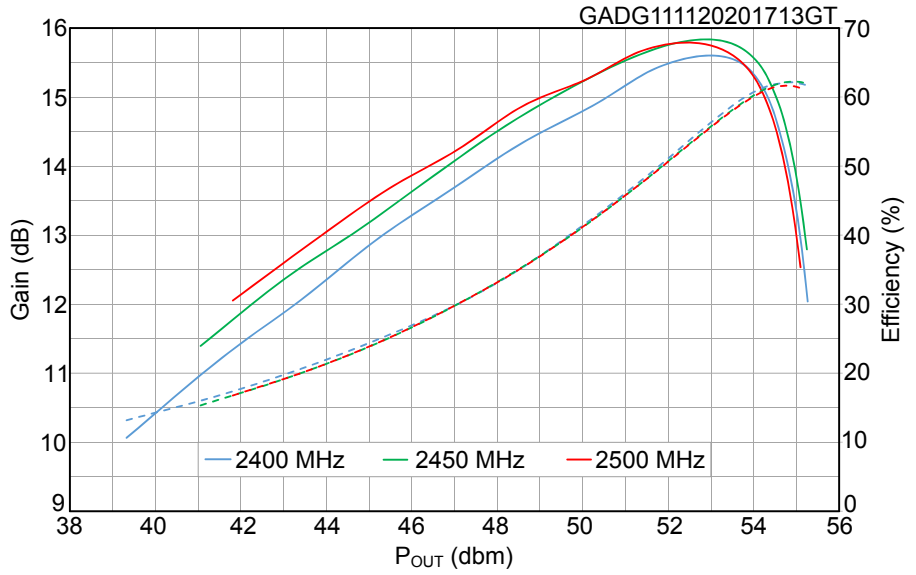
3 Typical performances

Figure 1. Power gain and drain efficiency vs output power at V_{DD} = 28 V



Note: I_{DQ} = 10 mA, pulse width = 10 µs, duty cycle = 10%.

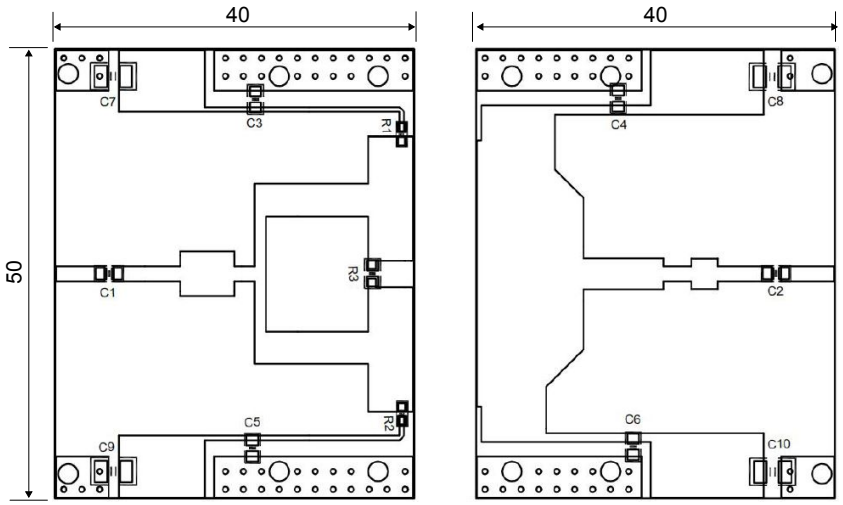
Figure 2. Power gain and drain efficiency vs output power at V_{DD} = 32 V



Note: I_{DQ} = 10 mA, pulse width = 10 µs, duty cycle = 10%.

4 Test circuits

Figure 3. **Test circuit layout (dimensions are in mm)**



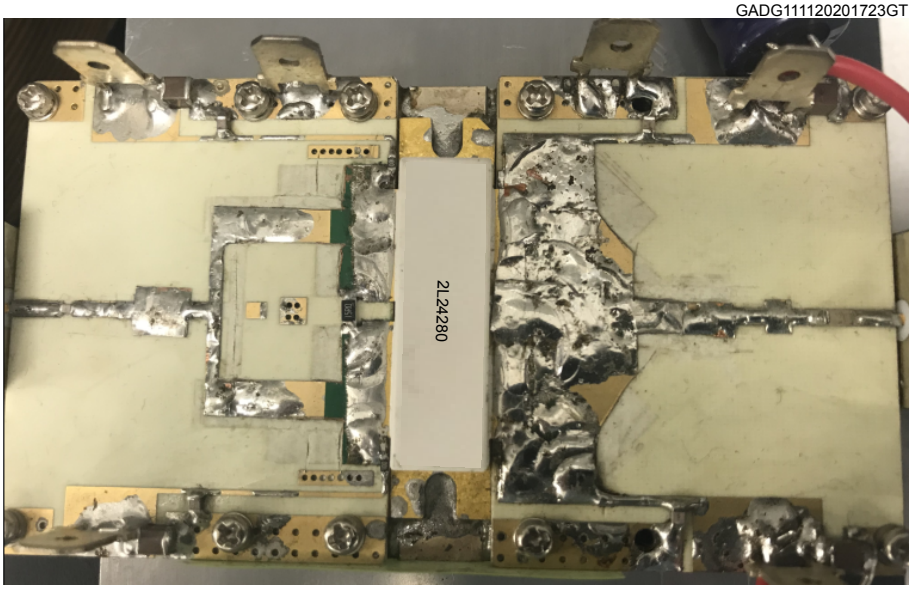
GADG030220210813GT

Table 6. **Components list**

Component	Value	Size	Reference
C1, C2, C3, C4, C5, C6	6.8 pF	0805	ATC600F
C7, C8, C9, C10	10 µF	1210	X7R
R1, R2	10 Ω	0603	
R3	15 Ω	1206	
PCB	0.762 mm (0.030") thick, εr = 3.48, Rogers RO4350B		

Figure 4. **Test circuit photo**

GADG111120201723GT



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 D4E package information

Figure 5. D4E package outline

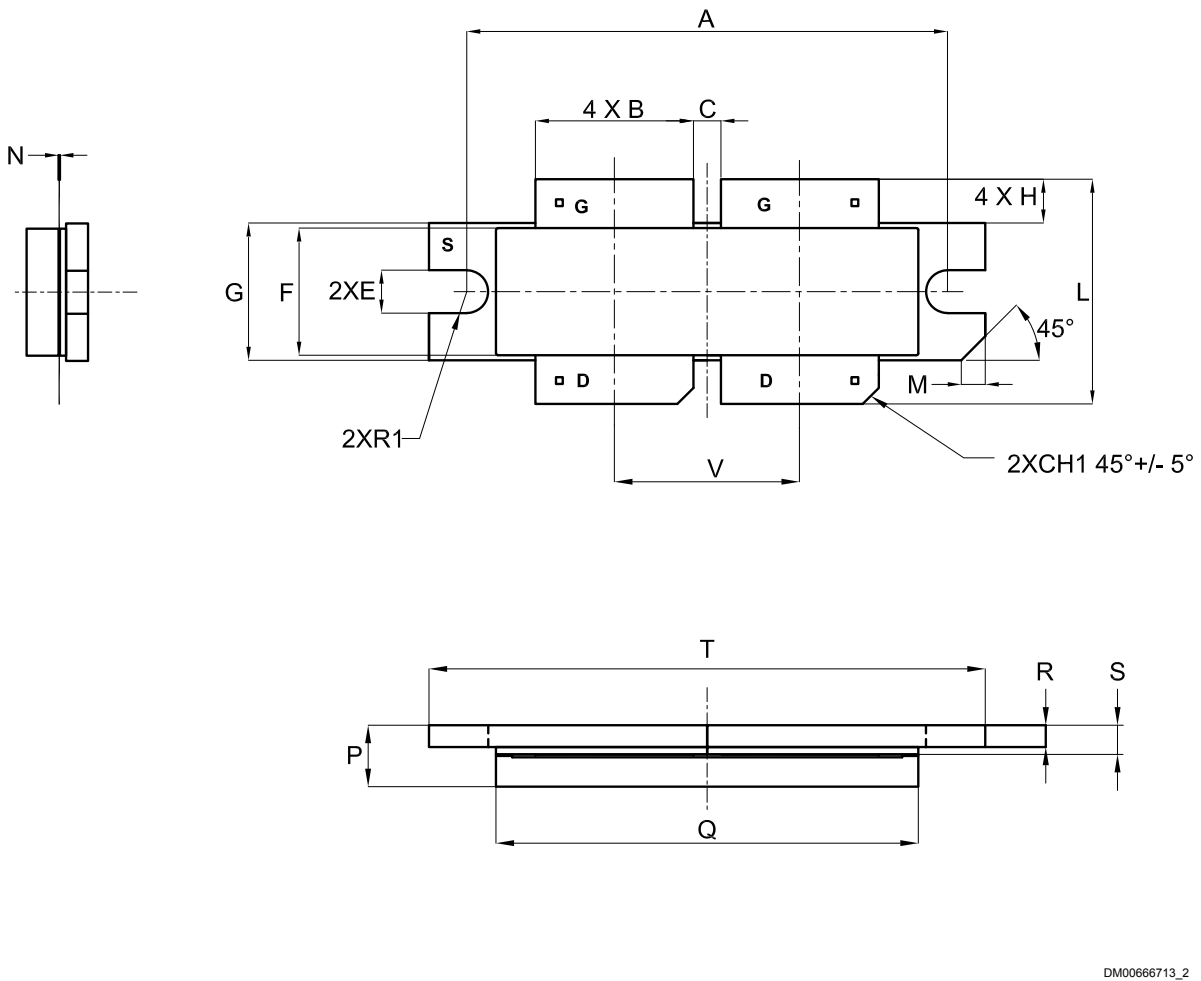
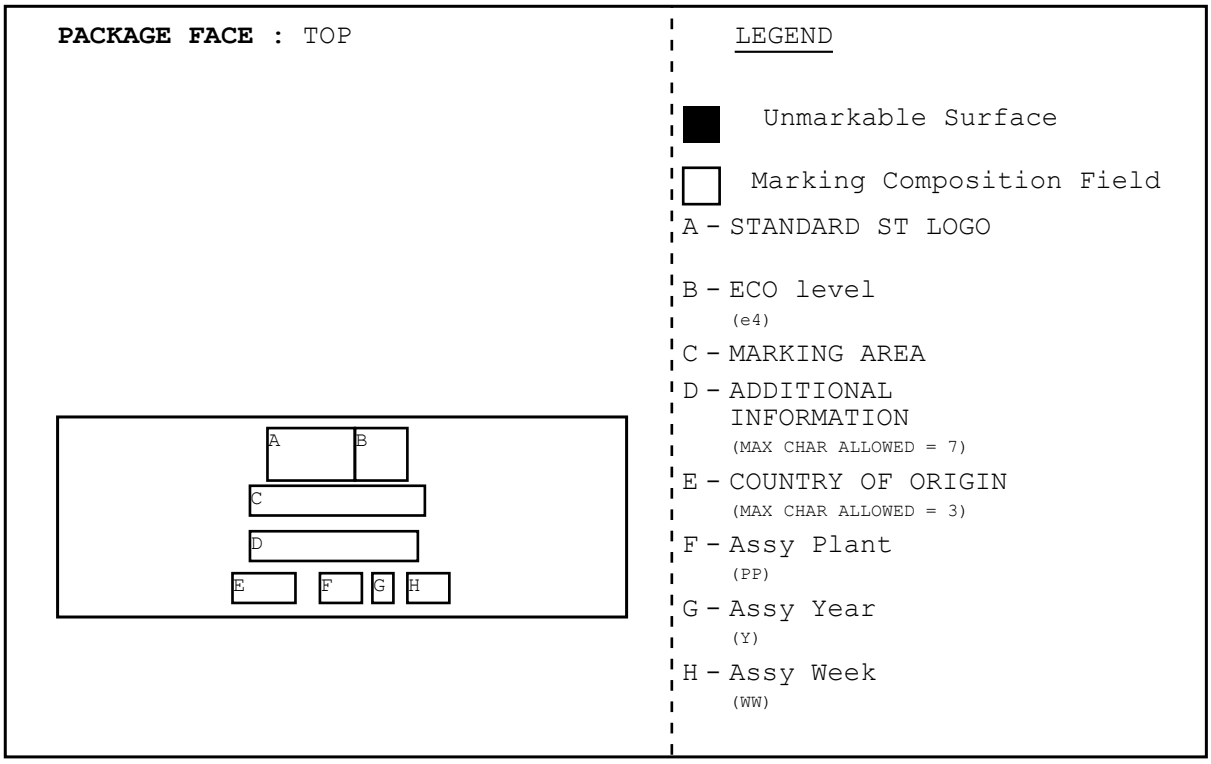


Table 7. **D4E package mechanical data**

Symbol	Millimeters		
	Min.	Typ.	Max.
A	35.44	35.56	35.68
B	11.56	11.68	11.80
C	1.92	2.04	2.16
E	3.06	3.18	3.30
F	9.25	9.40	9.50
G	10.04	10.16	10.28
H	5.72	5.85	3.48
L	16.11	16.62	17.13
M	1.51	1.78	2.05
N	0.10	0.13	0.16
P	4.17	4.55	4.93
Q	30.96	31.24	31.52
R	1.55	1.62	1.69
S	2.09	2.16	2.23
T	41.08	41.22	
V	13.60	13.72	13.84
R1		1.59	
CH1		1.19	

5.2 Marking information

Figure 6. **Marking composition**



GADG040220211644GT

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
16-Nov-2020	1	First release.
09-Feb-2021	2	Updated *Features* and *Device summary* in cover page. Updated *Table 3. ESD protection*. Updated *Table 5. Dynamic*. Updated *Figure 3. Test circuit layout* and added *Table 6. Components list*. Minor text changes.
21-Sep-2021	3	Updated Table 3. ESD protection. Updated Table 4. Static. Minor text changes.

Contents

1 Electrical data 2
2 Electrical characteristics 3
3 Typical performances 4
4 Test circuits 5
5 Package information 6
5.1 D4E package information 6
5.2 Marking information 8
Revision history 9

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2021 STMicroelectronics – All rights reserved