

Typical Applications

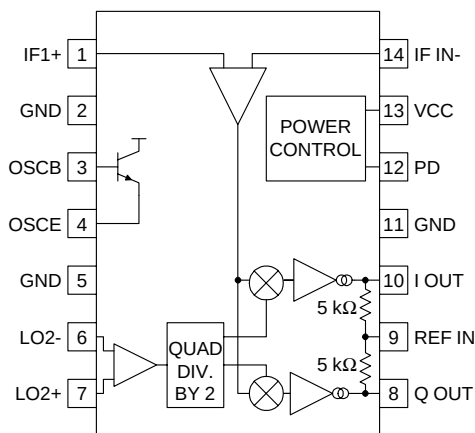
- UHF Digital and Analog Receivers
- Digital Communication Systems
- Spread-Spectrum Communication Systems
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment
- General Purpose Frequency Conversion

Product Description

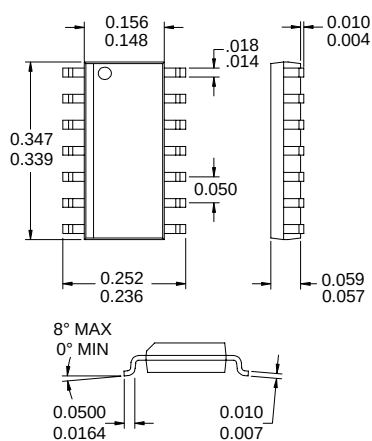
The RF2721 is a monolithic integrated quadrature demodulator intended for use in digital mobile radio receivers. In this application it is used to recover the in-phase and quadrature baseband signals from the amplified and filtered IF. The RF2721 is intended for IF systems where the IF frequency ranges from 100kHz to 500MHz, and the LO frequency is two times the IF. The IC contains all of the required components to implement the demodulation function of the receiver and contains a digital divider type 90° phase shifter, two double-balanced mixers, and baseband amplifiers designed to interface with analog to digital converters. The output DC offset may be slaved to the reference of the ADCs to maintain DC accuracy.

Optimum Technology Matching® Applied

- | | | |
|--|-----------------------------------|--------------------------------------|
| ☐ Si BJT | ☐ GaAs HBT | ☐ GaAs MESFET |
| ☒ Si Bi-CMOS | ☐ SiGe HBT | ☐ Si CMOS |



Functional Block Diagram



Package Style: SOIC-14

Features

- 5V Power Supply
- On-Chip Active Device for Oscillator
- ADC Compatible Outputs
- Low LO Power Requirement
- Digitally Controlled Power Down Mode
- 100kHz to 500MHz IF Operation

Ordering Information

- | | |
|-------------|----------------------------------|
| RF2721 | Quadrature Demodulator |
| RF2721 PCBA | Fully Assembled Evaluation Board |

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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage	-0.5 to +7.0	V _{DC}
Power Down Voltage (V _{PD})	-0.5 to V _{CC}	V _{DC}
IF Input Level	2.0	V _{PP}
LO Input Power	+10	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

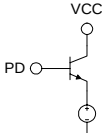


Caution! ESD sensitive device.

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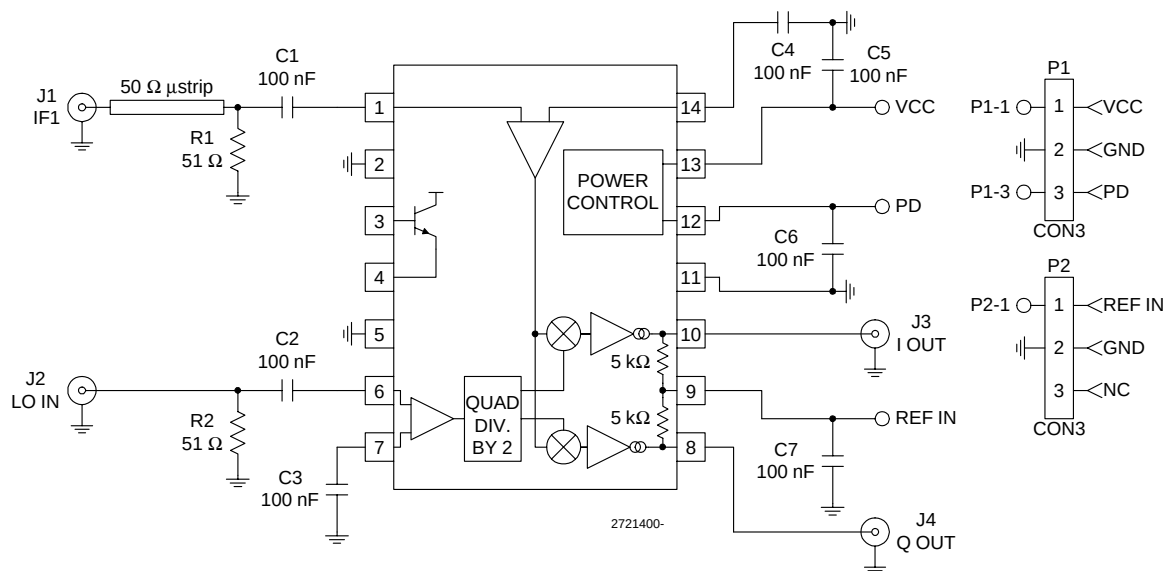
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V _{CC} =5.0V
IF Frequency Range		0.1 to 500		MHz	
Baseband Frequency Range		DC to >10		MHz	Load Impedance >5kΩ, C _{SHUNT} <1pF
		DC to 1		MHz	Load Impedance >5kΩ, C _{SHUNT} <10pF
Input Impedance		3		kΩ	At 70MHz, each input
Output Impedance		5000		Ω	
Maximum Output		>1.25		V _{PP}	With 250mV input
Gain	13	14		dB	Small-signal, 100mV input
I/Q Amplitude Balance		0.1	0.5	dB	
I/Q Phase Accuracy		±1	±5	°	
Reference Voltage		1.5 to 3.5		V	The reference voltage input should provide a low impedance at the I/Q frequency. The voltage sets the DC level seen on the I and Q ports.
DC Offset		3	20	mV	I to Q
		3	20	mV	I or Q to REF IN
LO					
Oscillator					Use provided transistor or external LO.
Frequency					Twice (2x) the IF frequency.
Level		0.1-1		V _{PP}	
Input Impedance		400-j1200		Ω	At 140MHz
Power Down					
Turn On/Off Time		<100		ns	
Input Resistance		>50		kΩ	
V _{IH}		2.5	V _{CC}	V	Threshold voltage; Part is "ON".
V _{IL}	0	0.8		V	Threshold voltage; Part is "OFF".
Power Supply					
Voltage		5		V	Specifications
		4.5 to 5.5		V	Operating limits
Current		4.5	7.2	mA	Operating
		300	500	μA	Power Down

Pin	Function	Description	Interface Schematic
1	IF IN+	Balanced IF input. An input level of 400mV _{PP} gives full output swing; a level of maximum 250mV _{PP} is recommended for linear operation. This pin has no internal DC block, and an external capacitor of 100nF is needed if connected to a DC path.	
2	GND	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane.	
3	OSC B	Base of the LO transistor. This pin is not connected to anything else. This transistor can be used for an oscillator. The collector of the transistor is connected to V _{CC} .	
4	OSC E	Emitter of the LO transistor. This pin is not connected to anything else.	See pin 3.
5	GND	Same as pin 2.	
6	LO2-	Balanced input for the doubled LO. An internal divide-by-2 network generates the actual LO for the mixers. The divided signal is not accessible. When the LO is driven single ended this pin should be connected to a 100nF capacitor to ground. This pin has an internal pull-up resistor to V _{CC} and an external DC blocking capacitor of 100nF is recommended.	
7	LO2+	Balanced input for the doubled LO. The input frequency should be twice (2x) the IF frequency. An internal divide-by-2 network generates the actual LO for the mixers. This pin has an internal pull-up resistor to V _{CC} , and an external DC blocking capacitor of 100nF is recommended. LO frequencies below 100kHz are acceptable, providing that the LO signal is square wave. Above 100kHz a sine wave signal is acceptable. The quadrature accuracy of the LO/2 frequency into the mixers is affected by the duty cycle of the LO input signal. Square wave signals with other than 50% duty cycle will degrade the quadrature accuracy of the LO signal, thereby adversely affecting the I and Q quadrature accuracy. Since the LO input is AC coupled, asymmetric sine waves and sine waves clipped on either the top or bottom half will not have 50% duty cycles relative to the internal DC reference point. For this reason, distorted LO sine wave signals will degrade performance in a fashion similar to non-50% duty cycle square waves. A sine wave input with even harmonics less than -15dBc is recommended. The internal limiting buffer amplifier ensures the amplitude stability of the demodulator.	See pin 6.
8	Q OUT	Demodulated baseband Q output. The reference DC level of this pin is set by the voltage of pin 9 (REF IN), which is connected to this pin through a 5kΩ resistor to the collectors of this push-pull output. This results in an output impedance of 5kΩ if the REF IN pin is connected to a low impedance source. The capacitance of the load determines the maximum baseband frequency. A very low capacitive load may stretch the 3dB bandwidth over 10MHz. Another way to increase bandwidth is by connecting a shunt resistor. This will trade-off gain for bandwidth.	
9	REF IN	Reference voltage input for the baseband outputs. This pin can be connected to the reference voltage source of the Analog to Digital Converter. It is connected to the I and Q outputs through 5kΩ resistors. This pin should have an external decoupling capacitor large enough to decouple the lowest baseband frequency.	See pin 8.

Pin	Function	Description	Interface Schematic
10	I OUT	Demodulated baseband I output. The reference DC level of this pin is set by the voltage of pin 9 (REF IN), which is connected to this pin through a 5k Ω resistor to the collectors of this push-pull output. This results in an output impedance of 5k Ω if the REF IN pin is connected to a low impedance source. The capacitance of the load determines the maximum baseband frequency. A very low capacitive load may stretch the 3dB bandwidth over 10MHz. Another way to increase bandwidth is by connecting a shunt resistor. This will trade gain for bandwidth.	See pin 8.
11	GND	Same as pin 2.	
12	PD	Power down control. When this pin is "low", all circuits are shut off. A "low" is typically 0.8V or less at room temperature. When this pin is "high", all circuits are operating normally.	
13	VCC	Power supply pin. An external 100nF bypass capacitor is recommended if no other bypass capacitor is nearby.	
14	IF IN-	Balanced IF input. An input level of 400mV _{PP} gives full output swing; a level of maximum 250mV _{PP} is recommended for linear operation. This pin has no internal DC block and an external capacitor of 100nF is needed if connected to a DC path. If the IF is driven by a single-ended source, connect this pin to an 100nF capacitor to ground.	See pin 1.

Evaluation Board Schematic

(Download [Bill of Materials](http://www.rfmd.com) from www.rfmd.com.)



Evaluation Board Layout

Board Thickness 1.5" x 1.5"
Board Thickness 0.031", Board Material FR-4

