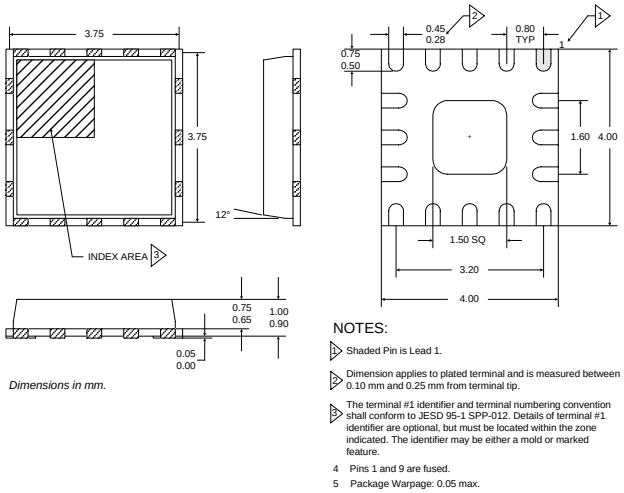
Typical Applications

- 868MHz/915MHz ISM Band Systems
- Local Oscillator Source
- Remote Keyless Entry
- AM/ASK/OOK Transmitter
- Wireless Security Systems

Product Description

The RF2514 is a monolithic integrated circuit intended for use as a low-cost AM/ASK transmitter. The device is provided in a 4mmx4mm, 16-pin leadless chip carrier and is designed to provide a phased locked frequency source for use in local oscillator or transmitter applications. The chip can be used in applications in the North American and European VHF/UHF ISM bands. The integrated VCO, phase detector, reference divider, and reference oscillator transistor require only the addition of an external crystal to provide a complete phase-locked oscillator. In addition to the standard power-down mode, the chip also includes an automatic lock detect feature that disables the transmitter output when the PLL is out-of-lock.



Dimensions in mm.

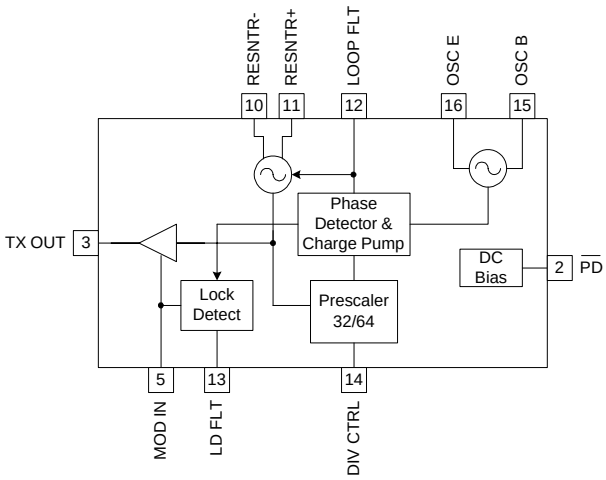
NOTES:

1. Shaded Pin is Lead 1.
2. Dimension applies to plated terminal and is measured between 0.10 mm and 0.25 mm from terminal tip.
3. The terminal #1 identifier and terminal numbering convention shall conform to JESD 95-1 SPP-012. Details of terminal #1 identifier are optional, but must be located within the zone indicated. The identifier may be either a mold or marked feature.
4. Pins 1 and 9 are fused.
5. Package Warpage: 0.05 max.

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ Si Bi-CMOS
- ☐ GaAs HBT
- ☐ SiGe HBT
- ☐ GaAs MESFET
- ☐ Si CMOS

Package Style: LCC, 16-Pin, 4x4



Functional Block Diagram

Features

- Fully Integrated PLL Circuit
- Integrated VCO and Reference Oscillator
- 2.2V to 3.6V Supply Voltage
- Low Current and Power Down Capability
- 100MHz to 1000MHz Frequency Range
- Out-of-Lock Inhibit Circuit

Ordering Information

RF2514	VHF/UHF Transmitter
RF2514 PCBA	Fully Assembled Evaluation Board

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7625 Thorndike Road
Greensboro, NC 27409, USA

Tel (336) 664 1233
Fax (336) 664 0454
http://www.rfmd.com

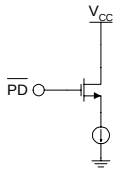
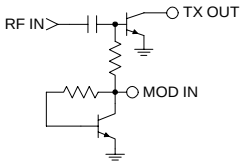
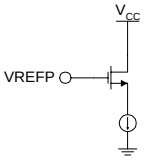
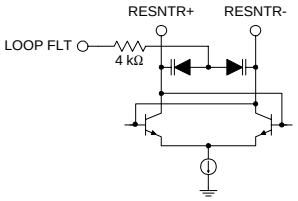
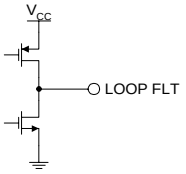
Absolute Maximum Ratings

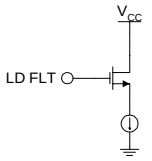
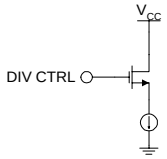
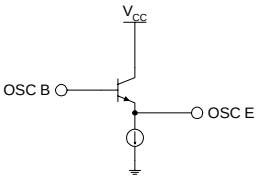
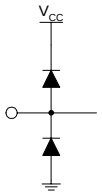
Parameter	Rating	Unit
Supply Voltage	-0.5 to +3.6	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to V_{CC}	V
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.0V, Freq=916MHz, R_{MODIN}=10kΩ
Frequency Range	100	868/915	1000	MHz	
Modulation		AM/ASK			
Modulation Frequency		4	20	kHz	Square wave, 50% duty cycle, 300kHz loop bandwidth
Incidental FM			15	kHz_{P-P}	
Output Power		1		dBm	50Ω load, CW
ON/OFF Ratio		52		dB	
PLL and Prescaler					
Prescaler Divide Ratio		32/64			
VCO Gain, K_{VCO}		40		MHz/V	Frequency and board layout dependent
PLL Phase Noise		-90		dBc/Hz	10kHz Offset, 300kHz loop bandwidth
		-95		dBc/Hz	100kHz Offset, 300kHz loop bandwidth
Harmonics		-25		dBc	With matched output and no additional filtering.
Reference Frequency		14.318	17	MHz	
Crystal Frequency Spurs			-52	dBc	300kHz PLL loop bandwidth
Max Crystal R_S		10	50	Ω	For a typ. 2ms turn-on time.
Max Crystal Motional Inductance		10		mH	For a typ. 2ms turn-on time.
Charge Pump Current		100		µA	KPD=100µA/2π=0.0159µA/rad
Power Down Control					
Power Down (V_{IL})	0		0.3	V	Voltage supplied to the input; device is “OFF”
Power Down (V_{IH})	V_{CC}-0.3		V_{CC}	V	Voltage supplied to the input; device is “ON”
Control Input Impedance	100			kΩ	
Turn On Time		2		ms	Crystal start-up, 14.318MHz crystal.
Turn Off Time		2		ms	
Power Supply					
Voltage	2.2	3.0	3.6	V	Specifications Operating limits
Current Consumption					
Average		8		mA	50% Duty Cycle 4kHz Data applied to the MOD IN input. R_{MODIN} (R7+R8)=10kΩ. Output power/DC current consumption externally adjustable by modulation input resistor (see applicable Application Schematic).
Sleep Mode			1	µA	$\overline{PD}$=0

Pin	Function	Description	Interface Schematic
1	GND1	Ground connection for the analog circuits, including TX buffer and output amplifier. Internally connected to die flag. For best performance, keep traces physically short and connect immediately to ground plane.	
2	$\overline{PD}$	Power Down control for all circuitry. When this pin is a logic “low” all circuits are turned off. When this pin is a logic “high”, all circuits are operating normally. See electrical parameters for “high” and “low” thresholds.	
3	TXOUT	Transmitter output. This output is an open collector and requires a pull-up inductor for bias/matching and a tapped capacitor for matching.	
4	VCC1	This pin is used to supply bias to the TX buffer amplifier.	
5	MOD IN	AM analog or digital modulation can be imparted to the carrier by an input to this pin. An external resistor is used to bias the output amplifiers through this pin. The voltage at this pin must not exceed 1.1V. Higher voltages may damage the device.	See pin 3.
6	VCC2	This pin is used to supply DC bias to the VCO, crystal oscillator, prescaler, phase detector, and charge pump. An IF bypass capacitor should be connected directly to this pin and returned to ground.	
7	GND2	Digital PLL ground connection.	
8	VREF P	Bias voltage reference pin for bypassing the prescaler and phase detector. The bypass capacitor should be of appropriate size to provide filtering of the reference crystal frequency and be connected directly to this pin.	
9	GND3	See pin 1.	
10	RESNTR-	The RESNTR pins are used to supply DC voltage to the VCO, as well as to tune the center frequency of the VCO. Equal value inductors should be connected to this pin and pin 11.	
11	RESNTR+	See pin 10.	
12	LOOP FLT	Output of the charge pump. An RC network from this pin to ground is used to establish the PLL bandwidth.	

Pin	Function	Description	Interface Schematic
13	LD FLT	This pin is used to set the threshold of the lock detect circuit. A shunt capacitor should be used to set an RC time constant with the on-chip series 1k resistor. The time constant should be approximately 10 times the reference period.	
14	DIV CTRL	Logic “High” input selects divide-by-64 prescaler. Logic “Low” input selects divide-by-32 prescaler.s	
15	OSC B	This pin is connected directly to the reference oscillator transistor base. The intended reference oscillator configuration is a modified Colpitts. A 68pF capacitor should be connected between pin 15 and pin 16.	
16	OSC E	This pin is connected directly to the emitter of the reference oscillator transistor. A 33pF capacitor should be connected from this pin to ground.	See pin 15.
Die Flag	GND	Exposed die flag is centered and measures 1.5mm x 1.5mm (0.059in. x 0.059in.). For best results, provide a solder pad for the flag and connect immediately to ground plane (see evaluation board lay-out). Internally connected to pins 1 and 9.	
	ESD	This diode structure is used to provide electrostatic discharge protection to 3kV using the Human body model. The following pins are protected: 1, 2, 4-9, 12-14. The die flag is not protected.	

RF2514 Theory of Operation

Introduction

Short range radio devices are becoming commonplace in today's environment. The most common examples are the remote keyless entry systems popular on many new cars and trucks and the ubiquitous garage door opener. Other applications are emerging along with the growth in home security and automation and the advent of various remote control applications. Typically these devices have been simplex, or one way, links. They are also typically built using surface acoustic wave (SAW) devices as the frequency control elements. This approach has been attractive because the SAW devices have been readily available and a transmitter, for example, could be built with only a few additional components. Recently, however, RF Micro Devices has introduced several new components that enable a new class of short range radio devices based on the use of crystals and phase locked loops for frequency control. These devices are superior in performance and comparable in cost to the traditional SAW based designs. The RF2514 is an example of such a device. The RF2514 is targeted for applications such as 315, 433, 868 and 915MHz band remote keyless entry systems, wireless security systems, and other remote control applications.

The RF2514 Transmitter

The RF2514 is a low cost AM/ASK VHF/UHF transmitter designed for applications operating within the frequency range of 100MHz to 1000MHz. In particular, it is intended for 868 and 915MHz band systems (ETS 300 220 applications and FCC Parts 15.231 and 15.249 transmitters) and remote keyless entry systems. It can also be used as a local oscillator signal source. The integrated VCO, phase detector, prescaler, and reference oscillator require only the addition of an external crystal to provide a complete phase-locked loop. In addition to the standard power down mode, the chip also includes an automatic lock detect feature that disables the transmitter output when the PLL is out-of-lock.

The device is manufactured on a 25GHz silicon bipolar-CMOS process and packaged in an industry standard MLF16 plastic package. This, combined with the low external parts count, enables the designer to achieve small-footprint, high-performance, low-cost designs.

The RF2514 is designed to operate from a supply voltage ranging from 2.2V to 3.6V, accommodating designs using three NiCd battery cells, two AAA flashlight cells, or a lithium button battery. The device is capable of providing up to +5dBm output power into a 50Ω load and is intended to comply with FCC and ETSI requirements for unlicensed remote control transmitters. ESD protection is provided on all pins except for OSCB, OSCE, RESNTR-, RESNTR+, TXOUT, and the two analog ground pins (1 and 9).

While this device is intended for OOK operation, it is possible to use narrowband FM. This is accomplished by modulating the reference oscillator rather than applying the data to the MOD IN input pin. The MOD IN pin should be tied high to cause the device to transmit. The deviation will be set by pulling limits of the crystal. Deviation sufficient for the transmission of voice and other low data rate signals can therefore be accomplished. Refer to the Application Schematic in the data sheet for details.

RF2514 Functional Blocks

A PLL consists of a reference oscillator, a phase detector, a loop filter, a voltage controlled oscillator (VCO), and a programmable divider in the feedback path. The RF2514 includes all of these internally except for the loop filter and the reference oscillator's crystal and two feedback capacitors.

The **reference oscillator** is a Colpitts type oscillator. Pins OSC B and OSC E provide connections to a transistor that is used as the reference oscillator. The Colpitts configuration is a low parts count topology with reliable performance and reasonable phase noise. Alternatively, an external signal could be injected into the base of the transistor. The drive level should, in either case, be around 500mV$_{PP}$. This level prevents overdriving the device and keeps the phase noise and reference spurs to a minimum.

The **prescaler** uses a series of flip-flops to divide the VCO frequency by either 64 or 32, depending upon the logic level present at the DIV CTRL pin. A high logic level will select the 64 divisor. A low logic level will select the 32 divisor. This divided signal is then fed into the phase detector where it is compared with the reference frequency.

The RF2514 contains an onboard **phase detector** and charge pump. The phase detector compares the phase of the reference oscillator to the phase of the prescaler output. The phase detector is implemented using flip-flops in a topology referred to as either "digital phase/frequency detector" or "digital tri-state comparator".

The circuit consists of two D flip-flops whose outputs are combined with a NAND gate which is then tied to the reset on each flip-flop. The outputs of the flip-flops are also connected to the charge pump inputs. Each flip-flop output signal is a series of pulses whose frequency is related to the flip-flop input frequency. When both inputs of the flip-flops are identical, the signals are both frequency and phase locked. If they are different, they will provide signals to the charge pump which will either charge or discharge the loop filter or place the charge pump in a high impedance state, maintaining the charge on the loop filter. The name "tri-state comparator" comes from this. The main benefit of this type of detector is the ability to correct for errors in both phase and frequency. When locked, the detector uses phase error for correction. When unlocked, it will use the frequency error for correction. This type of detector will lock under all conditions.

The **charge pump** consists of two transistors, one for charging the loop filter and the other for discharging the loop filter. The charge pump inputs are the outputs of the phase detector flip-flops. If both amplifier inputs are low, then the amplifier pair goes into a high impedance state, maintaining the charge on the loop filter. In the charge and discharge states, the loop filter integrates the pulses coming from the charge pump to create a control voltage for the voltage controlled oscillator.

The **VCO** is a tuned-differential amplifier with the bases and collectors cross-coupled to provide positive feedback and a 360° phase shift. The tuned circuit is located in the collectors and is comprised of internal varactors and external inductance, which also provides DC bias for the VCO. The varactor diodes are internally configured for negative tuning. That is, a higher control voltage results in a lower VCO frequency by reducing the varactor reverse bias which correspondingly increases the capacitance. The inductance is selected by the designer for the desired frequency of operation. Two inductor configurations are possible.

In the first configuration, two inductors are connected in series between RESNTR- and RESNTR+. A resistor is then used to provide the DC bias to the balanced inductance node formed by the series connection of the inductors. Ideally, the two inductors should be equal in value, but a slight imbalance is acceptable if necessary for VCO centering.

In the second configuration, a single inductor is placed across RESNTR- and RESNTR+ and one resistor is used to provide bias to the differential amplifier. The resistor is connected in series from VCC to either RESNTR- or RESNTR+. The inductor provides the DC bias path for the other resonator pin. This configuration has the advantage of lower cost and parts count, as only one inductor is required; the disadvantage is potentially suboptimal VCO centering due to limited standard inductor values. For example, 20nH may be the optimal inductance to center the VCO at the desired operating frequency, but only 18nH and 22nH inductors are available as standard values. However, for the two-inductor configuration, both inductors can be 10nH, thus giving the optimal 20nH of inductance. Of course, the problem of optimization can also be resolved by increasing (or decreasing) the inductance of the traces running to the inductor in the single-inductor configuration.

The output of the VCO is buffered and applied to the prescaler circuit, where it is divided by either 32 or 64, as selected by the designer, and compared to the reference oscillator frequency.

The **transmit amplifier** is a two-stage amplifier consisting of a driver and an open collector final stage. It is capable of providing 5dBm of output power into a 50Ω load while operating from a 3.6V power supply.

The **lock-detect circuitry** connects to the output of the phase detector circuitry and is used to disable the transmitter when the VCO is not phase-locked to the reference oscillator. This is necessary to avoid unwanted out-of-band transmission and to provide compliance with regulatory limits during an unlocked condition.

There are many possible reasons that the PLL could be unlocked. For instance, there is a short period during the start of any VCO in which the VCO starts oscillating and the reference oscillator builds up to full amplitude. During this period, the frequency will likely be outside the authorized band. Typically the VCO starts much faster than the reference oscillator. Once both VCO and reference oscillators are running, the phase detector can start slewing the VCO to the correct frequency, sliding across 200MHz of occupied spectrum. In some competitive devices, the transmitter output operates at full power under all of these conditions.

The lock protection circuit in the RF2514 is intended to stabilize quickly after power is applied to the chip and to disable the base drive to the transmit amplifier. This attenuates the output to levels that will be generally acceptable to regulatory boards as spurious emissions. Once the phase detector has locked the oscillators, then the lock circuit enables the MOD IN pin for

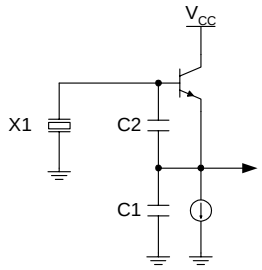
transmission of the desired data. There is no need for an external microprocessor to monitor the lock status, although that can be done with a low current A/D converter in a system micro, if needed. The lock detect circuitry contains an internal 1kΩ resistor which, combined with a designer-chosen capacitor for a particular RC time constant, filters the lock detect signal. This signal is then passed through an internal Schmitt trigger and used to enable or disable the transmit amplifier.

If the oscillator unlocks, even momentarily, the protection circuit quickly disables the output until lock is achieved. These unlocks can be caused by low battery voltage, poor power supply regulation, severe shock of the crystal or VCO, antenna loading, component failure, or a myriad of unexpected single-point failures.

The RF2514 contains onboard band gap reference voltage circuitry which provides a stable DC bias over varying temperature and supply voltages. Additionally, the device features a power-down mode, eliminating battery disconnect switches.

Designing with the RF2514

The reference oscillator is built around the onboard transistor at pins 15 and 16. The intended topology is that of a Colpitts oscillator. The Colpitts oscillator is quite common and requires few external components, making it ideal for low cost solutions. The topology of this type of oscillator is as seen in the following figure.



This type of oscillator is a parallel resonant circuit for a fundamental mode crystal. The transistor amplifier is an emitter follower and the voltage gain is developed by the tapped capacitor impedance transformer. The series combination of C_1 and C_2 act in parallel with the input capacitance of the transistor to capacitively load the crystal.

The nominal capacitor values can be calculated with the following equations

$$C_1 = \frac{60 \cdot C_{load}}{freq_{MHz}} \text{ and } C_2 = \frac{1}{\frac{1}{C_{load}} - \frac{1}{C_1}}$$

The load capacitance, C_{load}, is a characteristic of the crystal used; $freq_{MHz}$ is the oscillator frequency in MHz. The frequency can be adjusted by either changing C2 or by placing a variable capacitor in series with the crystal. As an example, assume a desired oscillator frequency of 14MHz and a load capacitance of 32pF. C_1=137.1pF and C_2=41.7pF.

These capacitor values provide a starting point. The drive level of the oscillator should be checked by looking at the signal at the OSC E pin. It has been found that the level at this pin should generally be around 500mV$_{PP}$ or less. This will reduce the reference spur levels and reduce noise produced by distortion. If this level is higher than 500mV$_{PP}$ then decrease the value of C_1. The values of these capacitors are usually adjusted during design to meet performance goals, such as minimizing the start-up time.

An important part of the overall design is the voltage controlled oscillator. The VCO is configured as a differential amplifier. The VCO range is set by the external inductor(s) and is fine-tuned via internal varactor diodes. The varactors are tuned by the loop filter output voltage through a 4kΩ resistor. (Refer to the internal schematic for RESNTR- in the pin description table.) To tune the VCO the designer only needs to calculate the value of the inductor(s) connected to RESNTR- and RESNTR+. The inductor value is determined by the equation:

$$L = \left(\frac{1}{2 \cdot \pi \cdot f}\right)^2 \cdot \frac{1}{C}$$

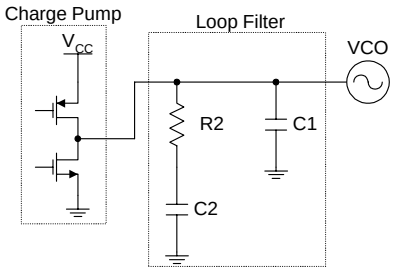
In this equation, f is the desired operating frequency and L is the value of the inductor required. In the case of a two-inductor resonator configuration, the value of L is halved due to the inductors being in each leg. The value C is the amount of capacitance presented by the varactors and parasitics. For calculation purposes, 1.5pF should be used. As an example, assume an operating frequency of 868MHz. The calculated inductor value is 22.4nH. A 22nH inductor (two 10nH inductors for the two-inductor configuration) would be appropriate as the closest available value. Be aware

that any inductance in the traces connecting the inductor(s) to the VCO pins will contribute to the overall resonator inductance and should be subtracted from the calculated value of L.

A parameter of the VCO that is necessary for calculating the loop filter values is the VCO sensitivity, K_{VCO} (sometimes referred to as VCO gain). To determine the VCO sensitivity, first connect the control voltage input point (LOOP FLT pin) to ground and note the frequency. (The frequency can be observed at the output if the LD FLT pin is connected to VCC.) Then connect the same point to the supply and again note the frequency. The difference between these two frequencies divided by the supply voltage is the VCO sensitivity expressed in Hz/V. There is little that the designer can do to increase the VCO sensitivity since it is largely determined by the tuning capacitance of the on-chip varactors. While increasing the inductor value will increase the tuning sensitivity, it will also lower the center frequency of the VCO's tuning range. A very small capacitance (1pF or less) may be added across the VCO pins, which will have the effect of lowering the VCO center frequency and decreasing VCO sensitivity, but this is likely to be neither necessary nor desirable in most applications.

Should adequate centering of the VCO range be unachievable with standard inductor values, two options are available for proper centering. First, a two-inductor resonator may be used with one inductor being one standard value higher than the other. Second, the tuning range of the VCO may be extended at the upper limit of the control voltage by increasing the VCO bias resistor(s). This allows the internal varactor diodes to be slightly forward biased, further increasing the resonator capacitance and thereby extending the lower frequency operation. Care should be taken not to reduce the VCO bias so much that the circuit ceases operation at the minimum required supply voltage.

External to the part, the designer needs to implement a loop filter to complete the PLL. The loop filter converts the output of the charge pump into a voltage that is used to control the VCO. Internally, the VCO is connected to the charge pump output through a 4kΩ resistor. The loop filter is then connected in parallel with this point at pin 12 (LOOP FLT). This limits the loop filter topology to a second order filter usually consisting of a shunt capacitor and a shunt series RC, as shown in the following schematic.



The transfer function is

$$F(s) = R_2 \cdot \left[\frac{s \cdot \tau_2 + 1}{s \cdot \tau_2 \cdot (s \cdot \tau_1 + 1)}\right]$$

where the time constants are defined as

$$\tau_2 = R_2 \cdot C_2 \text{ and } \tau_1 = R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)$$

The frequency at which unity gain occurs is given by

$$\omega_{LBW} = \frac{1}{\sqrt{\tau_1 \cdot \tau_2}}$$

This is defined as the loop bandwidth.

Once the desired phase margin (PM) and loop bandwidth (ω_{LBW}) are chosen, it is possible to calculate the time constants. These are found using the equations

$$\tau_1 = \frac{\sec(PM) - \tan(PM)}{\omega_{LBW}} \text{ and } \tau_2 = \frac{1}{\omega_{LBW}^2 \cdot \tau_1}$$

The phase detector gain, K_{PD}, is calculated by dividing the charge pump current by 2π. For the RF2514, the charge pump current is 100μA.

With these known, it is then possible to determine the values of the filter components.

$$C_1 = \frac{\tau_1}{\tau_2} \cdot \frac{K_{PD} \cdot K_{VCO}}{\omega_{LBW}^2 \cdot N} \cdot \sqrt{\frac{1 + (\omega_{LBW} \cdot \tau_2)^2}{1 + (\omega_{LBW} \cdot \tau_1)^2}}$$

$$C_2 = C_1 \cdot \left(\frac{\tau_2}{\tau_1} - 1\right) \qquad R_2 = \frac{\tau_2}{C_2}$$

As an example, consider a loop bandwidth of 300kHz, a phase margin of 60°, a divide ratio of 64, a K_{VCO} of 33MHz/V, and a K_{PD} of 0.01592mA/2πrad. Time constant τ_1 is 142.15ns, time constant τ_2 is 1.98ms, C_1 is 3.9pF, C_2 is 50.3pF, and R_2 is 39.4kΩ.

The control lines provide an interface for connecting the device to a microcontroller or other signal generating mechanism. The designer can treat pin 5 (MOD IN), pin 14 (DIV CTRL), and pin 2 (PD) as control pins whose voltage level can be set. The lock detect voltage at pin 13 (LD FLT) is an output that can be monitored by the microcontroller.

Pin 5 (MOD IN) is the data input to the modulator and must have a series resistor (R_{MOD_IN}) between it and the raw data source. The value of R_{MOD_IN} and the voltage at its input determine the output power level, with maximum power obtained for R_{MOD_IN}=3kΩ, the minimum allowable resistance. A three-element filter structure (series R, shunt C, series R) has been found to be effective in reducing the out-of-band spectral content by filtering the higher frequency components of the baseband data. For this filter, R_{MOD_IN} is the sum of the two series resistors. The filter values will vary according to the particular data rate of a given application and are best determined experimentally. When the input to R_{MOD_IN} is a high logic level, the carrier is transmitted; when the input is a low logic level, the carrier is not transmitted. For use as a local oscillator (LO) source, simply tie the MOD IN pin to the supply voltage through a suitable series resistor.

Pin 13 (LD FLT) is used to set the threshold of the lock detect circuit. A shunt capacitor is used to set an RC time constant with an on-chip series 1kΩ resistor. The time constant should be approximately 10 times the reference period.

General RF bypassing techniques must be observed to get the best performance. Choose capacitors such that they are series resonant near the frequency of operation.

Board layout is always an area in which great care must be taken. The board material and thickness are used in calculating the RF line widths. The use of vias allows IC and component ground pins to be connected closely to the ground plane, minimizing ground inductance. When laying out the traces around the VCO, it is desirable to keep the parasitics equal between the two legs. This will allow equal valued inductors to be used.

It is recommended that pre-compliance testing be performed during the design process to avoid surprises during final compliance testing, helping to keep the product development and release on schedule. Pre-compliance testing can be done with a GTEM cell, an open area test site, or at a compliance testing laboratory.

After the design has been completed and passes compliance testing, then application will need to be made to obtain final certifications with the respective regulatory bodies for the geographic region in which the product will be operated.

TROUBLESHOOTING GUIDE

The following measurements were obtained from a 915MHz Evaluation Board.

Test conditions are: V_{CC}=3.00V, R_{MOD_IN}=10kΩ, V_{MOD_IN}=V_{CC}.

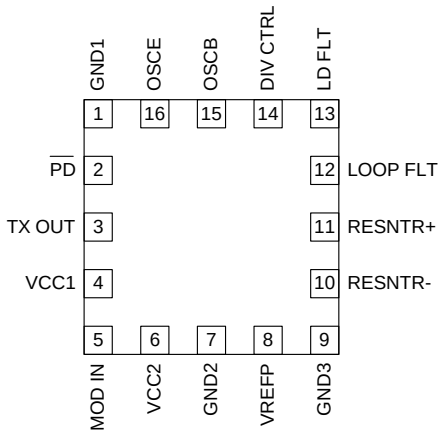
Pin Number	Pin Name	Typical DC Voltage	Ω to GND (Power Off)
1	GND1	0.00	0
2	PD	3.00	2.7M
3	TX OUT	3.00	1.6M
4	VCC1	3.00	1.6M
5	MOD IN	0.90	1.1M
6	VCC2	2.96	1.6M
7	GND2	0.00	0
8	VREF P	0.91	1.1M
9	GND3	0.00	0
10	RESNTR-	2.63	1.6M
11	RESNTR+	2.63	1.6M
12	LOOP FLT	2.52*	1.9M
13	LD FLT	2.77	234k
14	DIV CTL	3.00	1.6M
15	OSC B	2.83	1.7M
16	OSC E	2.00	Open

* Dependent on frequency of operation, board layout, and component variations.

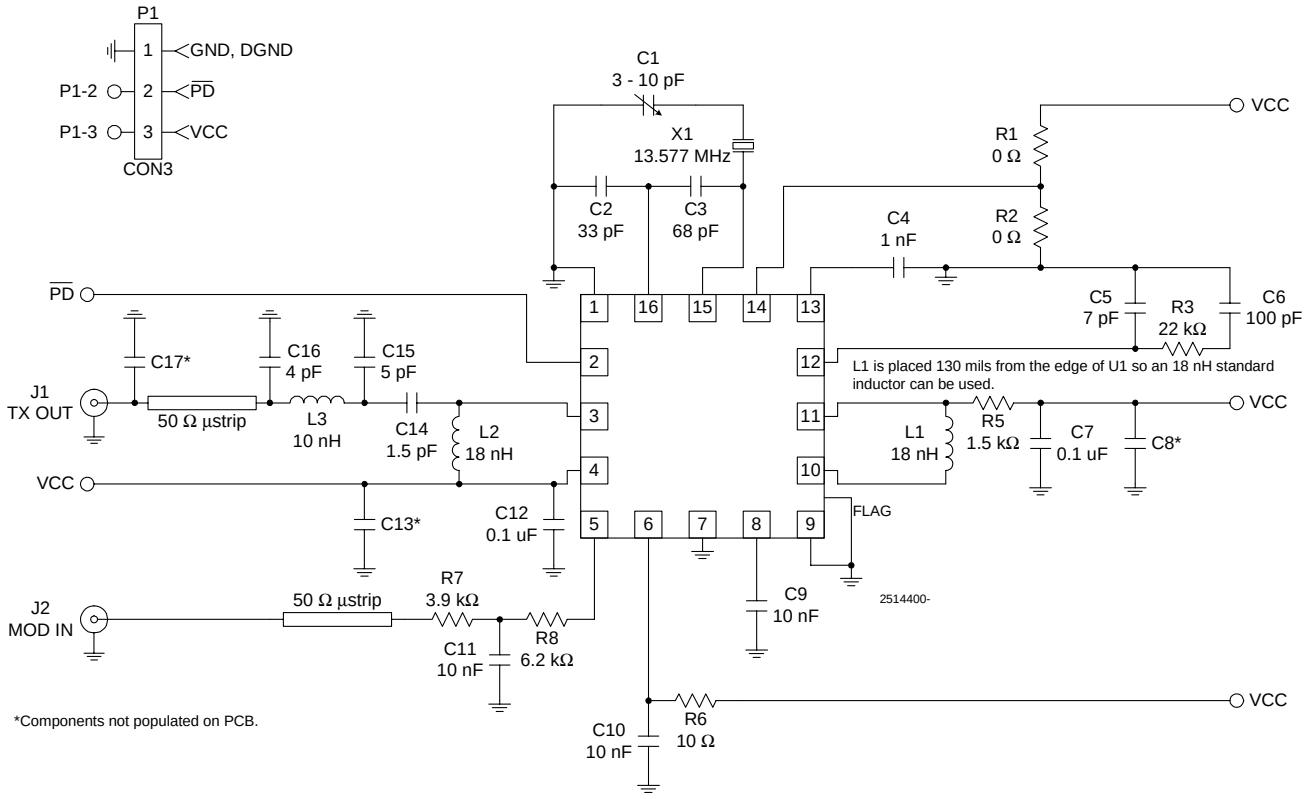
Bibliography

1. Keese, William O., An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phase-Locked Loops: Application Note 1001, National Semiconductor Corp., May 1996.
2. Rhea, Randall W., Oscillator Design and Computer Simulation, 2nd Ed., Atlanta: Noble Publishing, 1995.

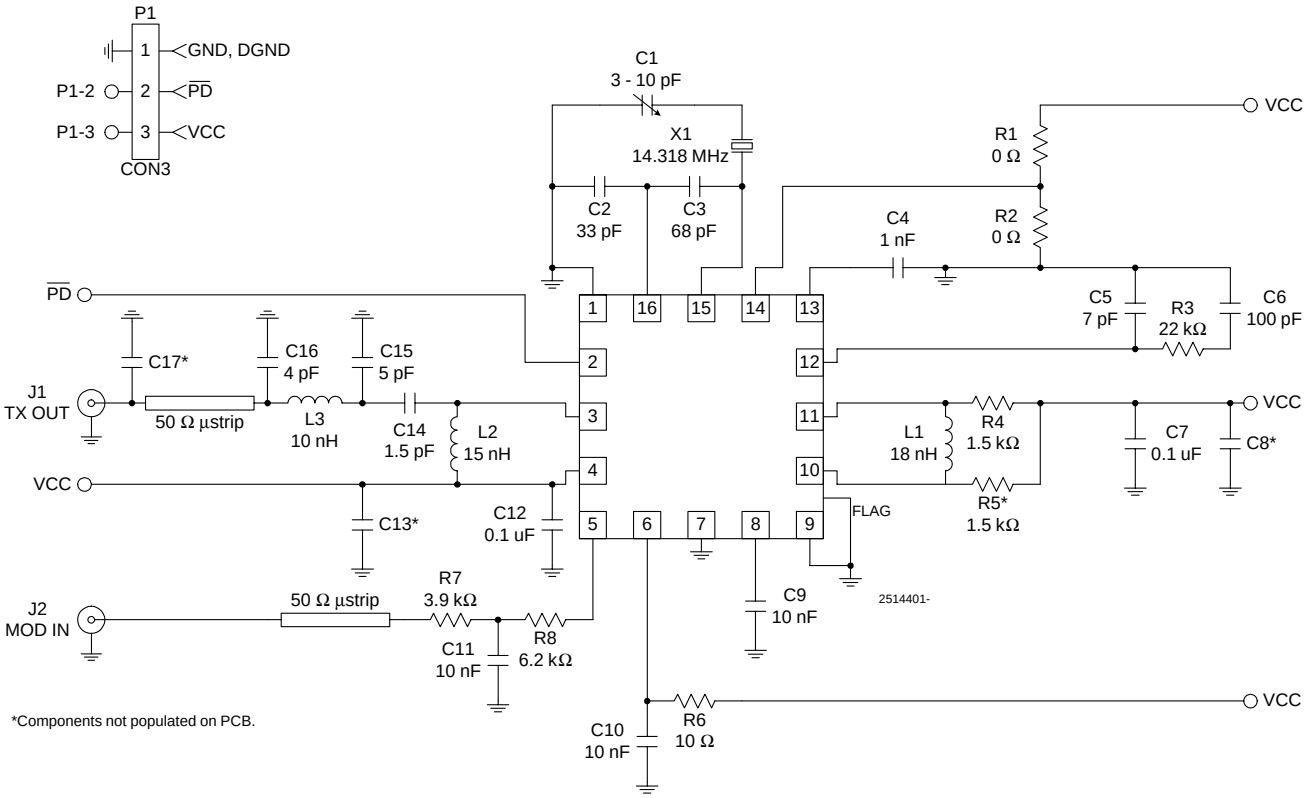
Pin Out


GND1
OSCE
OSCB
DIV CTRL
LD FLT
1
16
15
14
13
PD
2
12
LOOP FLT
TX OUT
3
11
RESNTR+
VCC1
4
10
RESNTR-
5
6
7
8
9
MOD IN
VCC2
GND2
VREFP
GND3

Evaluation Board Schematic
868MHz

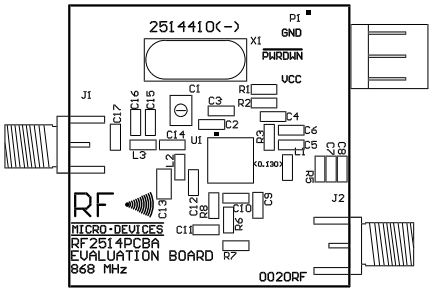


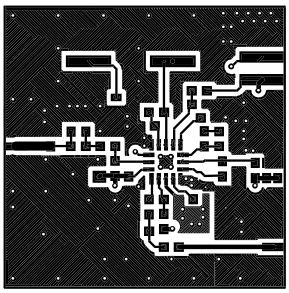
Evaluation Board Schematic
915MHz

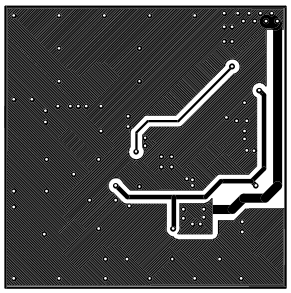


Evaluation Board Layout (868MHz)
Board Size 1.242” x 1.242”

Board Thickness 0.031”, Board Material FR-4







Evaluation Board Layout (915MHz)
Board Size 1.242” x 1.242”

Board Thickness 0.031”, Board Material FR-4

