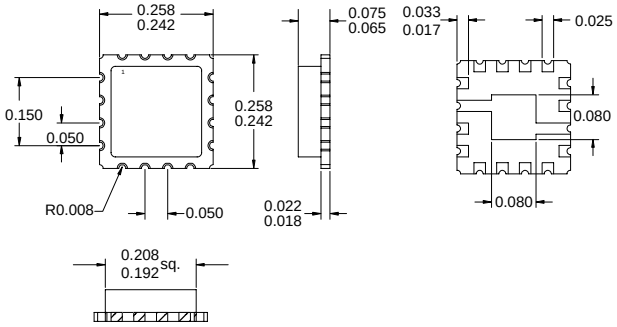
HIGH POWER LINEAR UHF AMPLIFIER

Typical Applications

- 900 MHz ISM Band Applications
- 400 MHz Industrial Radios
- Digital Communication Systems
- Driver Stage for Higher Power Applications
- Commercial and Consumer Systems
- Portable Battery-Powered Equipment

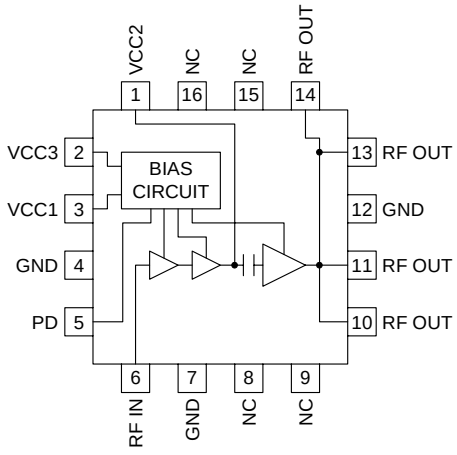
Product Description

The RF2105L is a high power, high efficiency linear amplifier IC. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in digital cellular phone transmitters or ISM applications requiring linear amplification. It is packaged in a 16-lead ceramic package with a backside ground. The device is self-contained with the exception of the output matching network and power supply feed line.



Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Package Style: QLCC-16 Alumina

Features

- Single 2.7V to 6.5V Supply
- Up to 1.2W CW Output Power
- 33dB Small Signal Gain
- 48% Efficiency
- Digitally Controlled Power Down Mode
- Small Package Outline (0.25" x 0.25")

Ordering Information

RF2105L	High Power Linear UHF Amplifier
RF2105L PCBA	Fully Assembled Evaluation Board

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Greensboro, NC 27409, USA
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Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{CC})	-0.5 to +8.5	V_{DC}
Power Down Voltage (V_{PD})	-0.5 to +6.5	V_{DC}
DC Supply Current	700	mA
Input RF Power	+12	dBm
Output Load	20:1	
Operating Case Temperature	-40 to +100	℃
Operating Ambient Temperature	-40 to +85	℃
Storage Temperature	-40 to +150	℃

Caution! ESD sensitive device.

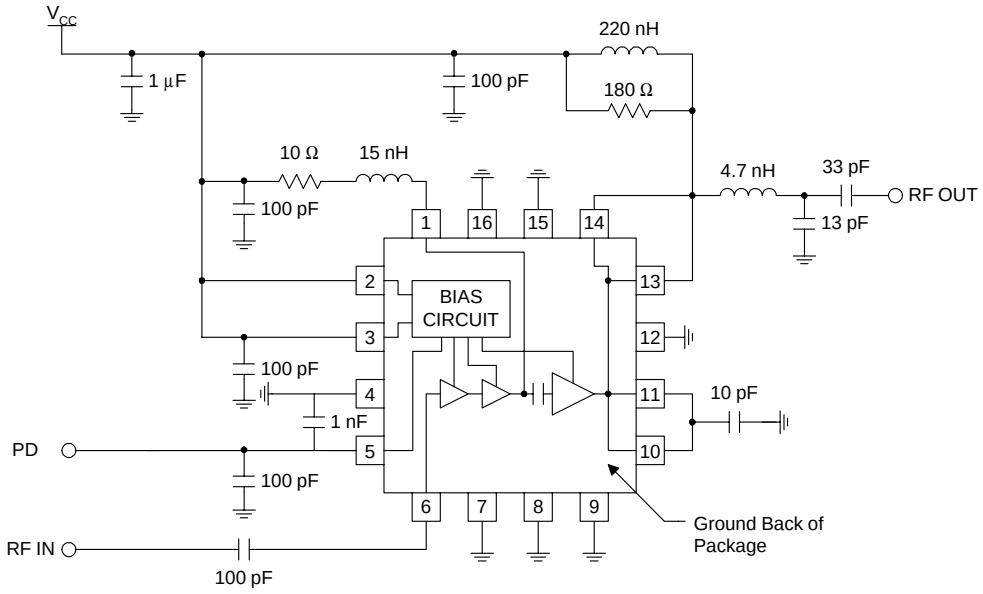
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Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25℃, V_{CC}=5.8V, V_{PD}=5.8V, Z_{LOAD}=9Ω, P_{IN}=0dBm, Freq=840MHz
Frequency Range		430 to 930		MHz	
Maximum CW Output Power		+30.8		dBm	V_{CC}=5.8V, V_{PD}=5.8V, Z_{LOAD}=9Ω Note that increasing V_{CC} above 5.8V does not result in higher output power; power may actually decrease.
		+29.3		dBm	V_{CC}=5.0V, V_{PD}=5.0V, Z_{LOAD}=9Ω
		+28.5		dBm	V_{CC}=4.4V, V_{PD}=4.4V, Z_{LOAD}=9Ω
		+30		dBm	V_{CC}=5.8V, V_{PD}=5.8V, Z_{LOAD}=12Ω
		+27.8		dBm	V_{CC}=5.0V, V_{PD}=5.0V, Z_{LOAD}=12Ω
		+27		dBm	V_{CC}=4.4V, V_{PD}=4.4V, Z_{LOAD}=12Ω
CW Efficiency at Max Output		48		%	
DC Current at Max Output		450		mA	
Small-signal Gain		33		dB	
Second Harmonic		-23		dBc	Without external second harmonic trap
Third Harmonic		-36		dBc	
Fourth Harmonic		-35		dBc	
Input VSWR		<2:1			With external matching network; see application schematic
Input Impedance		50		Ω	With external matching network; see application schematic
Two-Tone Specification					
Average Two-Tone Power		+27.0		dBm	PEP-3dB
IM_3		-30	-25	dBc	P_{OUT}=+24.0dBm/tone
IM_5		-32	-30	dBc	P_{OUT}=+24.0dBm/tone
IM_7		-40		dBc	P_{OUT}=+24.0dBm/tone
Two-Tone Current Drain	225	260	350	mA	
Two-Tone Power-Added Eff.		33		%	
Power Control					
Power Down “ON”		V_{CC}		V	Voltage supplied to the input
Power Down “OFF”		0		V	Voltage supplied to the input
PD Input Current		3.7	5.0	mA	Only in “ON” state
Power Supply					
Power Supply Voltage		2.7 to 6.5		V_{DC}	
Total Idle Current Drain		2	10	μA	V_{PD}<0.1V_{DC}, V_{CC}=6.5V
		60		mA	V_{PD}=4.4V_{DC}, V_{CC}=6.5V
		80		mA	V_{PD}=5.0V_{DC}, V_{CC}=6.5V
	80	100	165	mA	V_{PD}=5.8V_{DC}, V_{CC}=6.5V
		120		mA	V_{PD}=6.5V_{DC}, V_{CC}=6.5V

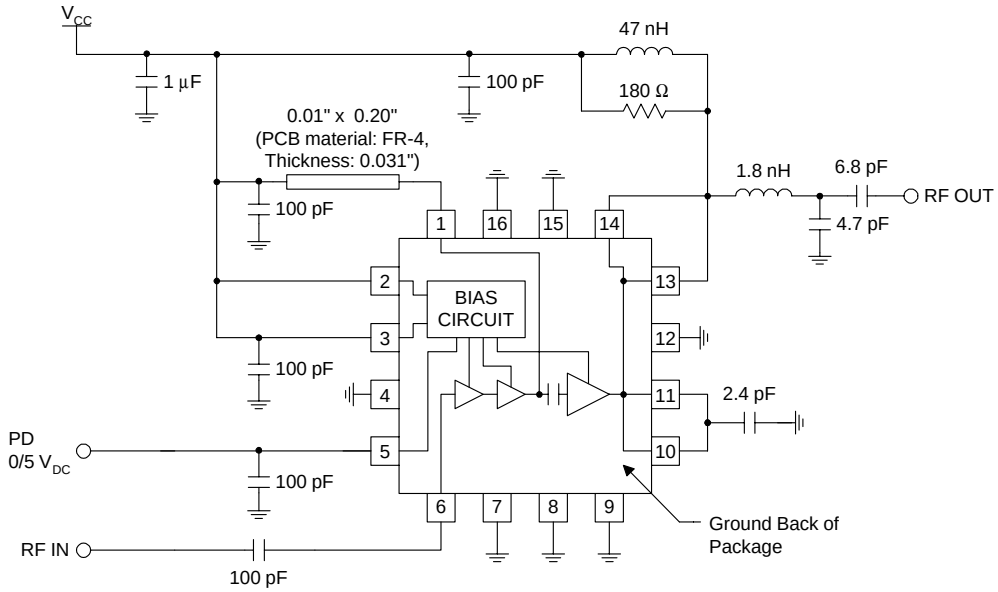
Pin	Function	Description	Interface Schematic
1	VCC2	Positive supply for the second stage (driver) amplifier. This is an unmatched transistor collector output. This pin should see an inductive path to AC ground (V_{CC} with a UHF bypassing capacitor). This inductance can be achieved with a short, thin microstrip line or with a low value chip inductor (~2.7nH). At lower frequencies, the inductance value should be larger (longer microstrip line) and V_{CC} should be bypassed with a larger bypass capacitor (see the application schematic for 430MHz operation). This inductance forms a matching network with the internal series capacitor between the second and third stages, setting the amplifier's frequency of maximum gain. An additional 1µF bypass capacitor in parallel with the UHF bypass capacitor is also recommended, but placement of this component is not as critical. In most applications, pins 1, 2, and 3 can share a single 1µF bypass capacitor.	
2	VCC3	Positive supply for the active bias circuits. This pin can be externally combined with pin 3 (VCC1) and the pair bypassed with a single UHF capacitor, placed as close as possible to the package. Additional bypassing of 1µF is also recommended, but proximity to the package is not as critical. In most applications, pins 1, 2, and 3 can share a single 1µF bypass capacitor.	
3	VCC1	Positive supply for the first stage (input) amplifier. This pin can be externally combined with pin 2 (VCC3) and the pair bypassed with a single UHF capacitor, placed as close as possible to the package. Additional bypassing of 1µF is also recommended, but proximity to the package is not as critical. In most applications, pins 1, 2, and 3 can share a single 1µF bypass capacitor.	
4	GND	Ground connection. For best performance, keep traces physically short and connect immediately to ground plane. In addition, for specified performance, the package's backside metal should be soldered to ground plane.	
5	PD	Power down control voltage. When this pin is at 0V, the device will be in power down mode, dissipating minimum DC power. When this pin is at V_{CC} (3V to 6.5V), the device will be in full power mode delivering maximum available gain and output power capability. This pin may also be used to perform some degree of gain control or power control when set to voltages between 0V and V_{CC}. It is not optimized for this function so the transfer function is not linear over a wide range as with other devices specifically designed for analog gain control; however, it may be usable for coarse adjustment or in some closed loop AGC systems. This pin should not, in any circumstance, be higher in voltage than V_{CC}, nor should it ever be higher than 6.5V. This pin should also have an external UHF bypassing capacitor.	
6	RF IN	Amplifier RF input. This is a 50Ω RF input port to the amplifier. It does not contain internal DC-blocking and therefore should be externally DC-blocked before connecting to any device which has DC present or which contains a DC path to ground. A series UHF capacitor is recommended for the DC-blocking.	
7	GND	Same as pin 4.	
8	NC	Not internally connected.	
9	NC	Not internally connected.	

Pin	Function	Description	Interface Schematic
10	RF OUT	Amplifier RF output. This is an unmatched collector output of the final amplifier transistor. It is internally connected to pins 10, 11, 13, and 14 to provide low series inductance and flexibility in output matching. Bias for the final power amplifier output transistor must also be provided through two of these four pins. Typically, pins 10 and 11 are connected to a network that creates a second harmonic trap. For 830MHz operation, this network is simply a single 2.4pF capacitor from both pins to ground. This capacitor series resonates with internal bond wires at two times the operating frequency, effectively shorting out the second harmonic. Shorting out this harmonic serves to increase the amplifier's maximum output power and efficiency, as well as to lower the level of the second harmonic output. Typically, pins 13 and 14 are externally connected very close to the package and used as the RF output with a matching network that presents the optimum load impedance to the PA for maximum power and efficiency, as well as providing DC-blocking at the output. An additional network of a bias inductor and parallel resistor provides DC bias and helps to protect the output from high voltage swings due to severe load mismatches. Shunt protection diodes are included to clip peak voltage excursions above ~15V to prevent voltage breakdown in worst case conditions.	
11	RF OUT	Same as pin 10.	
12	GND	Same as pin 4.	
13	RF OUT	Same as pin 10.	
14	RF OUT	Same as pin 10.	
15	NC	Not internally connected.	
16	NC	Not internally connected.	
Pkg Base	GND	This contact is the main ground contact for the entire device. Care should be taken to ensure that this contact is well soldered in order to prevent performance from being degraded from that indicated in the specifications.	

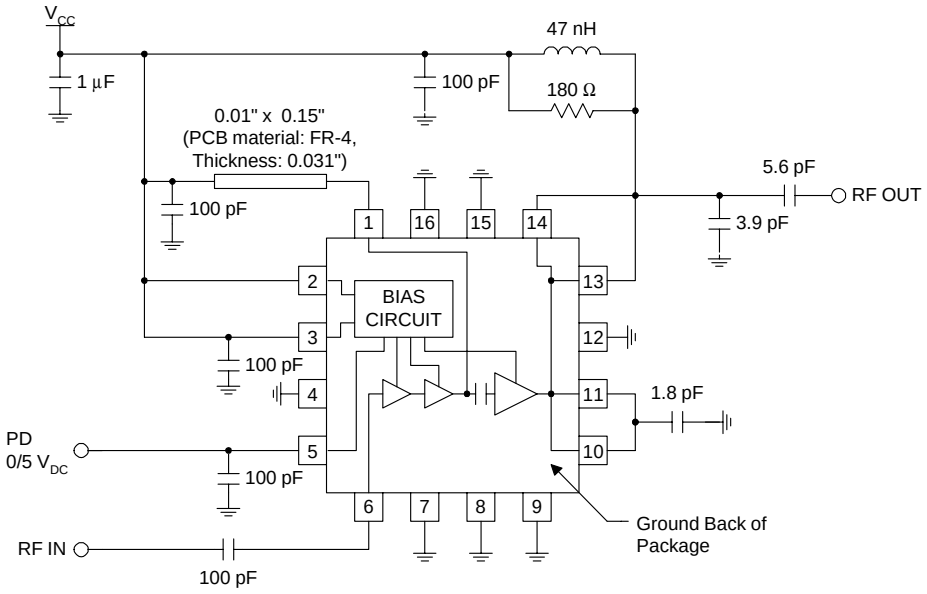
Application Schematic for 430MHz Operation



Application Schematic for 840MHz Operation

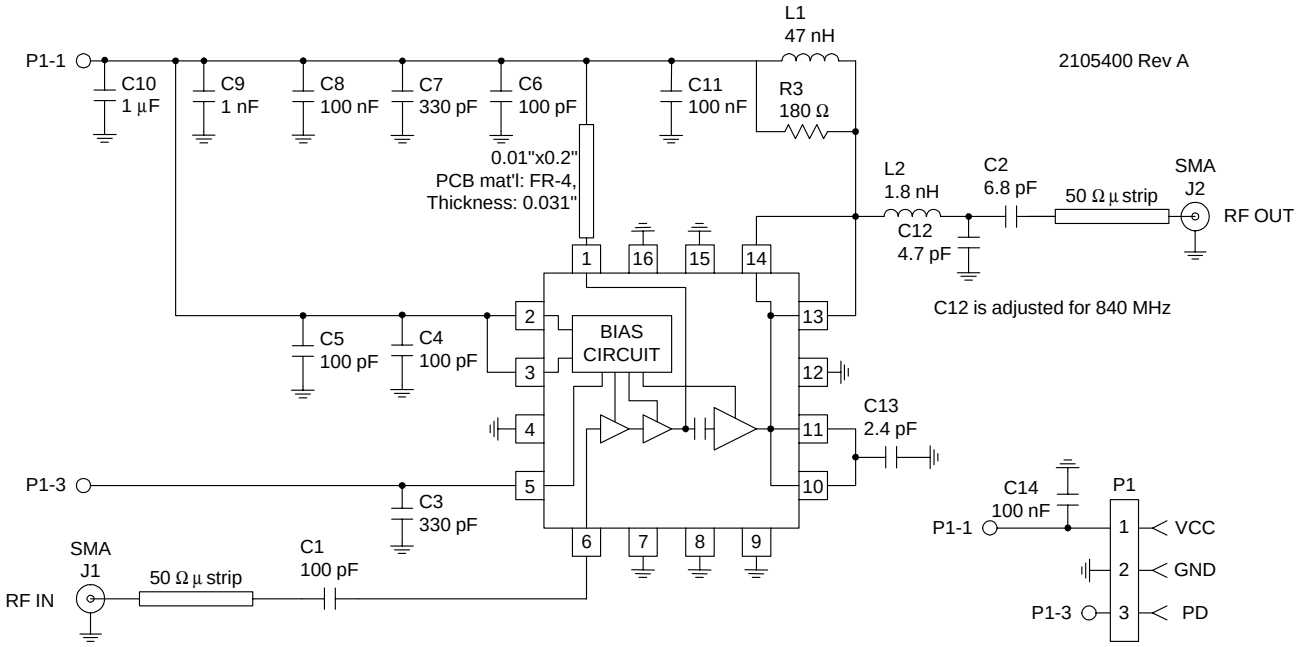


Application Schematic for 915MHz Operation



Evaluation Board Schematic (840MHz)

(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 3.020” x 2.020”
Board Thickness 0.031”, Board Material FR-4

