TEXAS INSTRUMENTS

REF2025, REF2030, REF2033, REF2041

SBOS600D – MAY 2014 – REVISED JULY 2018

REF20xx Low-Drift, Low-Power, Dual-Output, V_{REF} and V_{REF} / 2 Voltage References

1 Features

- Two Outputs, V_{REF} and V_{REF} / 2, for Convenient Use in Single-Supply Systems
- Excellent Temperature Drift Performance:
  - 8 ppm/°C (max) from –40°C to 125°C
- High Initial Accuracy: ±0.05% (max)
- V_{REF} and V_{BIAS} Tracking over Temperature:
  - 6 ppm/°C (max) from –40°C to 85°C
  - 7 ppm/°C (max) from –40°C to 125°C
- Microsize Package: SOT23-5
- Low Dropout Voltage: 10 mV
- High Output Current: ±20 mA
- Low Quiescent Current: 360 µA
- Line Regulation: 3 ppm/V
- Load Regulation: 8 ppm/mA
- Matte-Sn version (REF2025AISDDCR) for improved corrosion resistance in the Battelle Class III and similar harsh environments

2 Applications

- Digital Signal Processing:
  - Power Inverters
  - Motor Controls
- Current Sensing
- Industrial Process Controls
- Medical Equipment
- Data Acquisition Systems
- Single-Supply Systems

3 Description

Applications with only a positive supply voltage often require additional stable voltage in the middle of the analog-to-digital converter (ADC) input range to bias input bipolar signals. The REF20xx provides a reference voltage (V_{REF}) for the ADC and a second highly-accurate voltage (V_{BIAS}) that can be used to bias the input bipolar signals.

The REF20xx offers excellent temperature drift (8 ppm/°C, max) and initial accuracy (0.05%) on both the V_{REF} and V_{BIAS} outputs while operating at a quiescent current less than 430 µA. In addition, the V_{REF} and V_{BIAS} outputs track each other with a precision of 6 ppm/°C (max) across the temperature range of –40°C to 85°C. All these features increase the precision of the signal chain and decrease board space, while reducing the cost of the system as compared to a discrete solution. Extremely low dropout voltage of only 10 mV allows operation from very low input voltages, which can be very useful in battery-operated systems.

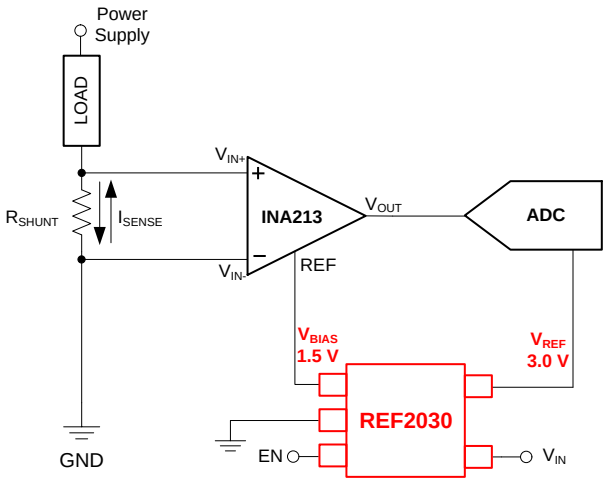
Both the V_{REF} and V_{BIAS} voltages have the same excellent specifications and can sink and source current equally well. Very good long-term stability and low noise levels make these devices ideally-suited for high-precision industrial applications.

Device Information(1)

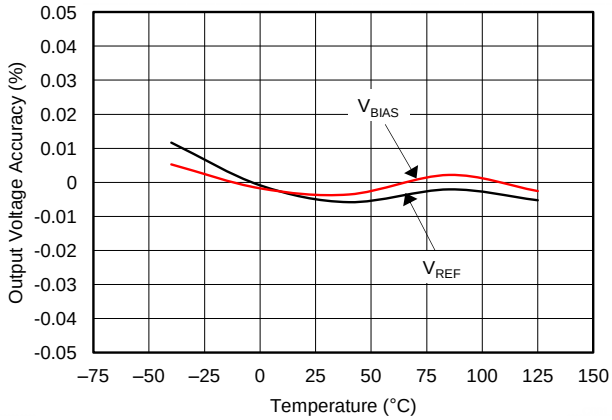
PART NAME	PACKAGE	BODY SIZE (NOM)
REF20xx	SOT (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Application Example



V_{REF} and V_{BIAS} vs Temperature



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2017) to Revision D — **Page**

- Changed application information to include corrosion resistance advantages. ... 18

Changes from Revision B (July 2014) to Revision C — **Page**

- Added I/O column to *Pin Functions* table ... 3
- Added *Storage temperature* parameter to *Absolute Maximum Ratings* table (moved from *ESD Ratings* table) ... 4
- Changed *ESD Rating* table: changed title, updated table format ... 4

Changes from Revision A (June 2014) to Revision B — **Page**

- Changed device status to Production Data from Mixed Status ... 1
- Deleted footnote 2 from Device Information table ... 1
- Deleted footnote from Device Comparison Table ... 3
- Added Thermal Information table ... 4

Changes from Original (May 2014) to Revision A — **Page**

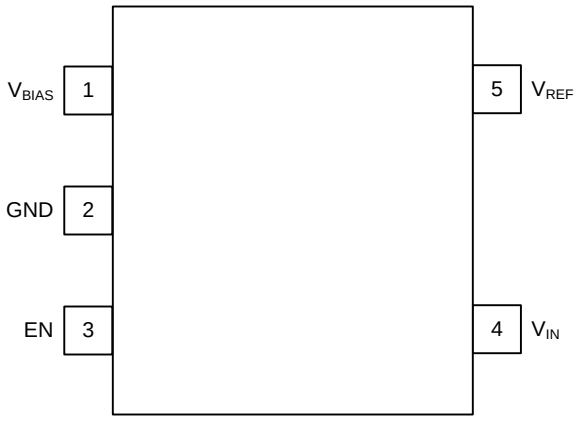
- Made changes to product preview data sheet ... 1

5 Device Comparison Table

PRODUCT	V_{REF}	V_{BIAS}
REF2025	2.5 V	1.25 V
REF2030	3.0 V	1.5 V
REF2033	3.3 V	1.65 V
REF2041	4.096 V	2.048 V

6 Pin Configuration and Functions

DDC Package
SOT23-5
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{BIAS}	Output	Bias voltage output (V_{REF} / 2)
2	GND	—	Ground
3	EN	Input	Enable (EN ≥ V_{IN} – 0.7 V, device enabled)
4	V_{IN}	Input	Input supply voltage
5	V_{REF}	Output	Reference voltage output (V_{REF})

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	V_{IN}	–0.3	6	V
	EN	–0.3	V_{IN} + 0.3	
Temperature	Operating	–55	150	°C
	Junction, T_j		150	
	Storage, T_{stg}	–65	170	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage range (I_L = 0 mA, T_A = 25°C)	V_{REF} + 0.02(1)		5.5	V

(1) See Figure 28 in Typical Characteristics for minimum input voltage at different load currents and temperature

7.4 Thermal Information

THERMAL METRIC(1)		REF20xx DDC (SOT23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	34.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

At T_A = 25°C, I_L = 0 mA, and V_{IN} = 5 V, unless otherwise noted. Both V_{REF} and V_{BIAS} have the same specifications.

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT								
	Output voltage accuracy				–0.05%		0.05%	
	Output voltage temperature coefficient(1)		–40°C ≤ T_A ≤ 125°C			±3	±8	ppm/°C
	V_{REF} and V_{BIAS} tracking over temperature(2)		–40°C ≤ T_A ≤ 85°C			±1.5	±6	ppm/°C
			–40°C ≤ T_A ≤ 125°C			±2	±7	
LINE AND LOAD REGULATION								
$\Delta V_{O(\Delta VI)}$	Line regulation		V_{REF} + 0.02 V ≤ V_{IN} ≤ 5.5 V			3	35	ppm/V
$\Delta V_{O(\Delta IL)}$	Load regulation	Sourcing	0 mA ≤ I_L ≤ 20 mA , V_{REF} + 0.6 V ≤ V_{IN} ≤ 5.5 V			8	20	ppm/mA
		Sinking	0 mA ≤ I_L ≤ –20 mA, V_{REF} + 0.02 V ≤ V_{IN} ≤ 5.5 V			8	20	
POWER SUPPLY								
I_{CC}	Supply current	Active mode				360	430	µA
			–40°C ≤ T_A ≤ 125°C				460	
		Shutdown mode				3.3	5	
			–40°C ≤ T_A ≤ 125°C				9	
	Enable voltage		Device in shutdown mode (EN = 0)		0		0.7	V
			Device in active mode (EN = 1)		V_{IN} – 0.7		V_{IN}	
	Dropout voltage					10	20	mV
			I_L = 20 mA				600	
I_{SC}	Short-circuit current					50		mA
t_{on}	Turn-on time		0.1% settling, C_L = 1 µF			500		µs
NOISE								
	Low-frequency noise(3)		0.1 Hz ≤ f ≤ 10 Hz			12		ppm_{PP}
	Output voltage noise density		f = 100 Hz			0.25		$ppm/\sqrt{Hz}$
CAPACITIVE LOAD								
	Stable output capacitor range				0		10	µF
HYSTERESIS AND LONG TERM STABILITY								
	Long-term stability		0 to 1000 hours			60		ppm
	Output voltage hysteresis(4)		25°C, –40°C, 125°C, 25°C	Cycle 1		60		ppm
				Cycle 2		35		

(1) Temperature drift is specified according to the box method. See the *Feature Description* section for more details.
(2) The V_{REF} and V_{BIAS} tracking over temperature specification is explained in more detail in the *Feature Description* section.
(3) The peak-to-peak noise measurement procedure is explained in more detail in the *Noise Performance* section.
(4) The thermal hysteresis measurement procedure is explained in more detail in the *Thermal Hysteresis* section.

7.6 Typical Characteristics

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5-V power supply, C_L = 0 µF, and 2.5-V output, unless otherwise noted.

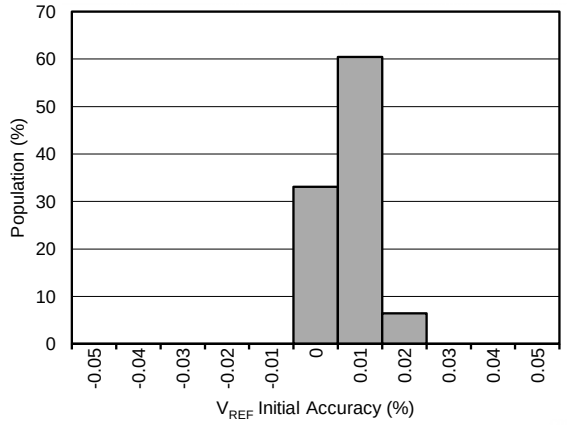
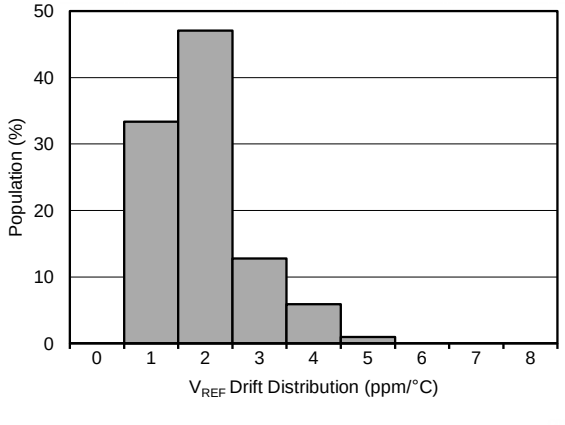


Figure 1. Initial Accuracy Distribution (V_{REF})



–40°C ≤ T_A ≤ 125°C

Figure 2. Drift Distribution (V_{REF})

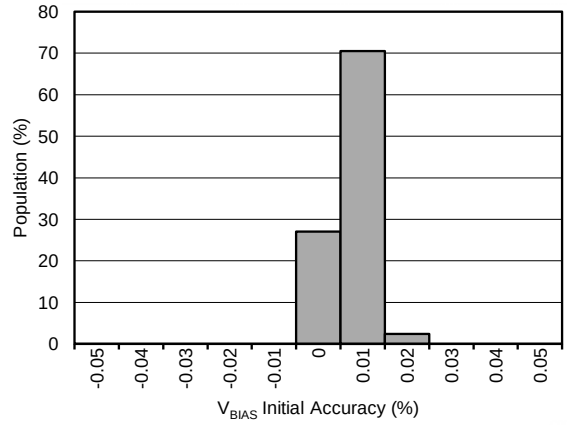
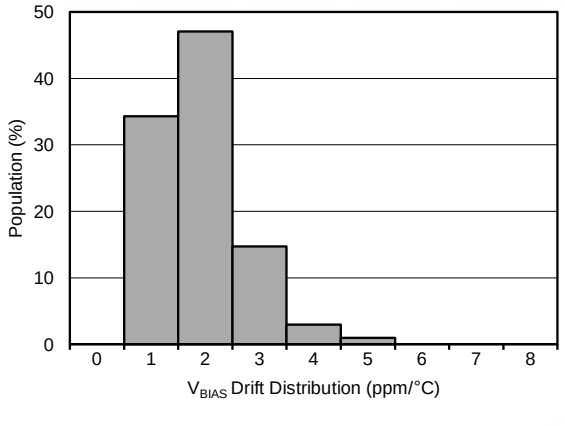


Figure 3. Initial Accuracy Distribution (V_{BIAS})



–40°C ≤ T_A ≤ 125°C

Figure 4. Drift Distribution (V_{BIAS})

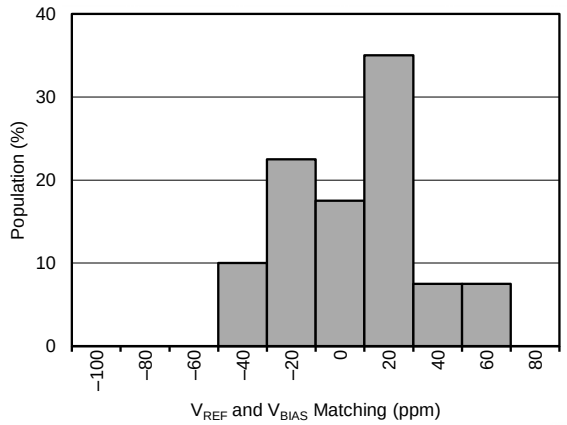
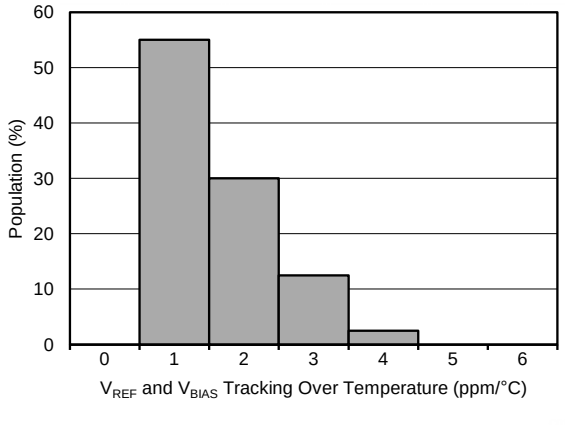


Figure 5. V_{REF} – 2 × V_{BIAS} Distribution

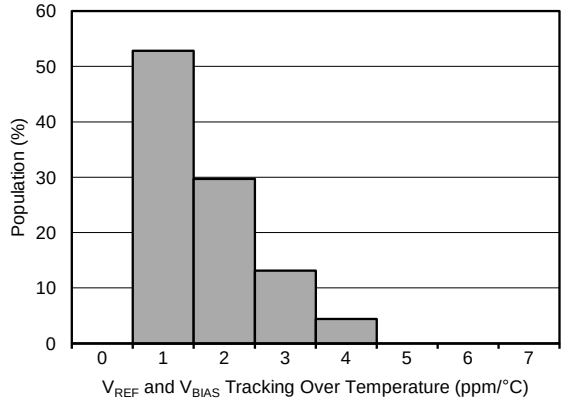


–40°C ≤ T_A ≤ 85°C

Figure 6. Distribution of V_{REF} – 2 × V_{BIAS} Drift Tracking Over Temperature

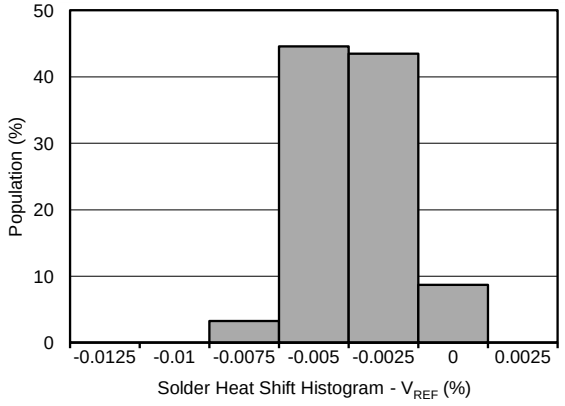
Typical Characteristics (continued)

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5-V power supply, C_L = 0 µF, and 2.5-V output, unless otherwise noted.



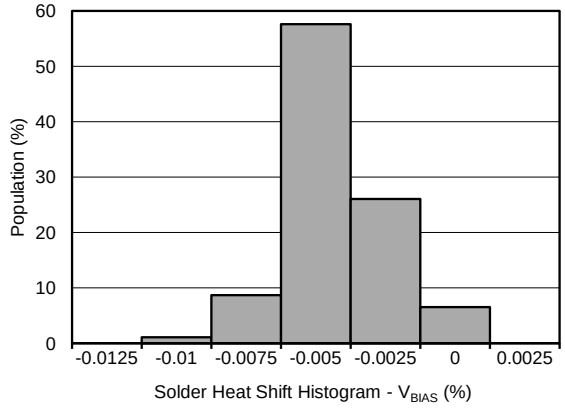
–40°C ≤ T_A ≤ 125°C

Figure 7. Distribution of V_{REF} – 2 × V_{BIAS} Drift Tracking Over Temperature



Refer to the *Solder Heat Shift* section for more information.

Figure 8. Solder Heat Shift Distribution (V_{REF})



Refer to the *Solder Heat Shift* section for more information.

Figure 9. Solder Heat Shift Distribution (V_{BIAS})

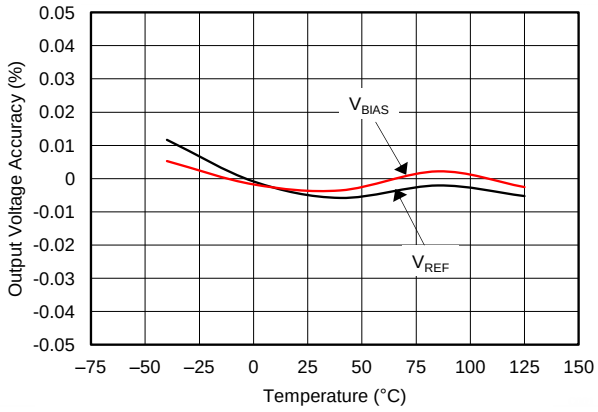


Figure 10. Output Voltage Accuracy (V_{REF}) vs Temperature

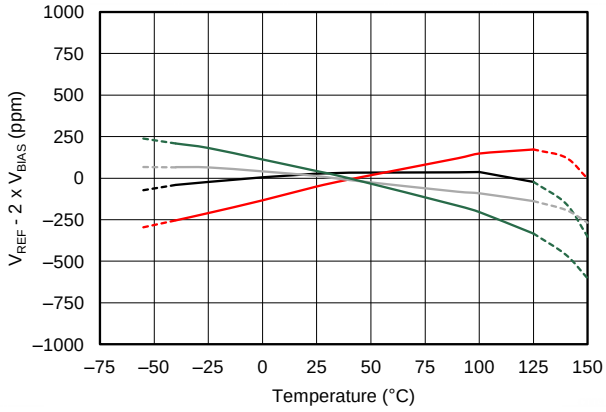
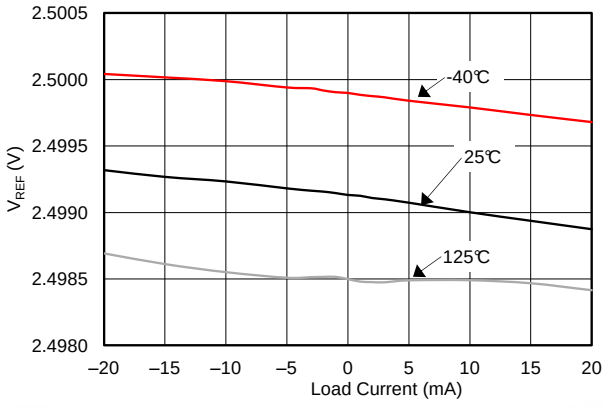


Figure 11. V_{REF} – 2 × V_{BIAS} Tracking vs Temperature



V_{REF} output

Figure 12. Output Voltage Change vs Load Current (V_{REF})

Typical Characteristics (continued)

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5-V power supply, C_L = 0 µF, and 2.5-V output, unless otherwise noted.

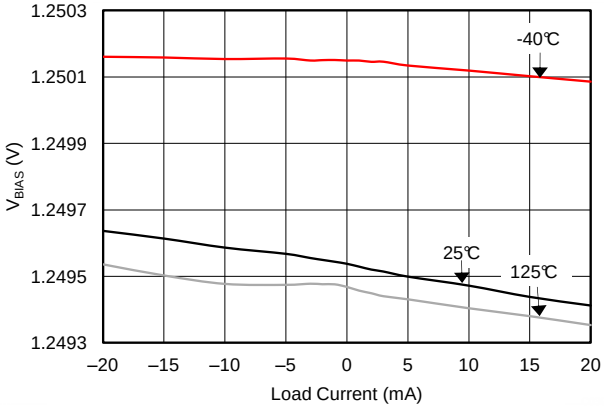


Figure 13. Output Voltage Change vs Load Current (V_{BIAS})

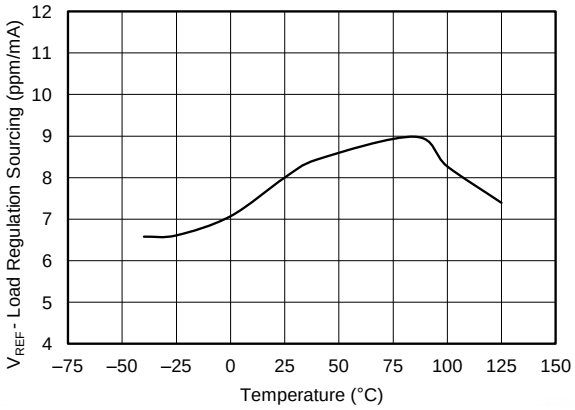


Figure 14. Load Regulation Sourcing vs Temperature (V_{REF})

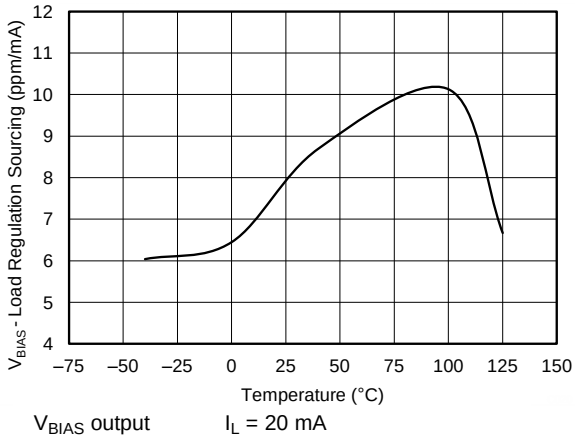


Figure 15. Load Regulation Sourcing vs Temperature (V_{BIAS})

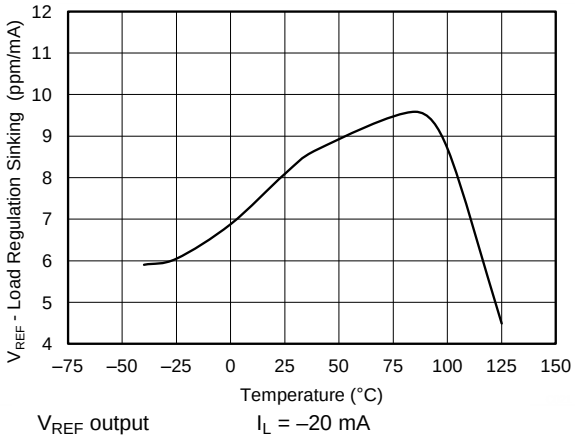


Figure 16. Load Regulation Sinking vs Temperature (V_{REF})

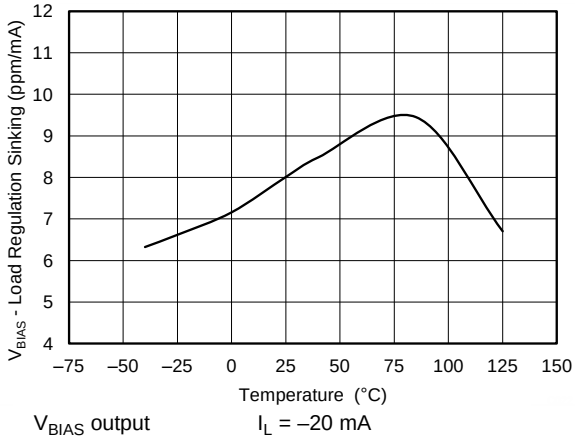


Figure 17. Load Regulation Sinking vs Temperature (V_{BIAS})

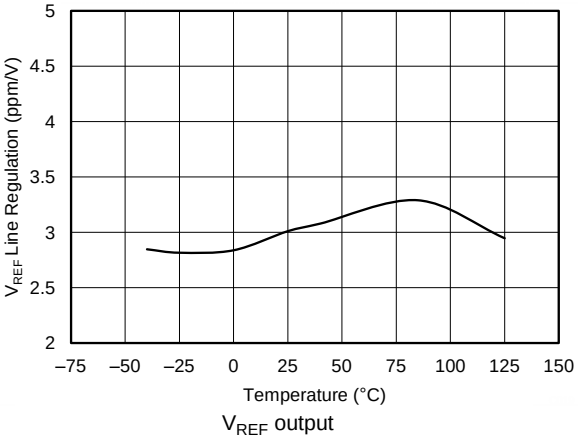
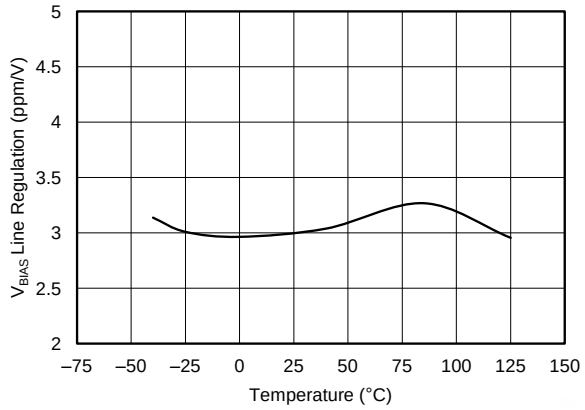


Figure 18. Line Regulation vs Temperature (V_{REF})

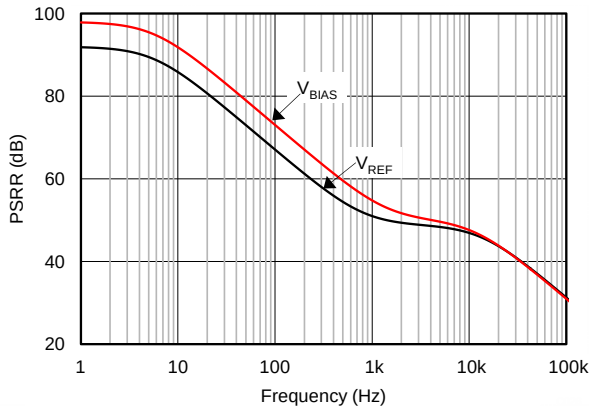
Typical Characteristics (continued)

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5-V power supply, C_L = 0 µF, and 2.5-V output, unless otherwise noted.



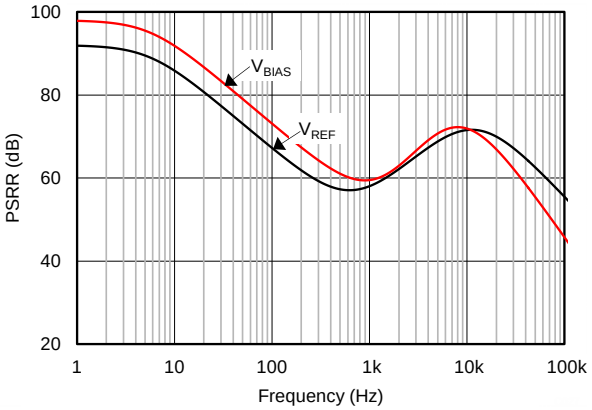
V_{BIAS} output

Figure 19. Line Regulation vs Temperature (V_{BIAS})



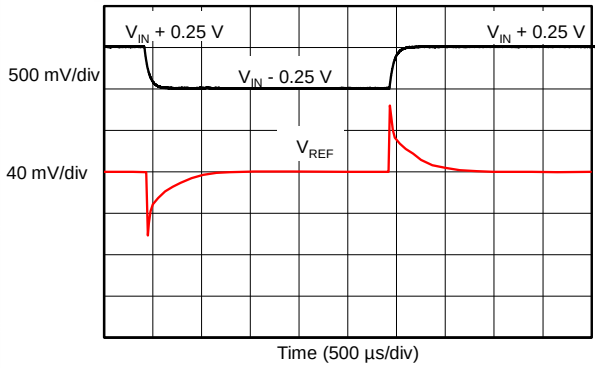
C_L = 0 µF

Figure 20. Power-Supply Rejection Ratio vs Frequency



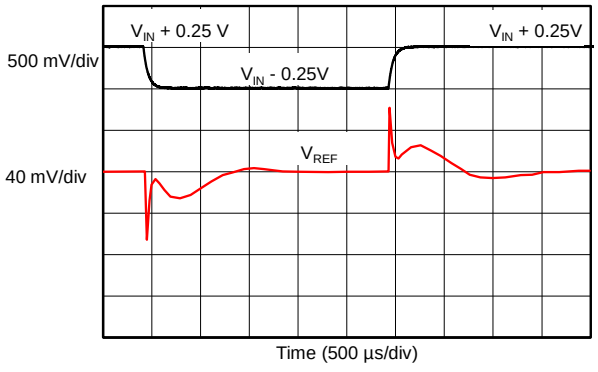
C_L = 10 µF

Figure 21. Power-Supply Rejection Ratio vs Frequency



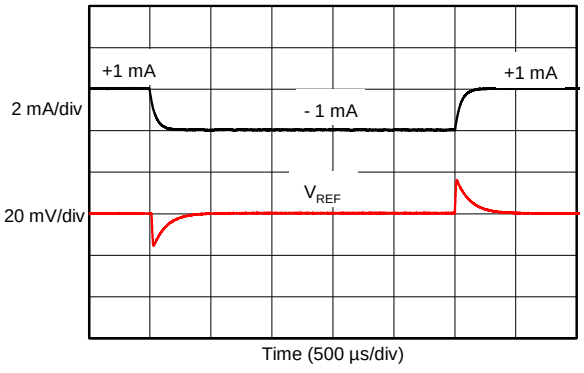
C_L = 1 µF

Figure 22. Line Transient Response



C_L = 10 µF

Figure 23. Line Transient Response

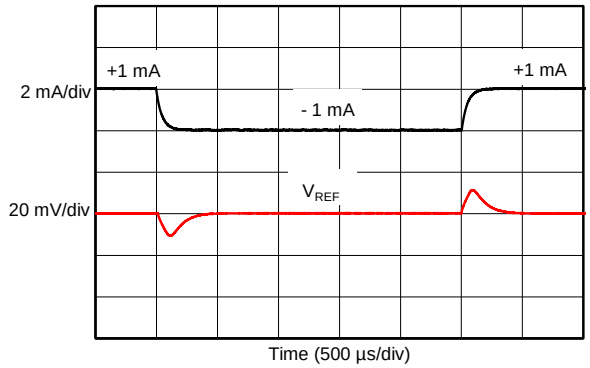


C_L = 1 µF I_L = ±1-mA step

Figure 24. Load Transient Response

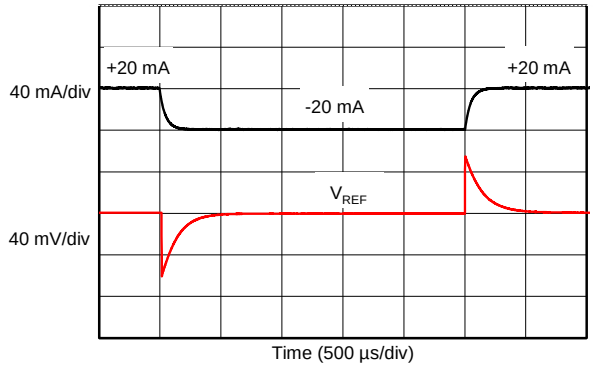
Typical Characteristics (continued)

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5-V power supply, C_L = 0 µF, and 2.5-V output, unless otherwise noted.



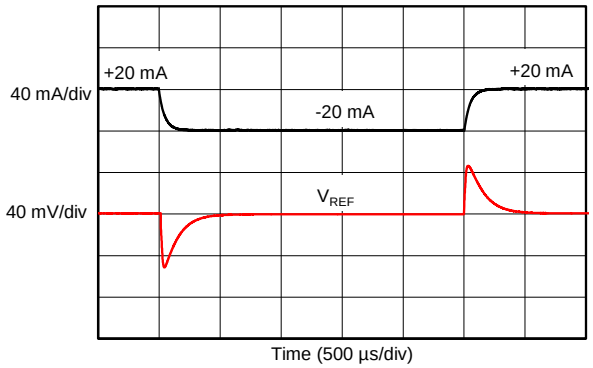
C_L = 10 µF I_L = ±1-mA step

Figure 25. Load Transient Response



C_L = 1 µF I_L = ±20-mA step

Figure 26. Load Transient Response



C_L = 10 µF I_L = ±20-mA step

Figure 27. Load Transient Response

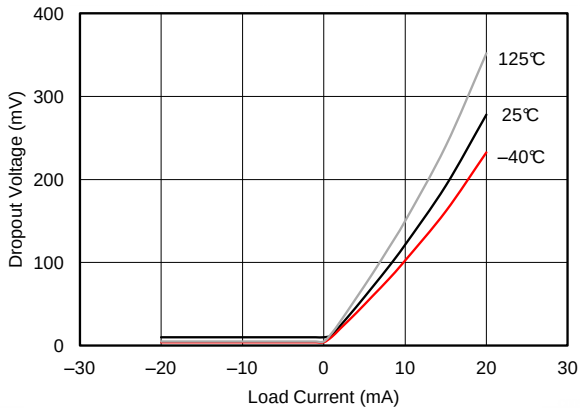
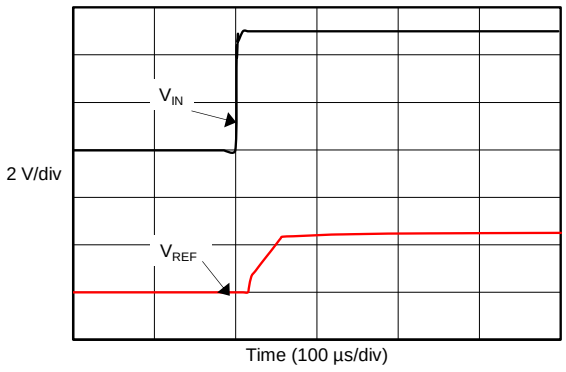
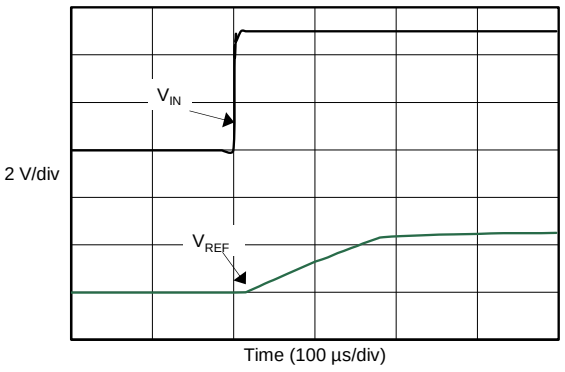


Figure 28. Minimum Dropout Voltage vs Load Current



C_L = 1 µF

Figure 29. Turn-On Settling Time



C_L = 10 µF

Figure 30. Turn-On Settling Time

Typical Characteristics (continued)

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5-V power supply, C_L = 0 µF, and 2.5-V output, unless otherwise noted.

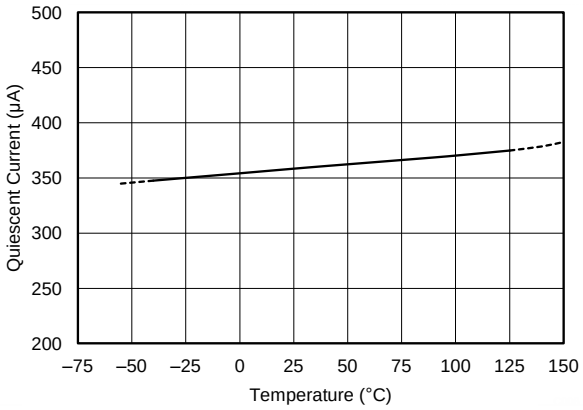


Figure 31. Quiescent Current vs Temperature

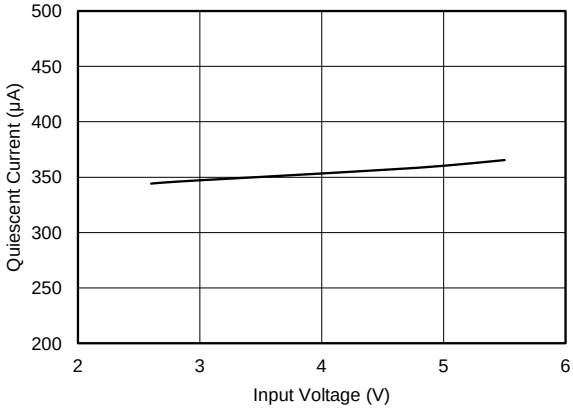
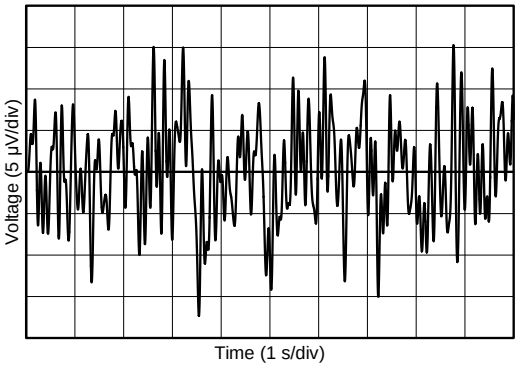
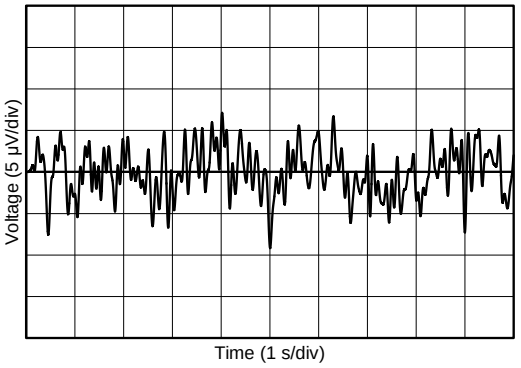


Figure 32. Quiescent Current vs Input Voltage



V_{REF} output

Figure 33. 0.1-Hz to 10-Hz Noise (V_{REF})



V_{BIAS} output

Figure 34. 0.1-Hz to 10-Hz Noise (V_{BIAS})

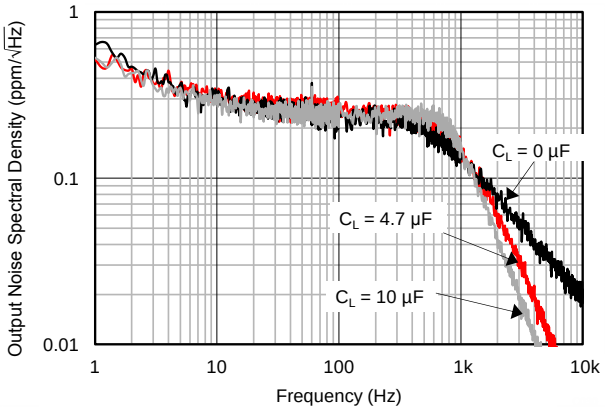
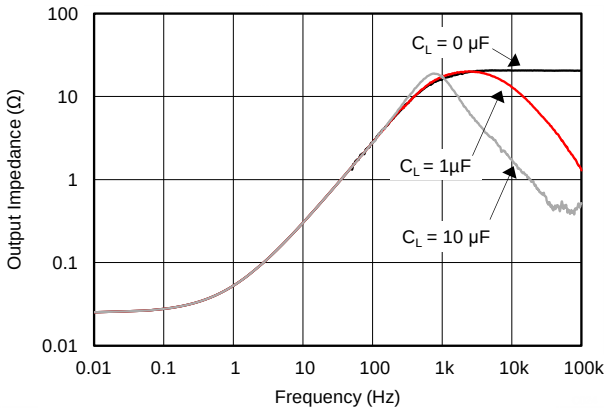


Figure 35. Output Voltage Noise Spectrum



V_{REF} output

Figure 36. Output Impedance vs Frequency (V_{REF})

Typical Characteristics (continued)

At T_A = 25°C, I_L = 0 mA, V_{IN} = 5-V power supply, C_L = 0 µF, and 2.5-V output, unless otherwise noted.

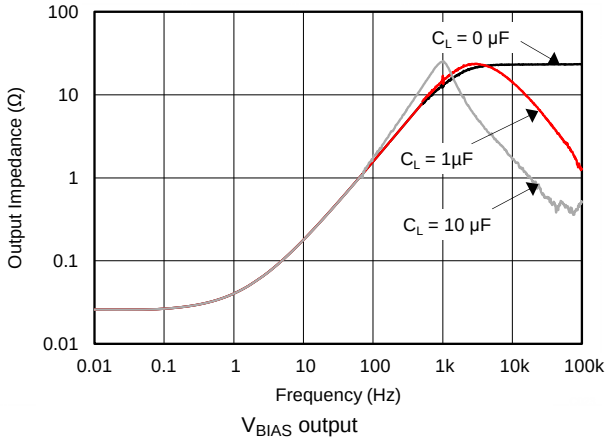


Figure 37. Output Impedance vs Frequency (V_{BIAS})

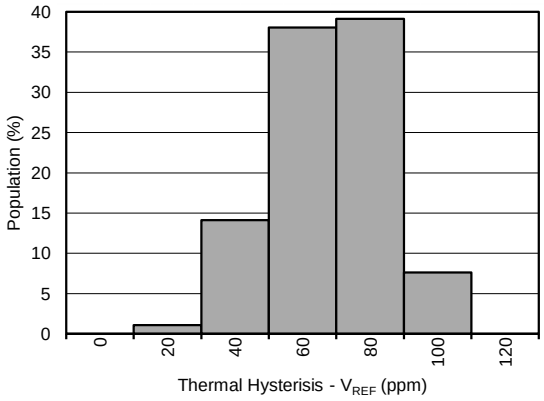


Figure 38. Thermal Hysteresis Distribution (V_{REF})

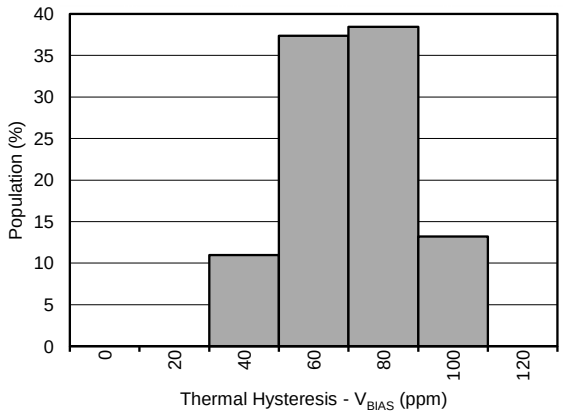


Figure 39. Thermal Hysteresis Distribution (V_{BIAS})

8 Parameter Measurement Information

8.1 Solder Heat Shift

The materials used in the manufacture of the REF20xx have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

In order to illustrate this effect, a total of 92 devices were soldered on four printed circuit boards [23 devices on each printed circuit board (PCB)] using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in Figure 40. The printed circuit board is comprised of FR4 material. The board thickness is 1.57 mm and the area is 171.54 mm × 165.1 mm.

The reference and bias output voltages are measured before and after the reflow process; the typical shift is displayed in Figure 41 and Figure 42. Although all tested units exhibit very low shifts (< 0.01%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device should be soldered in the second pass to minimize its exposure to thermal stress.

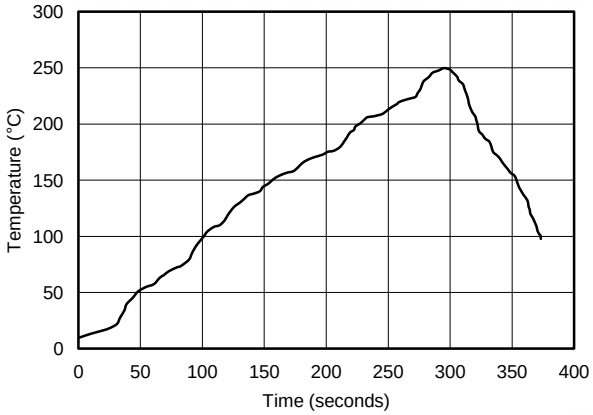


Figure 40. Reflow Profile

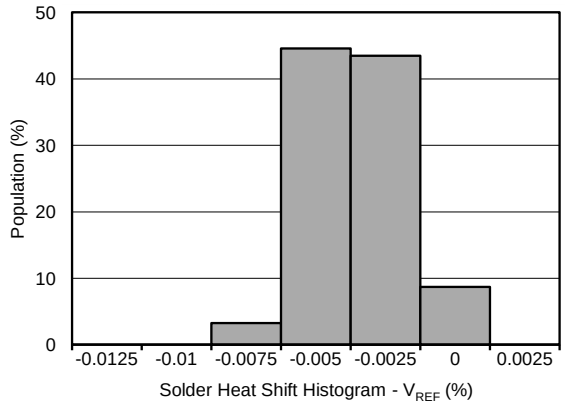


Figure 41. Solder Heat Shift Distribution, V_{REF} (%)

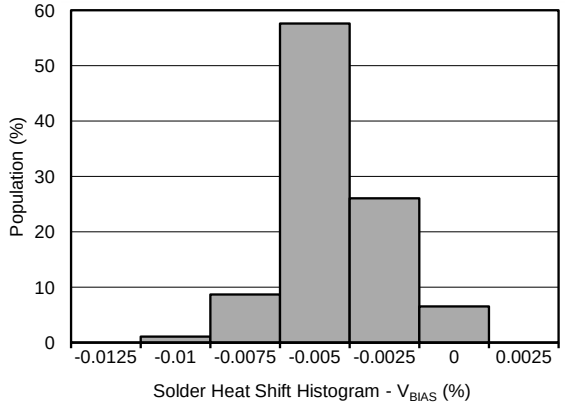


Figure 42. Solder Heat Shift Distribution, V_{BIAS} (%)

8.2 Thermal Hysteresis

Thermal hysteresis is measured with the REF20xx soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Hysteresis can be expressed by Equation 1:

$$V_{HYST} = \left(\frac{\left| V_{PRE} - V_{POST} \right|}{V_{NOM}} \right) \bullet 10^6 \quad \text{(ppm)} \tag{1}$$

where

- V_{HYST} = thermal hysteresis (in units of ppm),
- V_{NOM} = the specified output voltage,
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling, and
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to 125°C and returns to 25°C.

Typical thermal hysteresis distribution is as shown in Figure 43 and Figure 44.

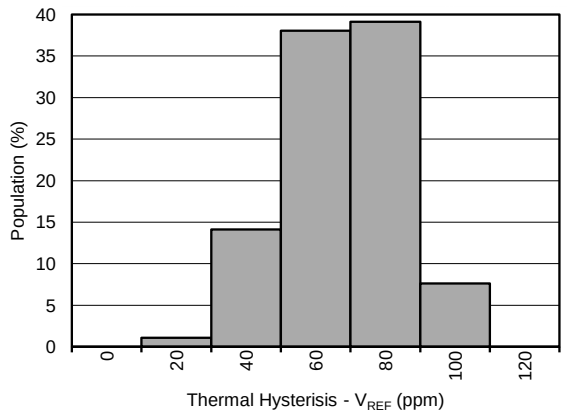


Figure 43. Thermal Hysteresis Distribution (V_{REF})

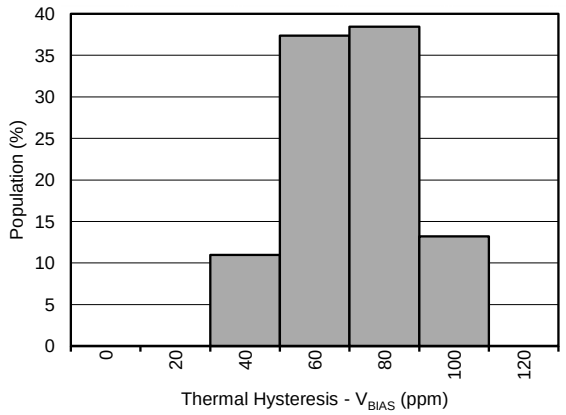


Figure 44. Thermal Hysteresis Distribution (V_{BIAS})

8.3 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise can be seen in Figure 45 and Figure 46. Device noise increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade ac performance. Peak-to-peak noise measurement setup is shown in Figure 47.

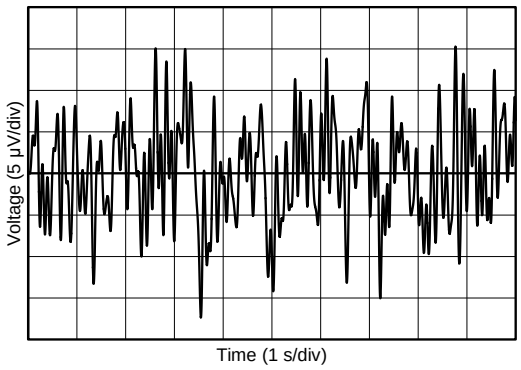


Figure 45. 0.1-Hz to 10-Hz Noise (V_{REF})

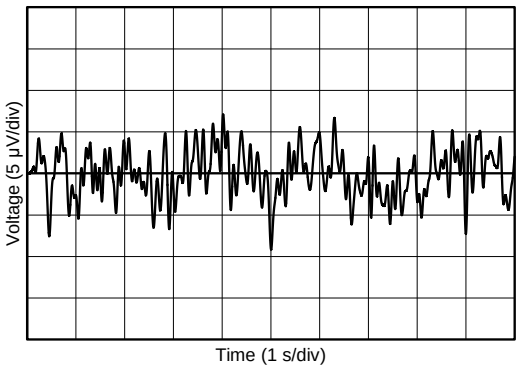


Figure 46. 0.1-Hz to 10-Hz Noise (V_{BIAS})

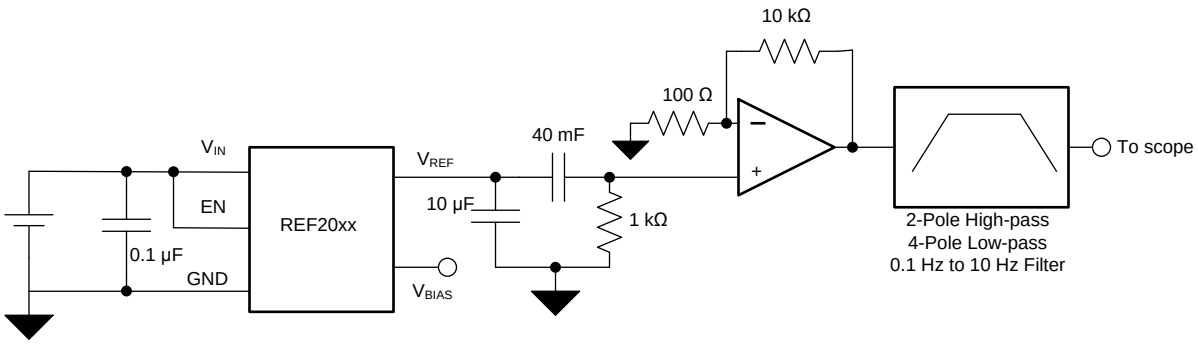


Figure 47. 0.1-Hz to 10-Hz Noise Measurement Setup

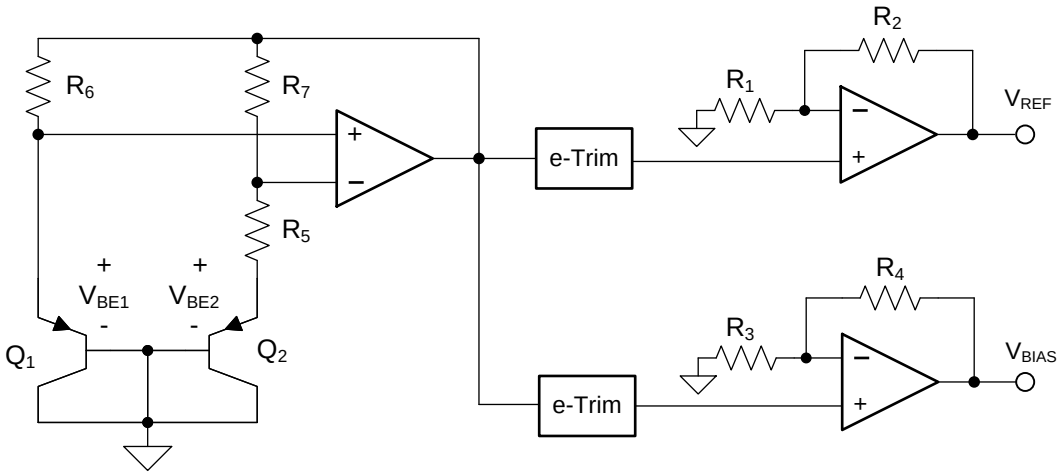
9 Detailed Description

9.1 Overview

The REF20xx are a family of dual-output, V_{REF} and V_{BIAS} (V_{REF} / 2) band-gap voltage references. The *Functional Block Diagram* section provides a block diagram of the basic band-gap topology and the two buffers used to derive the V_{REF} and V_{BIAS} outputs. Transistors Q_1 and Q_2 are biased such that the current density of Q_1 is greater than that of Q_2. The difference of the two base emitter voltages (V_{BE1} – V_{BE2}) has a positive temperature coefficient and is forced across resistor R_5. The voltage is amplified and added to the base emitter voltage of Q_2, which has a negative temperature coefficient. The resulting band-gap output voltage is almost independent of temperature. Two independent buffers are used to generate V_{REF} and V_{BIAS} from the band-gap voltage. The resistors R_1, R_2 and R_3, R_4 are sized such that V_{BIAS} = V_{REF} / 2.

e-Trim™ is a method of package-level trim for the initial accuracy and temperature coefficient of V_{REF} and V_{BIAS}, implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent transistor mismatch, as well as errors induced during package molding. e-Trim is implemented in the REF20xx to minimize the temperature drift and maximize the initial accuracy of both the V_{REF} and V_{BIAS} outputs.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 V_{REF} and V_{BIAS} Tracking

Most single-supply systems require an additional stable voltage in the middle of the analog-to-digital converter (ADC) input range to bias input bipolar signals. The V_{REF} and V_{BIAS} outputs of the REF20xx are generated from the same band-gap voltage as shown in the *Functional Block Diagram* section. Hence, both outputs track each other over the full temperature range of –40°C to 125°C with an accuracy of 7 ppm/°C (max). The tracking accuracy increases to 6 ppm/°C (max) when the temperature range is limited to –40°C to 85°C. The tracking error is calculated using the box method, as described by Equation 2:

$$\text{Tracking Error} = \left(\frac{V_{DIFF(MAX)} - V_{DIFF\ (MIN)}}{V_{REF} \bullet \text{Temperature Range}} \right) \bullet 10^6 \quad \text{(ppm)}$$

where

- $V_{DIFF} = V_{REF} - 2 \bullet V_{BIAS}$ (2)

Feature Description (continued)

The tracking accuracy is as shown in Figure 48.

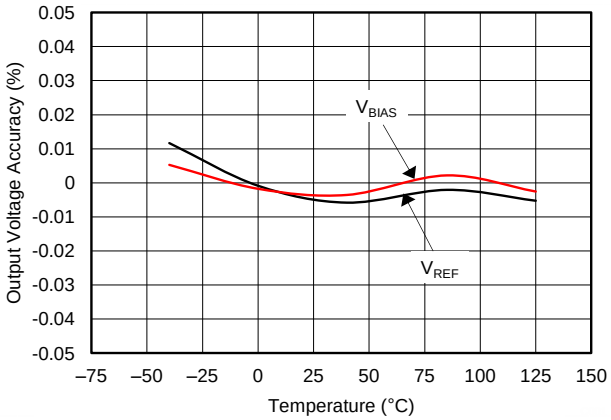


Figure 48. V_{REF} and V_{BIAS} Tracking vs Temperature

9.3.2 Low Temperature Drift

The REF20xx is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by Equation 3:

$$\text{Drift} = \left(\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF} \bullet \text{Temperature Range}} \right) \bullet 10^6 \quad \text{(ppm)} \tag{3}$$

9.3.3 Load Current

The REF20xx family is specified to deliver a current load of ±20 mA per output. Both the V_{REF} and V_{BIAS} outputs of the device are protected from short circuits by limiting the output short-circuit current to 50 mA. The device temperature increases according to Equation 4:

$$T_J = T_A + P_D \bullet R_{\theta JA} \tag{4}$$

where

- T_J = junction temperature (°C),
- T_A = ambient temperature (°C),
- P_D = power dissipated (W), and
- $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

The REF20xx maximum junction temperature must not exceed the absolute maximum rating of 150°C.

9.4 Device Functional Modes

When the EN pin of the REF20xx is pulled high, the device is in active mode. The device should be in active mode for normal operation. The REF20xx can be placed in a low-power mode by pulling the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 5 µA in shutdown mode. See the *Electrical Characteristics* for logic high and logic low voltage levels.

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The low-drift, bidirectional, single-supply, low-side, current-sensing solution, described in this section, can accurately detect load currents from –2.5 A to 2.5 A. The linear range of the output is from 250 mV to 2.75 V. Positive current is represented by output voltages from 1.5 V to 2.75 V, whereas negative current is represented by output voltages from 250 mV to 1.5 V. The difference amplifier is the INA213 current-shunt monitor, whose supply and reference voltages are supplied by the low-drift REF2030.

Industrial applications with electronics in corrosive environments are susceptible to corrosive damage due to the exposure to heat, moisture, and corrosive gases. The combination of the following conditions in a given system lead to higher risk of corrosive damage:

1. Ventilated enclosures exposing underlying PCB.
2. PCBs not conformally coated.
3. Exposed-lead components with plating susceptible to corrosion.
4. Changes in plating techniques for RoHS compliance (e.g. removal of Pb (lead) and certain types of plating).

To improve resistance to corrosion in harsh environments, the REF2025AISDDCR uses Matte-Sn plating with improved assembly process to reduce exposed Cu, leading to improved corrosion resistance in the Battelle Class III and similar harsh environments. The "S" in the part number identifies this special plating option. REF2025 versions that do not have the "S" will continue to be available in industry standard NiPdAu processing technique.

10.2 Typical Application

10.2.1 Low-Side, Current-Sensing Application

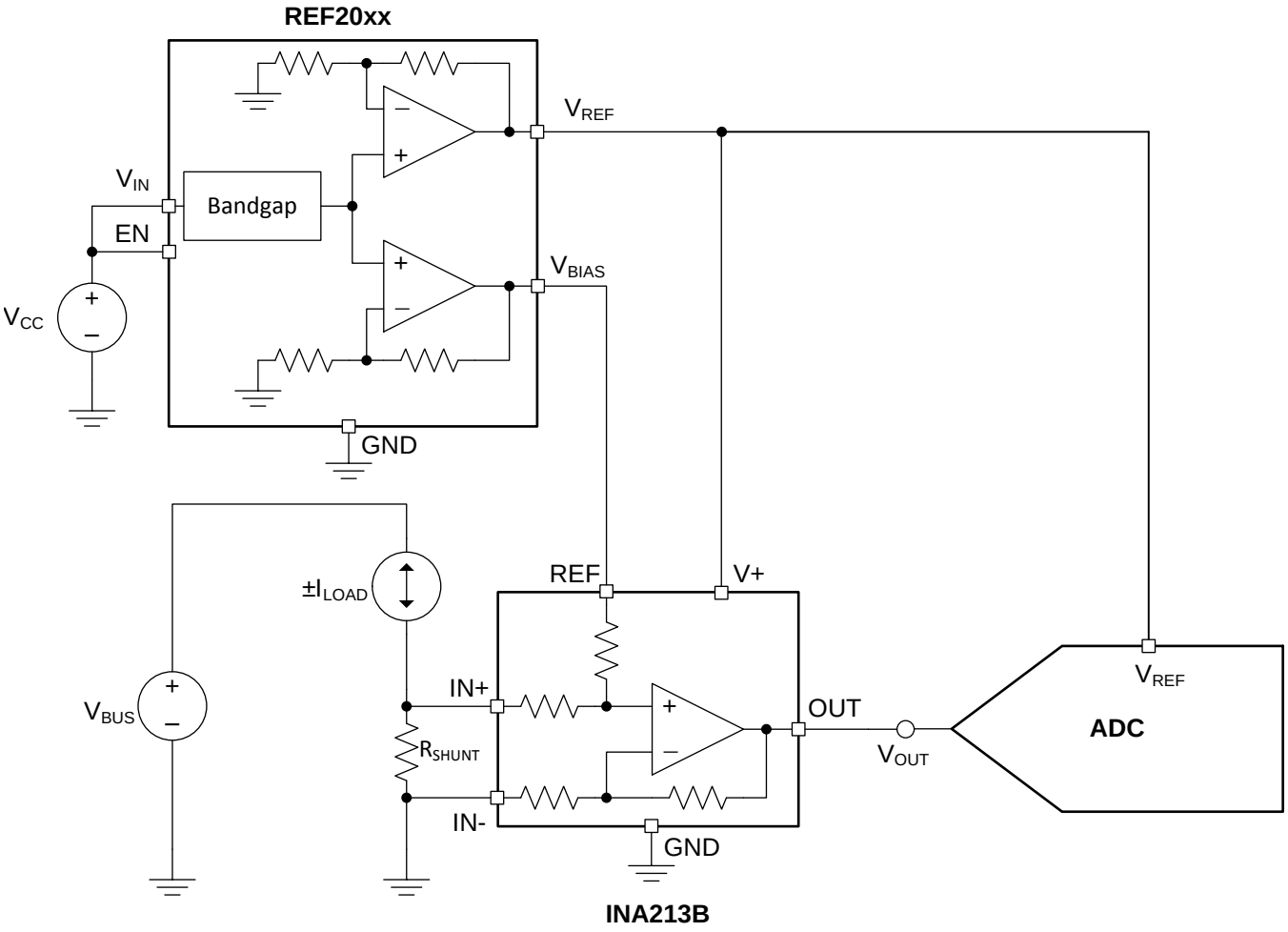


Figure 49. Low-Side, Current-Sensing Application

Typical Application (continued)

10.2.1.1 Design Requirements

The design requirements are as follows:

1. Supply voltage: 5.0 V
2. Load current: ±2.5 A
3. Output: 250 mV to 2.75 V
4. Maximum shunt voltage: ±25 mV

10.2.1.2 Detailed Design Procedure

Low-side current sensing is desirable because the common-mode voltage is near ground. Therefore, the current-sensing solution is independent of the bus voltage, V_{BUS}. When sensing bidirectional currents, use a differential amplifier with a reference pin. This procedure allows for the differentiation between positive and negative currents by biasing the output stage such that it can respond to negative input voltages. There are a variety of methods for supplying power (V+) and the reference voltage (V_{REF}, or V_{BIAS}) to the differential amplifier. For a low-drift solution, use a monolithic reference that supplies both power and the reference voltage. Figure 50 shows the general circuit topology for a low-drift, low-side, bidirectional, current-sensing solution. This topology is particularly useful when interfacing with an ADC; see Figure 49. Not only do V_{REF} and V_{BIAS} track over temperature, but their matching is much better than alternate topologies. For a more detailed version of the design procedure, refer to TIDU357.

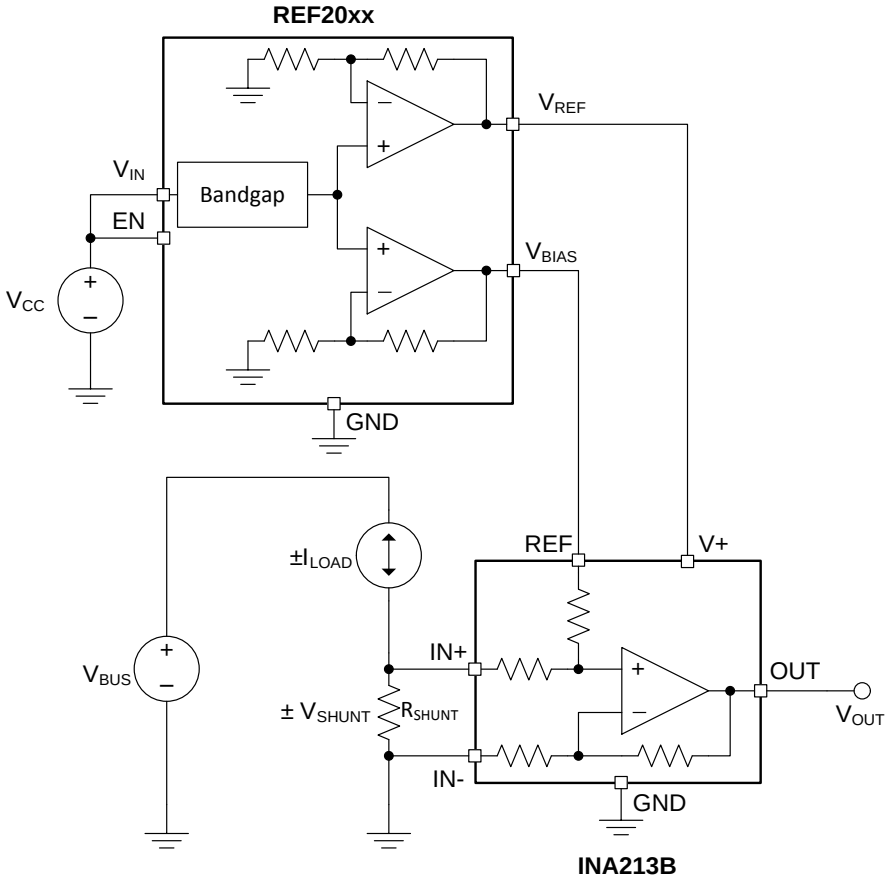


Figure 50. Low-Drift, Low-side, Bidirectional, Current-Sensing Circuit Topology

The transfer function for the circuit given in Figure 50 is as shown in Equation 5:

$$V_{OUT} = G \bullet (\pm V_{SHUNT}) + V_{BIAS}$$
$$= G \bullet (\pm I_{LOAD} \bullet R_{SHUNT}) + V_{BIAS} \quad (5)$$

Typical Application (continued)

10.2.1.2.1 Shunt Resistor

As illustrated in Figure 50, the value of V_{SHUNT} is the ground potential for the system load. If the value of V_{SHUNT} is too large, issues may arise when interfacing with systems whose ground potential is actually 0 V. Also, a value of V_{SHUNT} that is too negative may violate the input common-mode voltage of the differential amplifier in addition to potential interfacing issues. Therefore, limiting the voltage across the shunt resistor is important. Equation 6 can be used to calculate the maximum value of R_{SHUNT}.

$$R_{SHUNT(max)} = \frac{V_{SHUNT(max)}}{I_{LOAD(max)}} \tag{6}$$

Given that the maximum shunt voltage is ±25 mV and the load current range is ±2.5 A, the maximum shunt resistance is calculated as shown in Equation 7.

$$R_{SHUNT\,(max)} = \frac{V_{SHUNT\,(max)}}{I_{LOAD\,(max)}} = \frac{25mV}{2.5A} = 10m\Omega \tag{7}$$

To minimize errors over temperature, select a low-drift shunt resistor. To minimize offset error, select a shunt resistor with the lowest tolerance. For this design, the Y14870R01000B9W resistor is used.

10.2.1.2.2 Differential Amplifier

The differential amplifier used for this design should have the following features:

1. Single-supply (3 V),
2. Reference voltage input,
3. Low initial input offset voltage (V_{OS}),
4. Low-drift,
5. Fixed gain, and
6. Low-side sensing (input common-mode range below ground).

For this design, a current-shunt monitor (INA213) is used. The INA21x family topology is shown in Figure 51. The INA213B specifications can be found in the INA213 product data sheet.

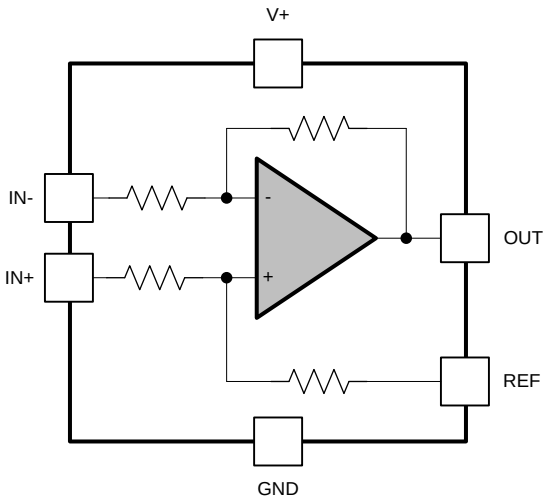


Figure 51. INA21x Current-Shunt Monitor Topology

Typical Application (continued)

The INA213B is an excellent choice for this application because all the required features are included. In general, instrumentation amplifiers (INAs) do not have the input common-mode swing to ground that is essential for this application. In addition, INAs require external resistors to set their gain, which is not desirable for low-drift applications. Difference amplifiers typically have larger input bias currents, which reduce solution accuracy at small load currents. Difference amplifiers typically have a gain of 1 V/V. When the gain is adjustable, these amplifiers use external resistors that are not conducive to low-drift applications.

10.2.1.2.3 Voltage Reference

The voltage reference for this application should have the following features:

1. Dual output (3.0 V and 1.5 V),
2. Low drift, and
3. Low tracking errors between the two outputs.

For this design, the REF2030 is used. The REF20xx topology is as shown in the *Functional Block Diagram* section.

The REF2030 is an excellent choice for this application because of its dual output. The temperature drift of 8 ppm/°C and initial accuracy of 0.05% make the errors resulting from the voltage reference minimal in this application. In addition, there is minimal mismatch between the two outputs and both outputs track very well across temperature, as shown in Figure 52 and Figure 53.

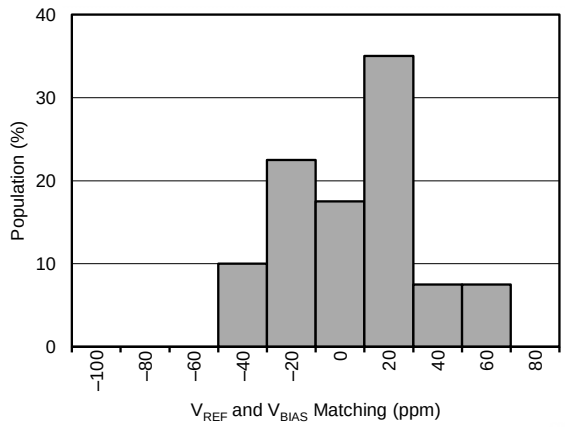


Figure 52. V_{REF} – 2 × V_{BIAS} Distribution (At T_A = 25°C)

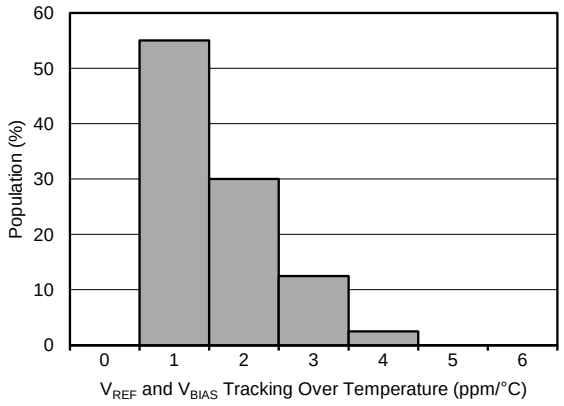


Figure 53. Distribution of V_{REF} – 2 × V_{BIAS} Drift Tracking Over Temperature

10.2.1.2.4 Results

Table 1 summarizes the measured results.

Table 1. Measured Results

ERROR	UNCALIBRATED (%)	CALIBRATED (%)
Error across the full load current range (25°C)	±0.0355	±0.004
Error across the full load current range (–40°C to 125°C)	±0.0522	±0.0606

10.2.1.3 Application Curves

Performing a two-point calibration at 25°C removes the errors associated with offset voltage, gain error, and so forth. Figure 54 to Figure 56 show the measured error at different conditions. For a more detailed description on measurement procedure, calibration, and calculations, please refer to TIDU357.

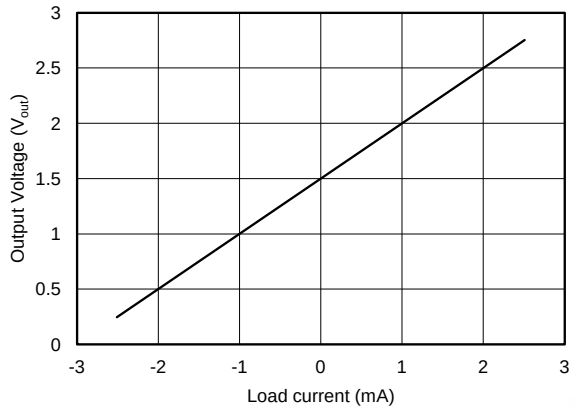


Figure 54. Measured Transfer Function

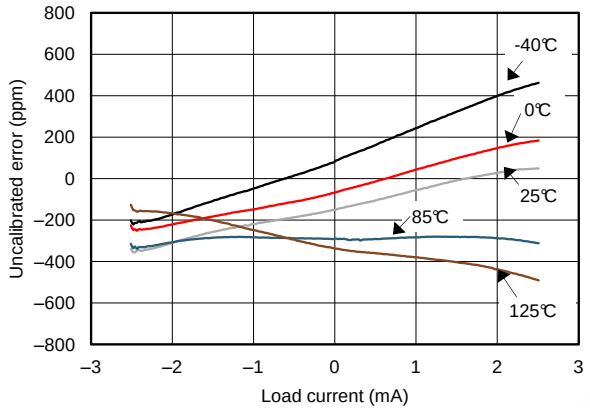


Figure 55. Uncalibrated Error vs Load Current

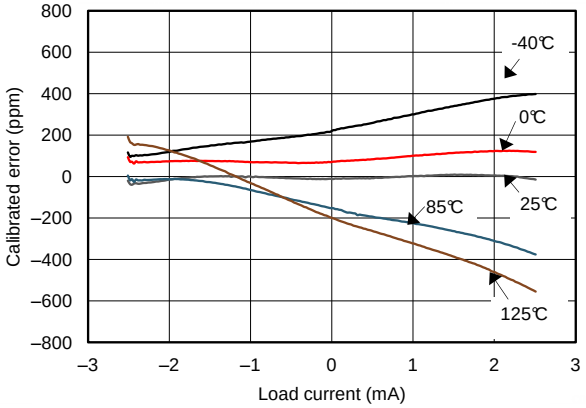


Figure 56. Calibrated Error vs Load Current

11 Power-Supply Recommendations

The REF20xx family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 20 mV above the output voltage. For loaded reference conditions, a typical dropout voltage versus load is shown in Figure 57. A supply bypass capacitor ranging between 0.1 µF to 10 µF is recommended.

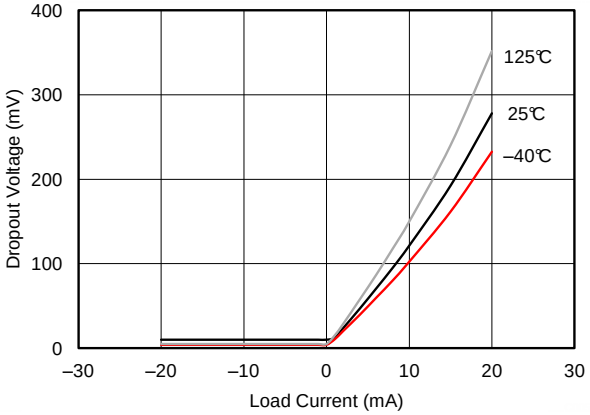


Figure 57. Dropout Voltage vs Load Current

12 Layout

12.1 Layout Guidelines

Figure 58 shows an example of a PCB layout for a data acquisition system using the REF2030. Some key considerations are:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors at V_{IN}, V_{REF}, and V_{BIAS} of the REF2030.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Minimize trace length between the reference and bias connections to the INA and ADC to reduce noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

12.2 Layout Example

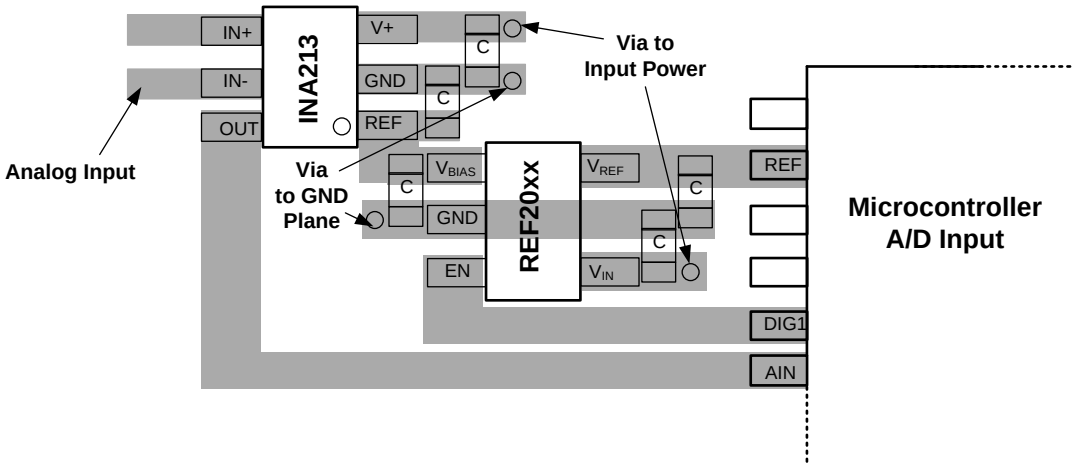


Figure 58. Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors* (SBOS437)
- *Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Reference Design* (TIDU357)

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
REF2025	Click here	Click here	Click here	Click here	Click here
REF2030	Click here	Click here	Click here	Click here	Click here
REF2033	Click here	Click here	Click here	Click here	Click here
REF2041	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.
e-Trim is a trademark of Texas Instruments, Inc.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF2025AIDDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GACM	Samples
REF2025AIDDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GACM	Samples
REF2025AISDDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 125	1M98	Samples
REF2030AIDDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GADM	Samples
REF2030AIDDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GADM	Samples
REF2033AIDDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAEM	Samples
REF2033AIDDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAEM	Samples
REF2041AIDDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAFM	Samples
REF2041AIDDCT	ACTIVE	SOT-23-THIN	DDC	5	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAFM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

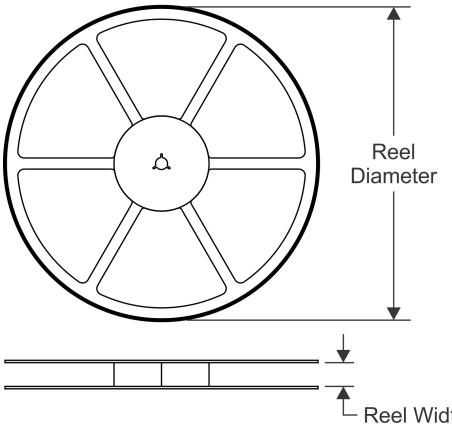
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

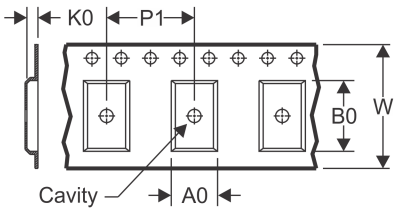
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

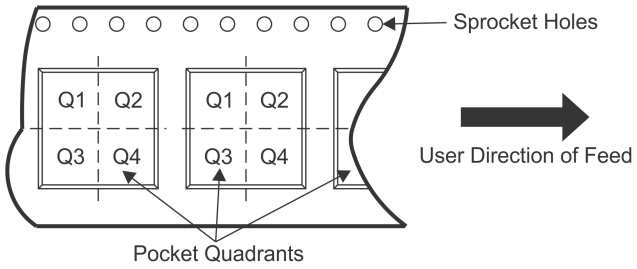


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

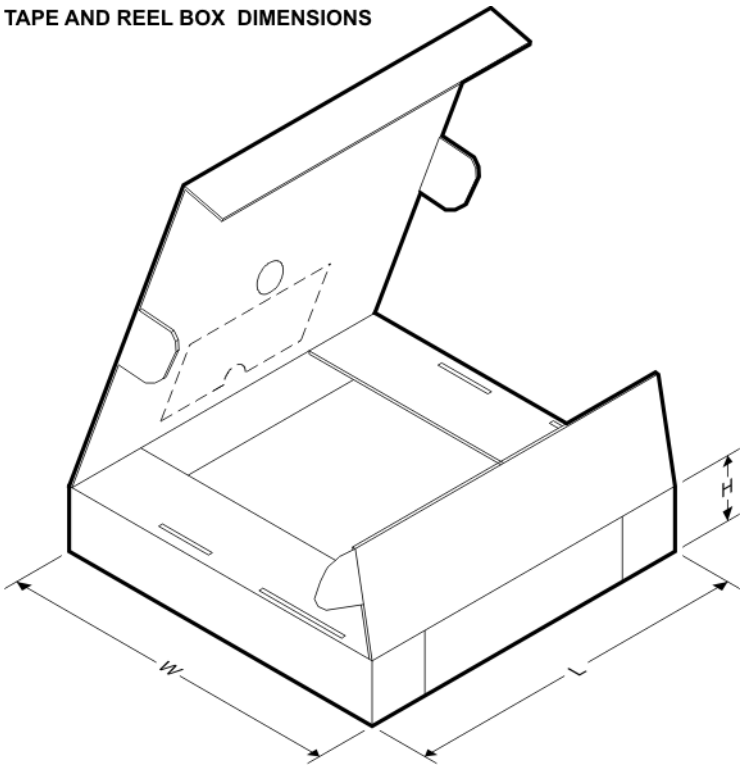
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF2025AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2025AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2025AISDDCR	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2030AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2030AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2033AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2033AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2041AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2041AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

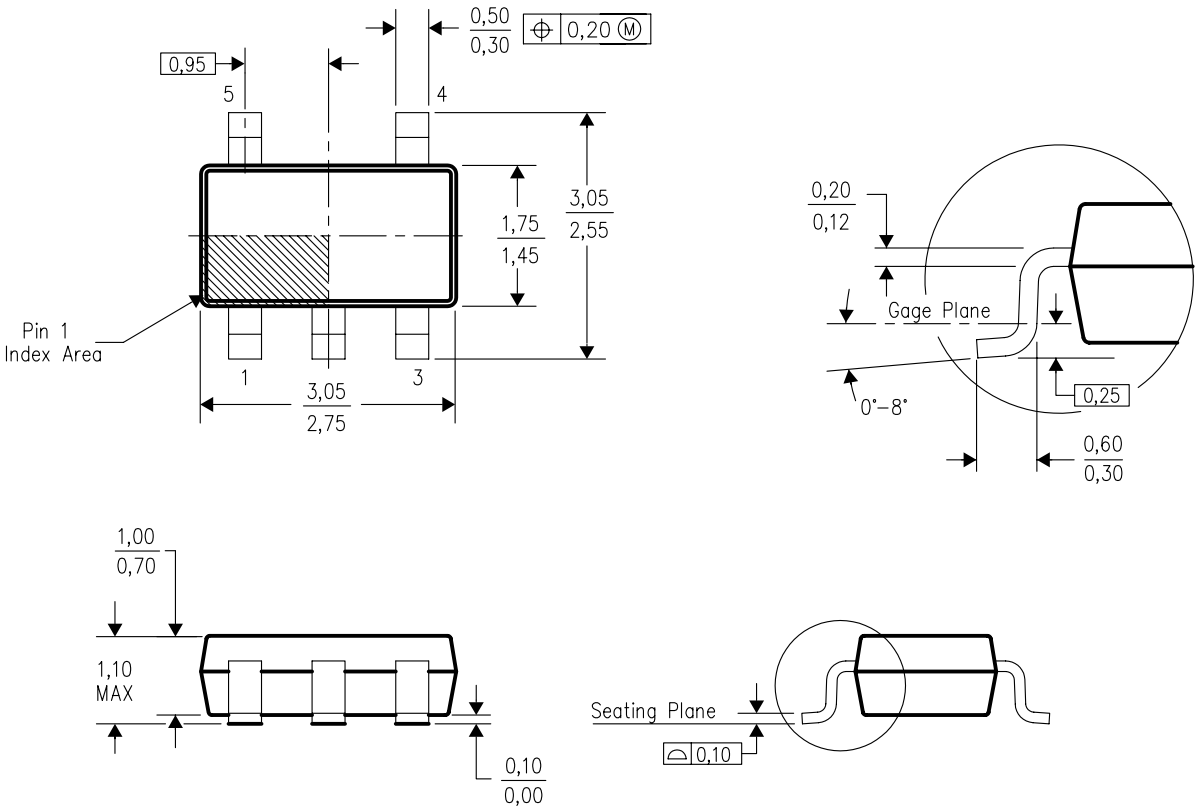
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF2025AIDDCR	SOT-23-THIN	DDC	5	3000	195.0	200.0	45.0
REF2025AIDDCT	SOT-23-THIN	DDC	5	250	195.0	200.0	45.0
REF2025AISDDCR	SOT-23-THIN	DDC	5	3000	195.0	200.0	45.0
REF2030AIDDCR	SOT-23-THIN	DDC	5	3000	195.0	200.0	45.0
REF2030AIDDCT	SOT-23-THIN	DDC	5	250	195.0	200.0	45.0
REF2033AIDDCR	SOT-23-THIN	DDC	5	3000	195.0	200.0	45.0
REF2033AIDDCT	SOT-23-THIN	DDC	5	250	195.0	200.0	45.0
REF2041AIDDCR	SOT-23-THIN	DDC	5	3000	195.0	200.0	45.0
REF2041AIDDCT	SOT-23-THIN	DDC	5	250	195.0	200.0	45.0

DDC (R–PDSO–G5) PLASTIC SMALL–OUTLINE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–193 variation AB (5 pin).

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