RAiO

RA8872

Character/Graphic

TFT LCD Controller

Specification

Version 1.1

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1. Description

RA8872 is a TFT LCD controller which supports the character and graphic mixed display. It is designed to meet the requirement of middle size TFT module up to 320x240 pixels with characters or 2D graphic application. With internal RAM, RA8872 can supports 65K color for 320x240 dots TFT Panel, 4K color for 640x240 display , or 4K color for 320x240 dots with 2-Layers.

The embedded CGROM is capable to display the alphaset of international standard ISO 8859-1/2/3/4. It includes 256x4 characters and can satisfiies almost English or Eurpean language family countries. For graphic usage, RA8872 supports a 2D Block Transfer Engine(BTE) that is compatible with 2D BitBLT function for processing the mass data transfer function. The geometric speed-up engine provides user an easy way to draw the programmable geometric shape by hardware, like line, square and circle. Besides, many powerful functions are combined with RA8872, such as screen rotation function, scroll function, graphic pattern, 2-layer mixed display and font enlargement function. These functions will save user a large of software effort during developement period.

RA8872 is a powerful and cheap choice for color application. To reduce the system cost, RA8872 proivde low cost 8080/6800 MCU I/F, a flexible 4-wires Touch Panel controller, PWM for adjusting panel back-light and some GPIOs. With the RA8872 design-in, user can achieve an easy-to-use, low-cost and high performace system compared with the other solution.

2. Feature

- Support Text/Graphic Mixed Display Mode.
- Support 8/12/16-Bits Generic RGB TFT Panel:
  2 Layers : Up to 320x240 Pixels, 4K Color
  1 Layer : Up to 320x240 Pixels, 65K Color.
- Color Depth TFT: 256/4K/65K Colors.
- Supporting MCU Interface: 8080/6800 with 8 Data Bus Width.
- Internal DDRAM Size: 230KB
- Embedded 10KB Character ROM with Font Size 8x16 Dots and Supporting Character Set of ISO8859-1/2/3/4.
- Embedded Block Transfer Engine (BTE) with 2D Function.
- Embedded Geometric Speed-up Engine.
- Font Enlargement X1, X2, X3, X4 for Horizontal or Vertical Direction.
- Screen Display Rotation 90°, 180° and 270° for Different Panel Type.
- Support Font Vertical Rotation.
- Support Block Scroll for Vertical or Horizontal Direction.
- Text Cursor for Character Writing.
- 32X32 Pixel Graphic Cursor Function.
- Support 256 User-defined 8x16 Characters.
- Support 32 User-defined Patterns of 8x8 Pixels.
- 2 programmable PWM for Back-Light Adjusting or Other's Application.
- Embedded 4-Wires Touch Panel Controller.
- 6 Sets of Programmable GPIO (GPIO0~5).
- Clock Source: External X'tal Clock Input with Internal PLL.
- Sleep Mode with Low Power Consumption.
- Operation Voltage: 3.0V~3.6V
- Package: LQFP-100pin.

3. Block Diagram

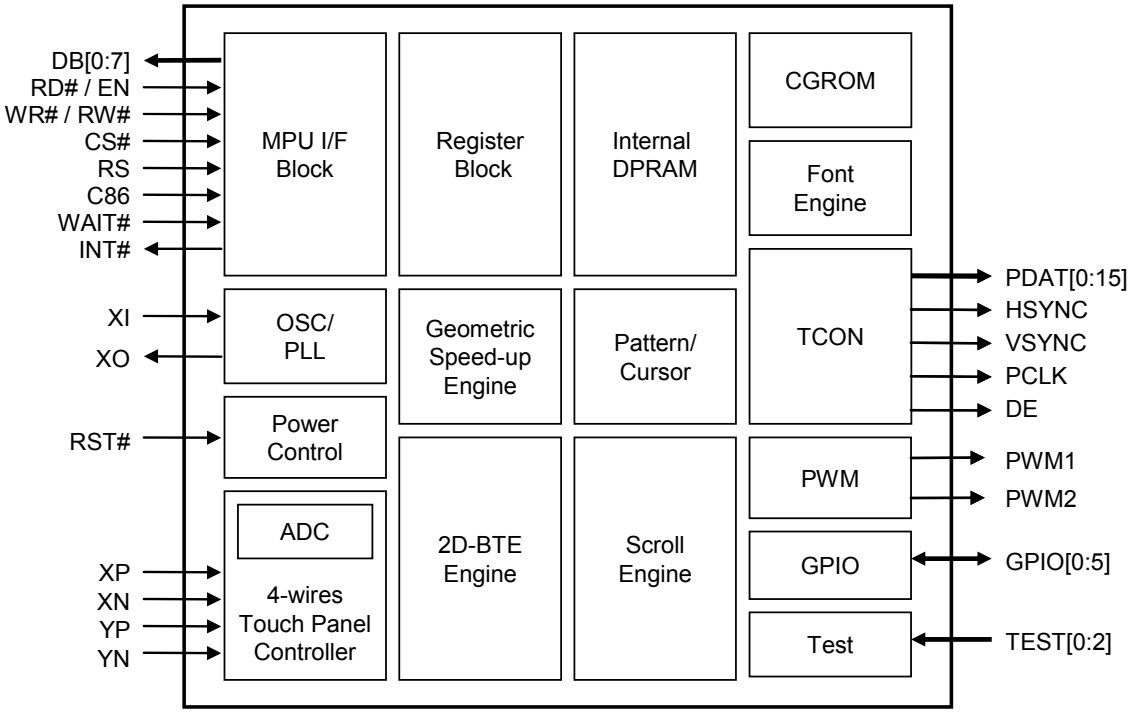

Figure 3-1 : Internal Block Diagram

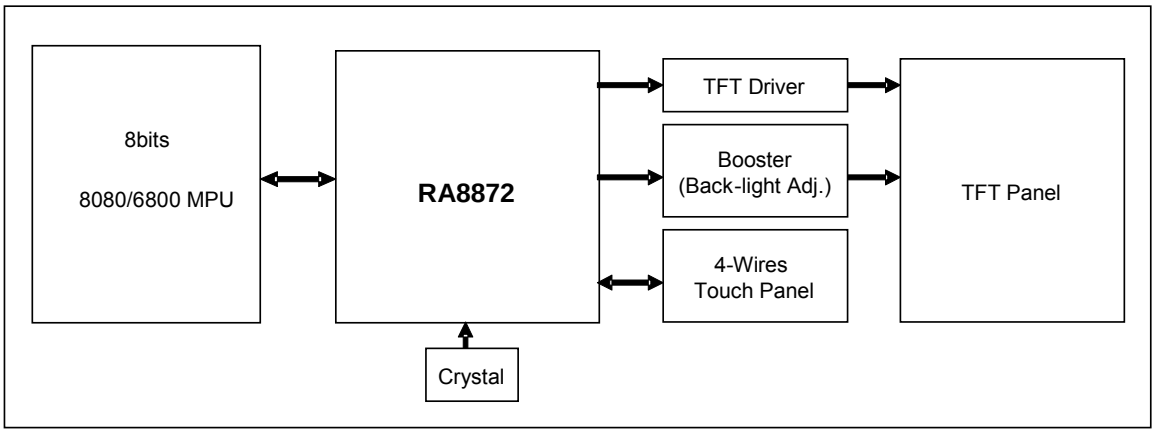

Figure 3-2 : System Block Diagram

4. Pin Definition

4-1 MCU Interface

Pin Name	I/O	Pin#	Pin Description
DB[0:7]	IO	14, 15, 19~ 24	**Data Bus** These are data bus for data transfer between MCU and RA8872.
RD# / EN	I	9	**Enable/Read Enable** When MCU interface (I/F) is 8080 series, this pin is used as data read (RD#), active low. When MCU I/F is 6800 series, this pin is used as Enable (EN), active high.
WR# / RW#	I	10	**Write/Read-Write** When MCU I/F is 8080 series, this pin is used as data write (WR#), active low. When MCU I/F is 6800 series, this pin is used as data read/write control (RW#). Active high for read and active low for write.
CS#	I	11	**Chip Select Input** Low active chip select pin.
RS	I	12	**Command / Data Select Input** The pin is used to select command/data cycle. RS = 0, data Read/Write cycle is selected. RS = 1, status read/command write cycle is selected. In 8080 interface, usually it connects to “A0” address pin. RS / WR# / Access Cycle: 0 / 0 / Data Write 0 / 1 / Data Read 1 / 0 / CMD Write 1 / 1 / Status Read
C86	I	13	**MCU Interface Select** 0 : 8080 interface is selected. 1 : 6800 interface is selected.
INT#	O	37	**Interrupt Signal Output** The interrupt output for MCU to indicate the status of RA8872.
WAIT#	O	36	**Wait Signal Output** This is a WAIT output to indicate the RA8872 is in busy state. The RA8872 can’t access MCU cycle when WAIT# pin is active. It is active low and could be used for MCU to poll busy status by connecting it to I/O port.

4-2 LCD Panel Interface

Pin Name	I/O	Pin#	Pin Description
PDAT[0:15]	O	85~100	**LCD Panel Data Bus** Data bus output for TFT LCD panel driver IC. This data bus must be connected to the corresponding bus of TFT-LCD panel.
HSYNC	O	81	**HSYNC Pulse** When generic TFT is selected, the signal is used as HSYNC.
VSYNC	O	82	**VSYNC Pulse** When generic TFT is selected, the signal is used as VSYNC.
PCLK	O	83	**Pixel Clock** When generic TFT is selected, the signal is used as PCLK.
DE	O	84	**Data Enable** When generic TFT is selected, the signal is used as DE.

4-3 Touch Panel and PWM Interface

Pin Name	I/O	Pin#	Pin Description
XP	A	8	**XP Signal for Touch Panel** This pin connects to XP switch signal of 4-wires touch panel.
XN	A	5	**XN Signal for Touch Panel** This pin connects to XN switch signal of 4-wires touch panel.
YP	A	6	**YP Signal for Touch Panel** Touch Panel control signal. This pin connects to YP switch signal of 4-wires touch panel. It must be connected a 100KΩ pull-up resistor when the Touch Panel function is enable.
YN	A	7	**YN Signal for Touch Panel** Touch Panel control signal. This pin connects to YN switch signal of 4-wires touch panel.
PWM1 **PWM2**	O	33, 34	**PWM Output** PWM output pins. The duty could be programmed by register setting.
GPIO[0:5]	IO	64~66, 69~71	**General Purpose I/O** These signals are used as GPIO signals; user can program it by register.

4-4 Clock and Power Interface

Pin Name	I/O	Pin#	Pin Description
XI	I	28	**Crystal Input Pin** Input pin for internal crystal circuit. It should be connected to external crystal to generate the source of PLL circuit. That will generate the system clock for RA8872.
XO	O	29	**Crystal Output Pin** Output pin for internal crystal circuit.
RST#	I	38	**Reset Signal Input** This active-low input performs a hardware reset on the RA8872. It is a Schmitt-trigger input for enhanced noise immunity; however, care should be taken to ensure that it is not triggered if the supply voltage is lowered.
TEST[0:2]	I	40~42	**Test Mode Input** For chip test function, should be connected to GND for normal operation.
VR1	A	76	**Reference Voltage Input** This is a reference voltage input. For normal operation, it only need add a 0.1uF capacitor to ground.
VR2	A	74	**Reference Voltage Output** This is a reference voltage output. For normal operation, it only need add a 0.2uF capacitor to ground.
ADC_VREF	A	4	**ADC Reference Voltage** This pin is the reference voltage input of ADC. The reference voltage could be generated by RA8872 or from external circuit.
LDO_VDD	P	27, 79,	**LDO VDD** 3.3V power source for LDO. The internal LDO will generate the 1.8V power output.
LDO_GND	P	25, 78	**LDO GND** Ground signal for internal LDO.
LDO_OUT	P	80	**LDO Output** 1.8V power generated by internal LDO. It must connect bypass capacities to prevent power noise.
LDO_CAP	P	30	**LDO Capacitor Input** It must connect 1uF bypass capacities to prevent power noise.
CORE_VDD	P	17, 57	**CORE VDD** Core VDD is 1.8V. The core power input that connects to LDO_OUT. It must connect 1uF bypass capacities to prevent power noise.
ADC_VDD	P	2	**ADC VDD** ADC 3.3V power signals. Please connect this signal to 3.3V.

Pin Name	I/O	Pin#	Pin Description
ADC_GND	P	3	**ADC GND** ADC ground signal. Please connect this signal to ground.
VDD	P	18, 32, 61, 77	**IO VDD** 3.3V IO power input.
GND	P	1, 16, 31, 35, 50, 51, 59	**GND** IO Cell/Core ground signals.

5. Package

