

PLASTIC SILICON RECTIFIER

VOLTAGE RANGE: 50 --- 1000V
CURRENT: 1.0 A

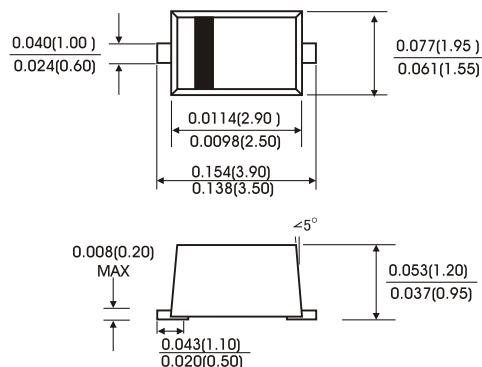
FEATURES

- Glass passivated junction
- For Surface Mount Applications, Easy to pick and place
- Plastic package has Underwriters Laboratory Flammability Classification 94V-0
- High temperature soldering guaranteed: 260°C/10 seconds at terminals,
- Component in accordance to RoHS 2002/95/EC and WEEE 2002/96/EC

MECHANICAL DATA

- Case: SOD-123FL molded plastic
- Terminals: Solder plated, solderable per MIL-STD-750, Method 2026
- Polarity: Color band denotes cathode end
- Mounting Position: Any
- Weight: 0.01 gram

SOD-123FL



MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Ratings at 25°C ambient temperature unless otherwise specified.

Single phase, half wave, 60 Hz, resistive or inductive load. For capacitive load, derate by 20%.

		Symbols	R1A	R1B	R1D	R1G	R1J	R1K	R1M	Units
Maximum Recurrent Peak Reverse Voltage		VRRM	50	100	200	400	600	800	1000	Volts
Maximum RMS Voltage		VRMS	35	70	140	280	420	560	700	Volts
Maximum DC Blocking Voltage		VDC	50	100	200	400	600	800	1000	Volts
Maximum Average Forward Rectified Current at TL=100°C		l(AV)	1.0							Amps
Peak Forward Surge Current 8.3ms single half sine-wave superimposed on rated load (JEDEC method)		lFSM	25.0							Amps
Maximum Instantaneous Forward Voltage at 1.0 A		VF	1.3							Volts
Maximum DC Reverse Current at rated DC blocking voltage	TA=25°C	IR	5.0							μA
	TA=125°C		50							
Maximum reverse recovery time(Note1)		t _{rr}	150				250	500		ns
Typical junction capacitance(Note2)		CJ	15.0							pF
Operating junction and storage temperature range		TJ TSTG	-55 to +150							°C

NOTE: 1. Measured at 1.0MHz and applied reverse voltage of 4.0V DC.

2. Thermal resistance from junction to ambient.

FIG.1-TYPICAL FORWARD CURRENT DERATING CURVE

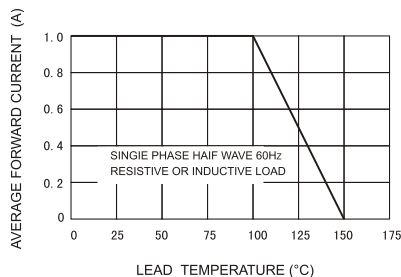


FIG.2-MAXIMUM NON-REPETITIVE FORWARD SURGE CURRENT

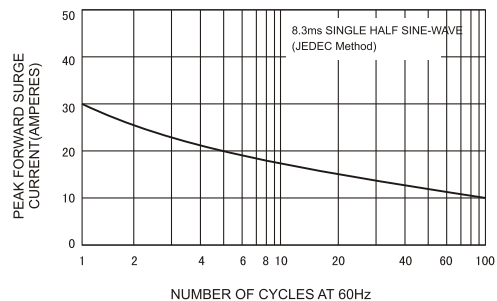


FIG.3-TYPICAL INSTANTANEOUS FORWARD CHARACTERISTICS

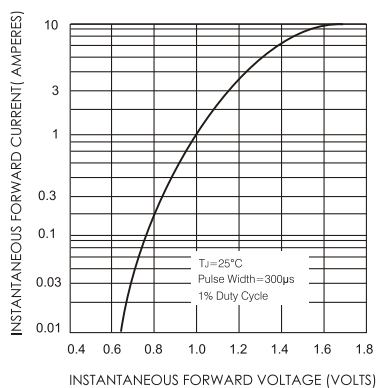


FIG.4-TYPICAL REVERSE CHARACTERISTICS

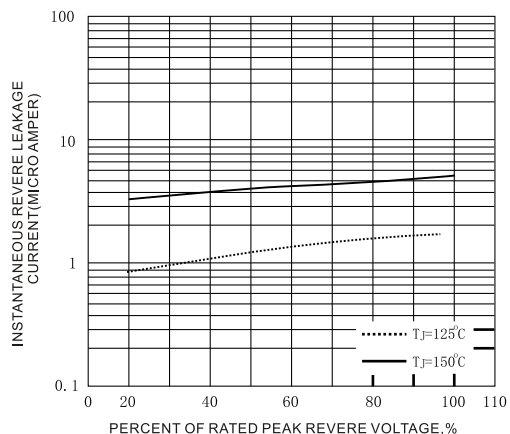


FIG.5-TYPICAL JUNCTION CAPACITANCE

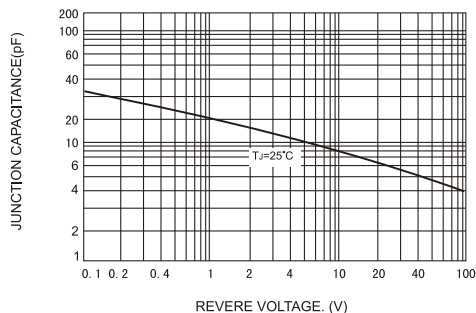


FIG.6-TEST CIRCUIT DIAGRAM AND REVERSE RECOVERY TIME CHARACTERISTIC

