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RoHS

QPI-10

QUIETPOWER®

AdvancedTCA™ Hot-Swap SiP with V•I Chip EMI Filter

Description

The QPI-10 integrates a total hot-swap function with an EMI filter for V•I Chip applications. The product aligns with the AdvancedTCA™ PICMG3.0, require-ments for hot insertion and board level conducted noise limitations. The EMI filter provides conducted common-mode (CM) and differential-mode (DM) noise attenuation from 150 kHz to 30 MHz. The QPI-10 is designed for use on a 48 or 60 Vdc bus (36 – 76 Vdc). The inrush current limit and circuit breaker are designed to satisfy the 200 W per board PICMG3.0, limit up to 70°C PCB temperature around the QPI-10.

The under and overvoltage thresholds can be trimmed separately via the UVEN and OV inputs using external series resistors. The QPI-10 provides two Power Good signals, with one referenced to the input ground and the other to the output ground, which can be used to enable other circuits along with the V•I Chip converter.

Features

- **>40 dB CM attenuation at 1 MHz**
- **>60 dB DM attenuation at 1 MHz**
- **80 Vdc (max input)**
- **100 Vdc surge 100 msec**
- **1500 V hipot hold off to shield**
- **6 A breaker with delay plus 12 A limiter**
- **25 mm x 25 mm x 4.5 mm SiP (System-in-Package)**
- **Low profile LGA package**
- **-40° to +100°C PCB temperature (See Fig. 5)**
- **Hot-swap & filter combined saves PCB space**
- **Efficiency ~99%**
- **Connects between OR'ing diodes & power conversion input hold-up capacitance**
- **Patents pending**
- **TÜV approval**

Applications

- **Telecom & ATCA PICMG® 3.0 boards using Vicor's V•I Chip technology**

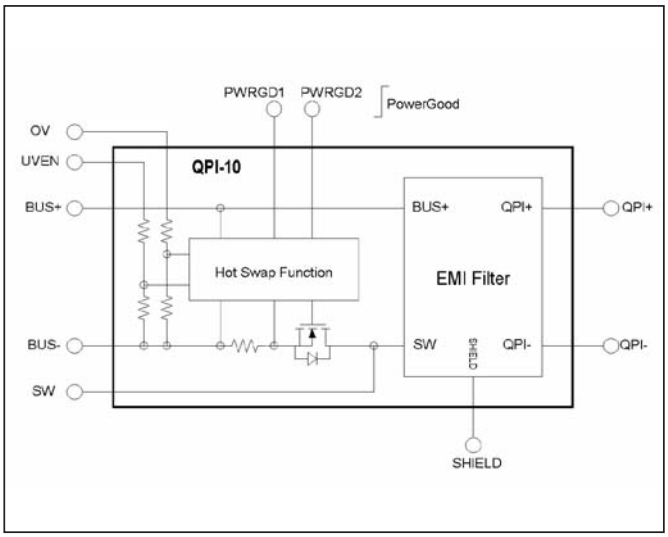


Figure 1 *– Block Diagram*

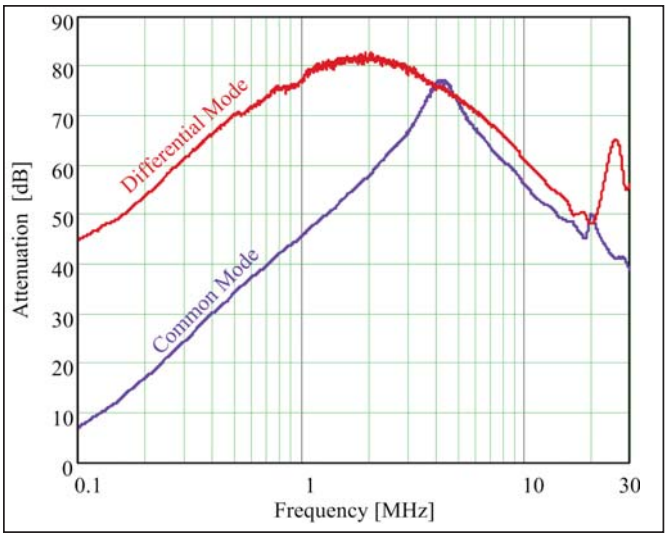


Figure 2 *– Typical Attenuation*

Absolute Maximum Ratings – *Exceeding these parameters may result in permanent damage to the product.*

Pins	Parameter	Notes	Min	Typ	Max	Units
BUS+, SW, PWRGD1, PWRGD2 to BUS-	Input voltage	Continuous	-0.5		80	Vdc
BUS+, SW, PWRGD1, PWRGD2 to BUS-	Input voltage	100 ms transient			100	Vdc
BUS+ / BUS- to Shield	BUS inputs to shield hipot				+/-1500	Vdc
QPI+ to QPI-	Input to output current	Pulsed limit @ 25°C		12		Adc
Package	Power dissipation	VBUS = 48 V, 6 Adc, 25°C			3.0	W
Package	Operating temperature	PCB to QPI interface	-40		100	°C
Package	Thermal resistance	Free air			50	°C/W
Package	Junction temperature	Tb = 100 °C Pd = 3W @15°C/W			145	°C
Package	Thermal resistance	PCB layout dependent(1)			15	°C/W
Package	Storage temperature		-40		125	°C
Package	Reflow temperature	20 s exposure @(2)			212	°C
All Pins	ESD	HBM			+/-2	kV

Note 1: *Refer to Figure 14 and Figure 15 for critical PCB layout guidelines to achieve this thermal resistance when reflowed onto the PCB.*
Note 2: *RoHS compliant product maximum peak temperature is 245°C for 20 seconds.*

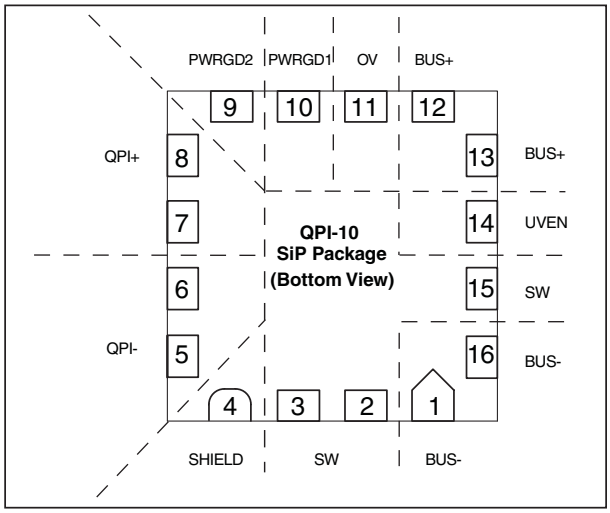
Electrical Characteristics – *Parameter limits apply over the operating PCB temperature range unless otherwise noted*

Symbol	Parameter	Notes	Min	Typ	Max	Units
Vb+b-	BUS+ to BUS- input range	Measured at 5 A(3)	UV	80		Vdc
V+oi	BUS+ to QPI+ voltage drop	Measured at 5 A(3)		110		mVdc
V-oi	BUS- to QPI- voltage drop	Measured at 5 A(3)		-380		mVdc
CMIL	Common-mode insertion loss	VBUS = 48 V frequency =1 MHz	40			dB
DMIL	Differential-mode insertion loss	VBUS = 48 V frequency =1 MHz	60			dB
I BUS+ to BUS-	Input bias current at 80 V	Input current from BUS+ to BUS-		10		mA
IPG QPI+ to QPI-	Load current prior to PWRGD	Critical maximum DC load		25		mA
UV	Undervoltage threshold - rising	Controller disabled to enabled		34		V
UVHYS	Undervoltage hysteresis - falling	Controller enabled to disabled		UV - 2 V		V
OV	Overvoltage threshold - rising	Controller enabled to disabled		76		V
OVHYS	Overvoltage hysteresis - falling	Controller disabled to enabled		OV - 4 V		V
PWRGD1SAT	Power Good low voltage	IPWG = 1 mA, referenced to BUS-	0.2		0.6	mV
PWRGD2SAT	Power Good low voltage	IPWG = 1 mA, referenced to QPI-	0.2		0.6	mV
PWGLK	Power Good high leakage	VPWG = 80 V			1	µA

Note 3: *Refer to Figure 5 for current derating curve*

Pad Description

Pin Number	Name	Description
1, 16	BUS-	Negative bus potential
2, 3, 15	SW	Negative rail controlled by hot insertion function.
4	SHIELD	Shield connects to the converter shield and Y capacitor common point via RY
5, 6	QPI-	Negative input to the converter
7, 8	QPI+	Positive input to the converter
10	PWRGD1	Open drain, referenced to BUS-, that asserts low when power is NOT good
9	PWRGD2	Open drain, referenced to QPI-, that asserts low when power is NOT good
12, 13	BUS+	Positive bus potential
14	UVEN	Highside of UV resistor divider
11	OV	Highside of OV resistor divider



Applications Information

The QPI-10 is an EMI filter especially designed for V•I Chip products, providing conducted common-mode and differential-mode attenuation from 150 kHz to 30 MHz. Designed for the telecom and ITE bus range, the QPI supports the PICMG® 3.0 specification for filtering system boards using Vicor's V•I Chip technology to the EN55022 Class B limit.

The resulting plot in Figure 4 shows the QPI-10 is effective in reducing the V•I Chip total noise spectrum to well below the EN55022 Class B Quasi-peak detection limit.

The plot in Figure 4 was taken using the standard 50/50 µH LISN and measurement conditions, with the Peak detection mode of the spectrum analyzer, for a conducted EMI test. The results are compared to the CISPR22 EN55022 Class B Quasi-peak detection limit showing the total noise spectrum for V•I Chip combination using a P048K048T24 and V048K120T025 with a QPI-10 connected, as shown in Figure 3.

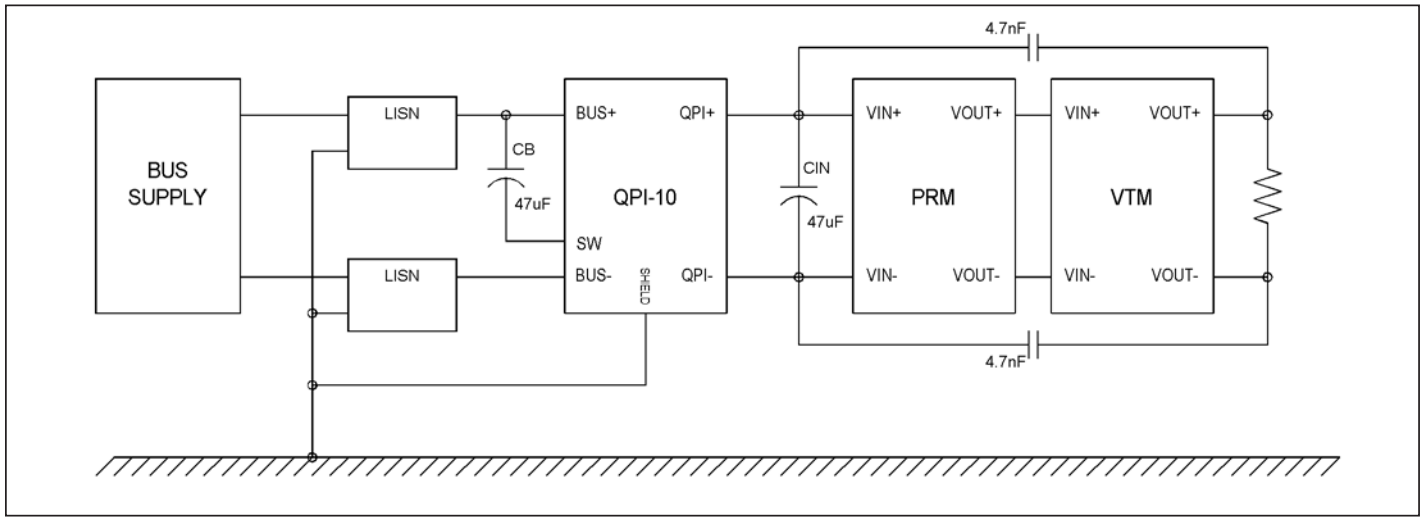


Figure 3 *– Standard LISN test setup, 170 W load.*

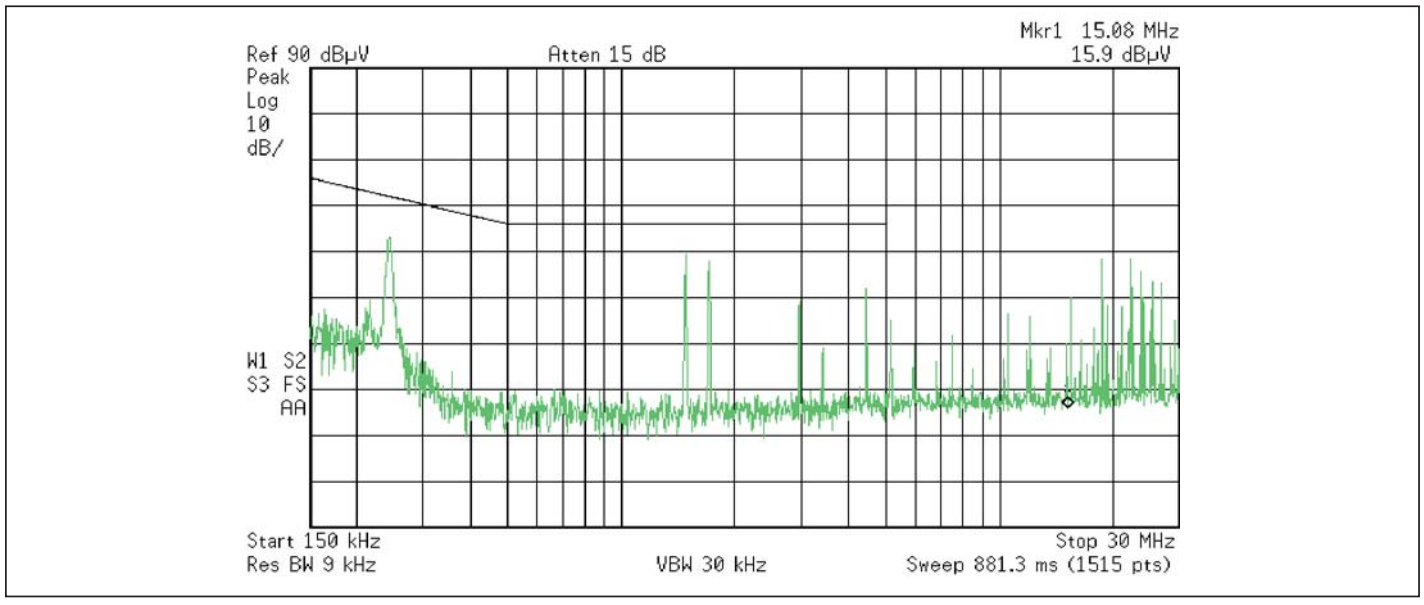


Figure 4 *– Conducted EMI profile of V•I Chip with QPI-10.*

Applications Information – Hot-Swap

The QPI-10's high-temperature rating of 6 A provides filtering for up to 288 W of power from a 48 V bus with a 70°C PCB temperature. It is well suited for the 200 W per board limit in the PICMG® 3.0. The 1.0" x 1.0" x 0.2" surface mount LGA package provides ease of manufacturing by eliminating through-hole assembly. The current derating curve, shown in Figure 5, should be used when the PCB temperature that the QPI-10 is mounted to exceeds 70°C.

The hot-swap feature is created with an internal switch that controls the current path between BUS- and SW pins. The state of the switch can be on, off or in a current-control mode depending on the state of the control function.

The QPI-10 has two signal pins that can be used to indicate the power-up status of the QPI-10. Both are active-low when power is not good. PWRGD1 is an opendrain that is referenced to the BUS- rail of the QPI-10. PWRGD2 is an opendrain that is referenced to the QPI– rail, allowing it to directly control the Enable pin of the V•I Chip converter, without any kind of signal translation required. An example circuit of both options can be seen in Figures 8a and 8b.

The QPI-10 is designed to have an under-voltage hysteretic range of 32 V to 34 V when the UVEN pin is tied to the BUS+ pin with no additional series resistance. The QPI-10 becomes enabled when the input voltage exceeds 34 V and continues to work down to 32 V before being disabled.

The over-voltage hysteretic range is designed to be 72 V to 76 V when the OV pin is tied to the BUS+ pin without a trimming resistor in series. The QPI-10 remains functioning until the OV surpasses 76 V, where it will shutdown until the input voltage falls below 72 V.

External resistors can be added to trim the UV and OV trip points higher. The graph in Figure 6 shows the trimming effect for a range of external series resistors.

The equations in Figure 7 can be used to calculate the required series resistor for increasing the preprogrammed trip points.

An external capacitor CE, shown in Figures 8a and 8b, will provide the required hold-up filtering during the AdvancedTCA's 5 ms, zero-volt BUS transient event. This filtering will enable the Power Good state of the QPI-10 to remain unchanged during this transient, provided there is enough hold-up capacitance and input energy to maintain the power converter's operation. Without this capacitor, the QPI-10 would detect an undervoltage fault and shut off its internal pass switch. The fault would also initiate a restart of the hot-swap control and would require up to 20 ms to turn back on its internal switch.

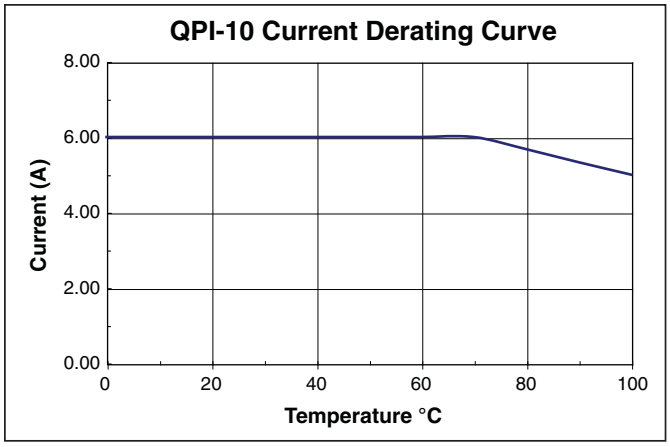


Figure 5 *– QPI-10 current derating curve over temperature.*

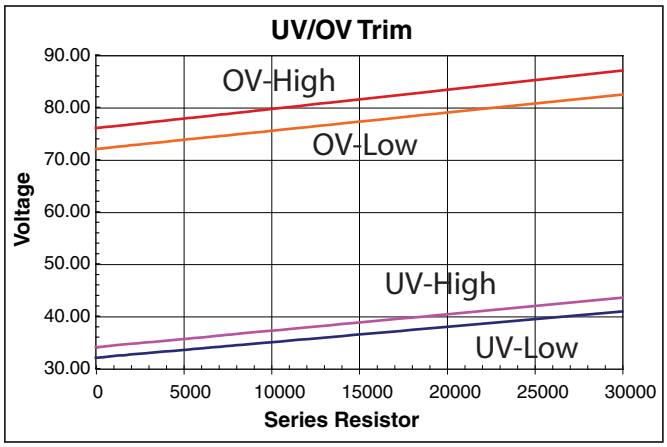


Figure 6 *– Trimming UV/OV with an external series resistor*

$$UVEN_{LO} = \frac{2.5\ V(RUVEN + 108450)}{8450}$$

$$UVEN_{HI} = 2.5\ V + (RUVEN + 100K)(316\mu A)$$

$$OV_{LO} = 2.5\ V + (ROV + 200K)(348\mu A)$$

$$OV_{HI} = \frac{2.5\ V(ROV + 206800)}{6800}$$

Figure 7 *– UVEN and OV resistor equations.*

Note: *If the CE Capacitor is used, a maximum value of 1 k should be used for RUVEN to prevent damaging the enabling diodes.*

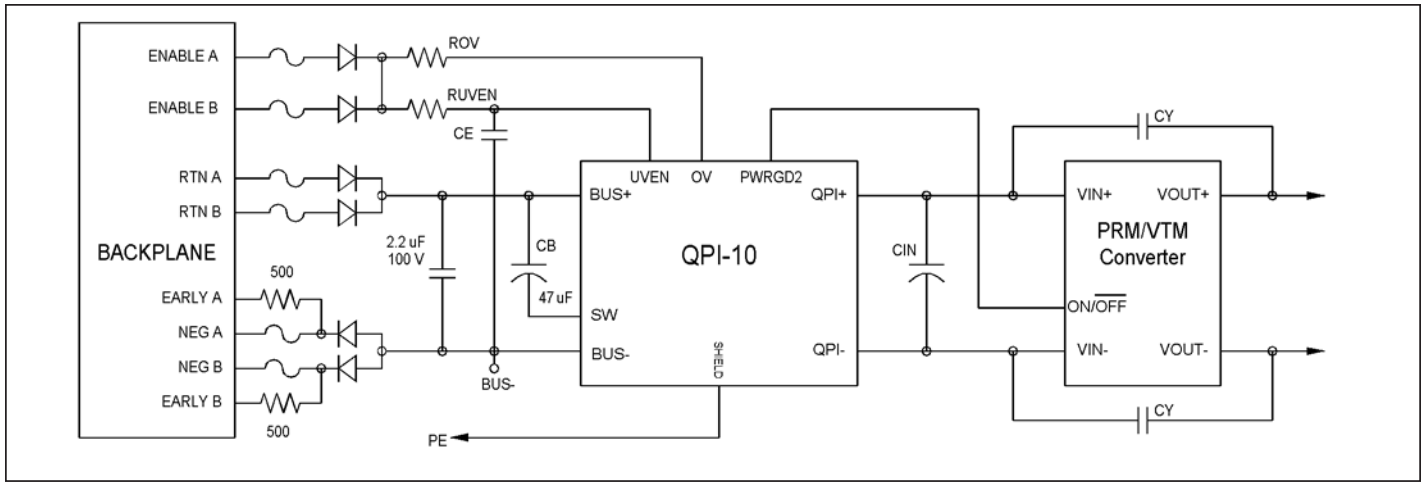


Figure 8a *– Typical ATCA system with QPI-10 and high enable converter.*

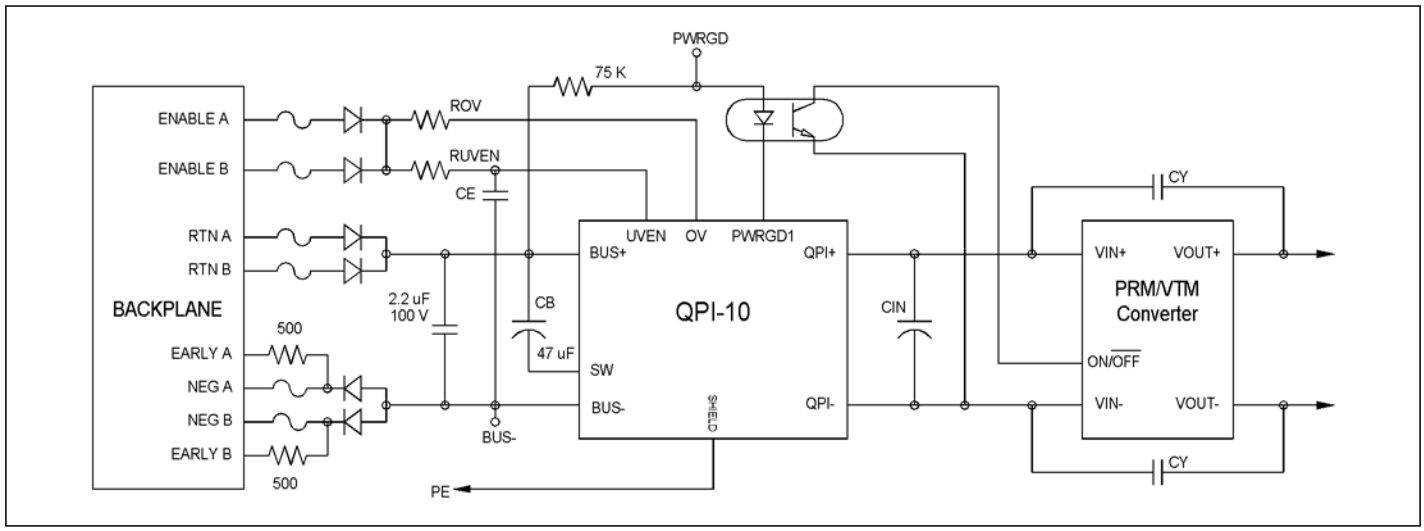


Figure 8b *– Typical ATCA system with QPI-10 and high enable converter.*

Start-up

The following oscilloscope pictures show the hot-swap BUS- current, QPI- to BUS- voltage and PWRGD to BUS- output voltage of the QPI-10 during operation. Figures 9 and 10 are the QPI-10's inrush characteristics under two load capacitance conditions. In Figure 9 a 470 µF capacitor required roughly 170 ms to completely charge from a 48 V bus voltage. The QPI-10 can drive large amounts of bulk capacitance to satisfy AdvancedTCA's transient hold-up requirement (PICMG 3.0, 4.1.4.3) as shown in Figure 10 with a 4,700 µF load capacitance. Under this condition the PWRGD takes about 8.7 seconds to go high after the UVEN input is pulled high upon the complete insertion of the board into the shelf. Figure 10's time-scale is too long to show the current pulses that charge the bulk capacitance.After insertion, when the UVEN voltage exceeds 34 V the UV detection fault is cleared, the QPI-10 goes through a delay cycle (~15 ms) to allow for system stabilization and debounce. After this time, the QPI– to BUS- path is turned on and current is allowed to pass, monitored by the current sense function. Initially the current level exceeds the 6 A circuit breaker limit, the event timer starts and the Power Good state is not valid. The sense function and linear control loop will

allow twice the circuit breaker current to pass. If the current does not drop below the circuit breaker level prior to reaching the timer limit, typically 275 µs, the QPI- to BUS- path will open. The effective duty cycle under the current limit condition is approximately 1%. Once the load capacitors are fully charged to the input bus potential, the load condition falls below 6 A and the PWRGD pin is asserted high, providing that the bus supply is still within the valid UV and OV range.

Transient Protection and Recovery

Figures 11 and 12 show the QPI-10's ability to handle low resistance shorts (< 2Ω) at the load terminals to emulate fast and slow blown fuse events. In Figure 11, the transient short is 2 seconds long and the QPI- to BUS- path is opened within 400 µs of this occurrence. Figure 12 demonstrates the QPI-10's performance with a continuous short circuit on its output, where it remains in a low duty cycle mode until the short is removed, then restarts normally.

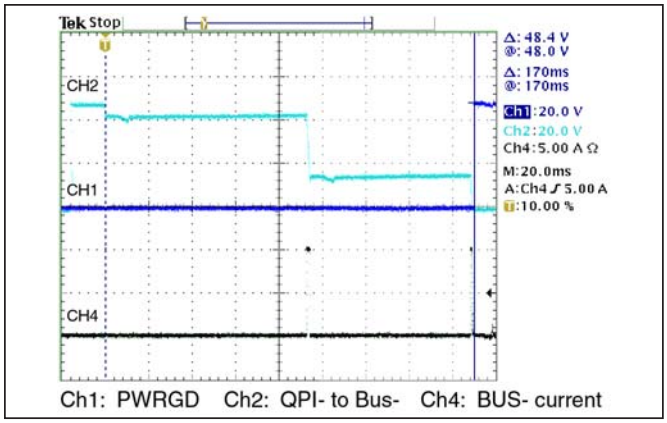


Figure 9 *– 470 µF capacitor @ 48 V.*

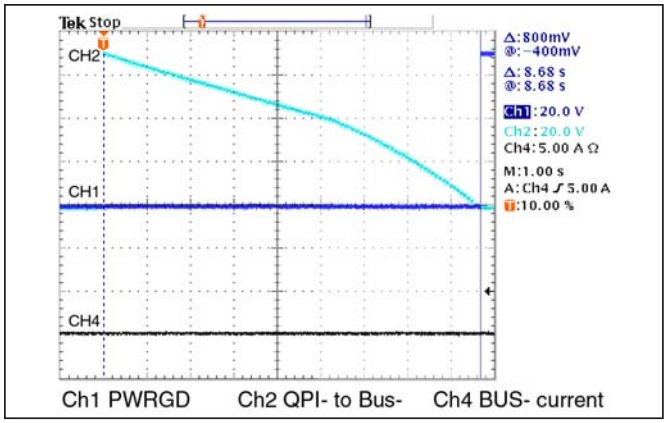


Figure 10 *– 4700 µF capacitor @ 72 V.*

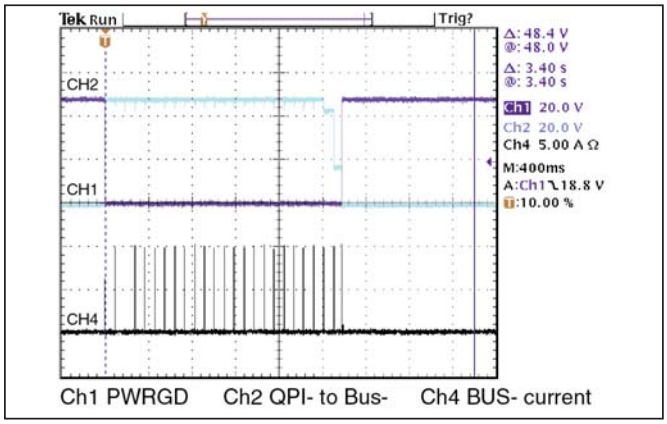


Figure 11 *– 2 seconds short-circuit.*

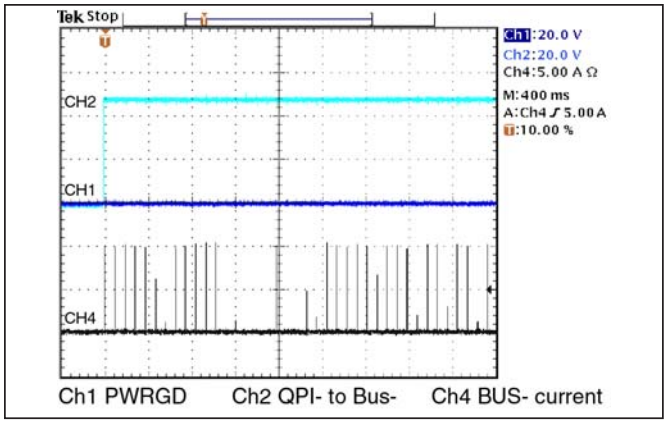


Figure 12 *– Start-up into short circuit.*

Mechanical & Layout Information

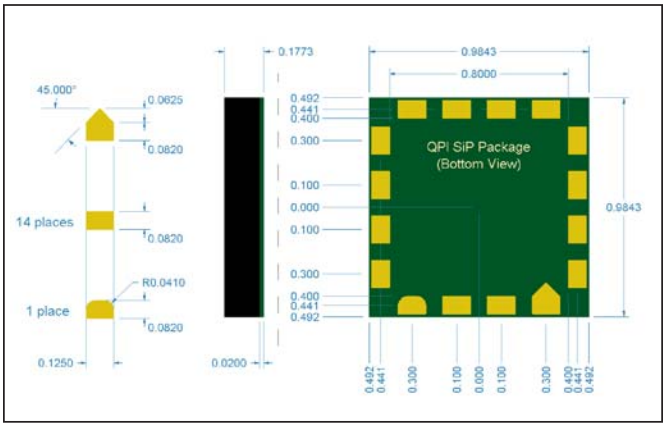


Figure 13 *– SiP package mechanicals; LGA pad, package height and pad location dimensions – inches.*

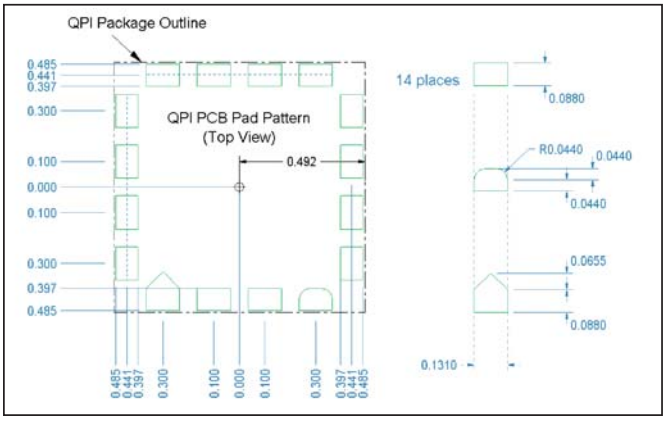


Figure 15 *– Recommended PCB receiving footprint.*

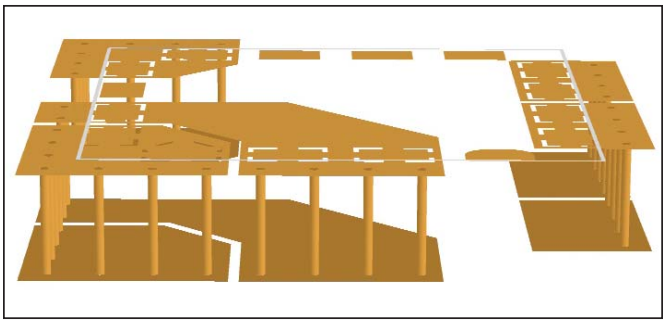


Figure 16 *– Recommended PCB layout on a 2 layer board*

Post Solder Cleaning

Picor lidded QP SIPs are not hermetically sealed and must not be exposed to liquid, including but not limited to cleaning solvents, aqueous washing solutions or pressurized sprays.

When soldering, it is recommended that no-clean flux solder be used, as this will insure that potentially corrosive mobile ions will not remain on, around, or under the module following the soldering process.

For applications requiring water wash compatibility the "–01" open frame version should be used.

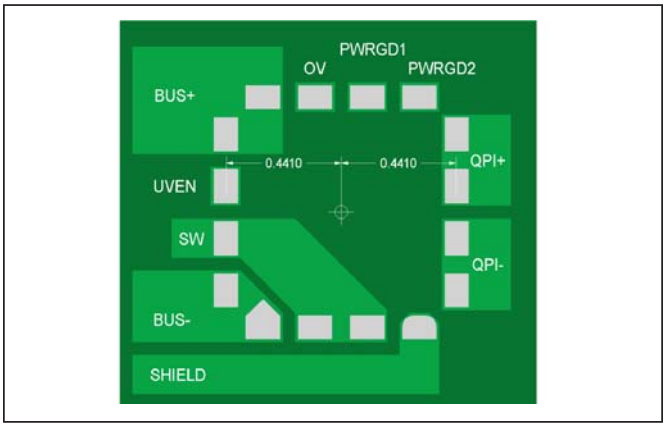


Figure 14 *– Recommended PCB Receiving Pattern.*

QPI-10 PCB Layout Recommendations

The filtering performance of the QPI-9 and –10 is sensitive to capacitive coupling between its input and output pins. Parasitic plane capacitance must be kept below 1 pico-Farad between inputs and outputs using the layout shown above and the recommendations described below to achieve maximum conducted EMI performance.

To avoid capacitive coupling between input and output pins, there should not be any planes or large traces that run under both input and output pins, such as a ground plane or power plane. For example, if there are two signal planes or large traces where one trace runs under the input pins, and the other under the output pins, and both planes over-lap in another area, they will cause capacitive coupling between input and output pins. Also, planes that run under both input and outputs pins, but do not cross, can cause capacitive coupling if they are capacitively by-passed together.

Figure 16 shows the recommended pcb layout on a 2 layer board. Here, the top layer planes are duplicated on the bottom layer so that there can be no over-lapping of input and output planes. This method can be used for boards of greater layer count.

Ordering Information

Part Number	Description
QPI-10LZ	QPI-10 LGA Package, RoHS Compliant
QPI-10LZ-01	QPI-10 LGA, RoHS Compliant Open Frame Package

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