MP8865

High-Efficiency, 6A, 21V, Synchronous Step-Down Converter with I²C Interface

DESCRIPTION

The MP8865 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with an I²C control interface. It offers a very compact solution to achieve a 6A continuous output current with excellent load and line regulation over a wide input supply range. The MP8865 has synchronous-mode operation for higher efficiency over the output load range.

The reference voltage level can be controlled on-the-fly through the 3.4Mbps I²C serial interface. The voltage range can be adjusted from 0.6V to 1.87V in 10mV steps. Also, the voltage slew rate, switching frequency, enable, and power-saving mode are selectable through the I²C interface.

Current-mode operation provides fast transient response and eases loop stabilization. Full protection features include over-current protection (OCP), over-voltage protection (OVP), and thermal shutdown (TSD).

The MP8865 requires a minimal number of readily available, standard, external components and is available in a QFN-15 3mm x 3mm package.

FEATURES

- Wide 4.5V to 21V Operation Input Range
- 45mΩ/18mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- 1% VOUT Accuracy
- I²C Programmable Reference Voltage Range from 0.6V to 1.87V in 10mV Steps with Slew Rate Control
- I²C Selectable Switching Frequency. Default 600kHz Switching Frequency.
- Programmable Output Voltage
- Power-Saving Mode, OTP, and OCP via I²C
- Power Good Indication
- 1-Bit I²C Address Set
- OCP Protection in Hiccup Mode
- External Soft Start
- Available in a QFN-15 3mm x 3mm Package

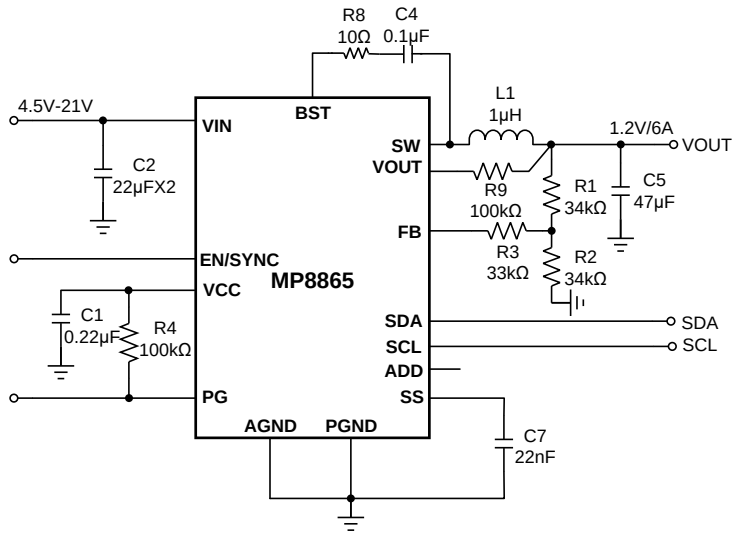
APPLICATIONS

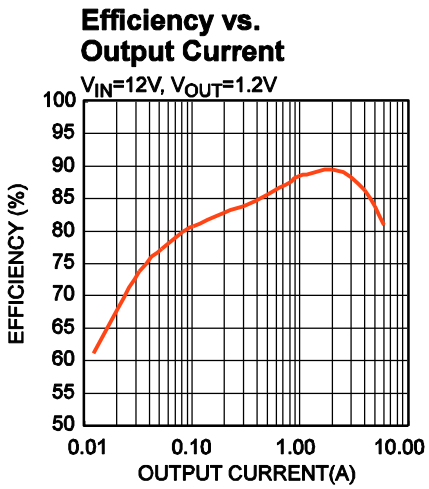
- SoC and Media Processors
- General Consumers
- Distributed Power Systems

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.

"MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

TYPICAL APPLICATION





MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number	Package	Top Marking
MP8865GQ*	QFN-15 (3mmx3mm)	*See Below*
EVKT-8865	Evaluation Kit	

*For Tape & Reel, add suffix –Z (e.g. MP8865GQ–Z);

TOP MARKING

AGLY
LLL

AGL: Product code of MP8865GQ
Y: Year code
LLL: Lot number

EVALUATION KIT EVKT-8865

EVKT-8865 Kit contents: (Items can be ordered separately).

#	Part Number	Item	Quantity
1	EV8865-Q-00A	MP8865GQ evaluation board	1
2	EVKT-USBI2C-02	Includes one USB to I2C dongle, one USB cable, and one ribbon cable	1
3	Tdrive-8865	USB flash drive that stores the GUI installation file and supplemental documents	1

Order direct from MonolithicPower.com or our distributors

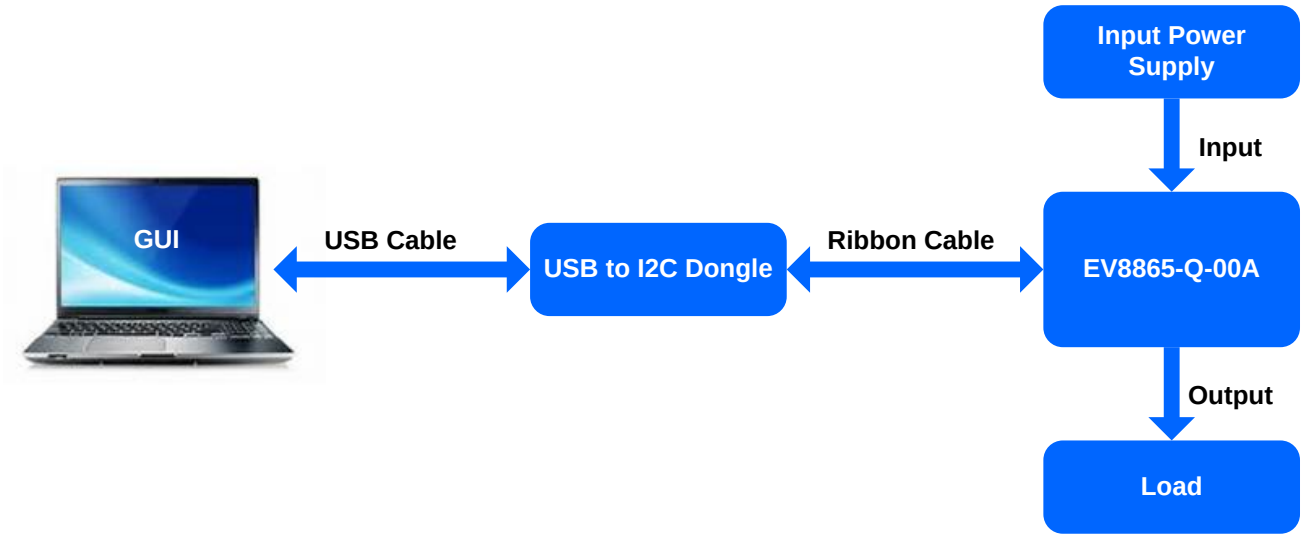
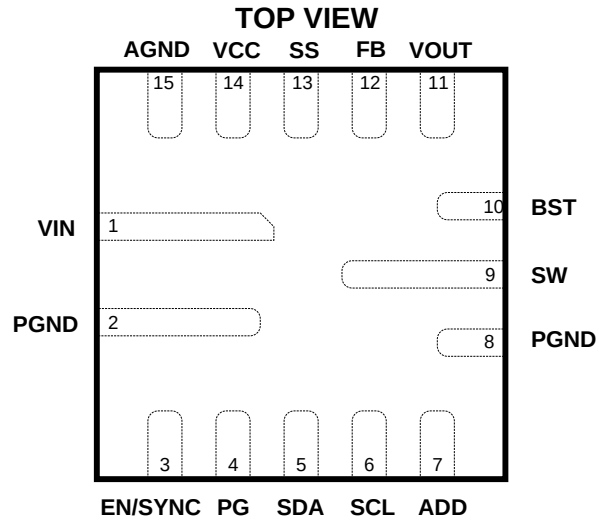


Figure 1: EVKT-8865 Evaluation Kit Set-Up

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

PACKAGE REFERENCE



QFN-15 (3mmx3mm)

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} …….. .....-0.3V to 22V
V_{SW}.....
-0.3V (-5V for <10ns) to V_{IN}+0.3V (27V for <25ns)
V_{BST} ……. V_{SW}+5.5V
All Other Pins…… ..... -0.3V to 5.4V (2)
Continuous Power Dissipation (T_A = +25°C) (3)
……...2.5W
Junction Temperature……..….150°C
Lead Temperature……260°C
Storage Temperature……-65°C to 150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN}……..4.5V to 21V
Output Voltage V_{OUT}…… .....
……0.6V to V_{IN} x D_{MAX} or 5.2V(5)
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (6) θ_{JA} θ_{JC}

QFN-15 (3mmx3mm)….. ..... …50…12…°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Please refer to the “Enable/SYNC” control section on page 15 for the absolute maximum rating of EN.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) The output voltage CANNOT exceed the 5.2V absolute maximum value at any input condition.
6) Measured on JESD51-7, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to 125°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V, T_J=25°C			5	μA
Supply Current (Quiescent)	I_q	V_{EN} = 2V, No Switching, PFM Mode		500	760	μA
HS Switch-On Resistance	HS_{RDS-ON}	V_{BST-SW}=5V		45		mΩ
LS Switch-On Resistance	LS_{RDS-ON}	V_{CC} =5V		18		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V			1	μA
Current Limit (7)	I_{LIMIT}	Under 40% Duty Cycle	7.5	9.5		A
Default Oscillator Frequency	f_{SW}	V_{FB}=500mV	480	600	680	kHz
Foldback Frequency	f_{FB}	V_{FB}=250mV		0.5		f_{SW}
Maximum Duty Cycle	D_{MAX}	V_{FB}=500mV	90	95		%
Minimum On Time(7)	t_{ON_MIN}			60		ns
Feedback Voltage	V_{REF}	T_J =25°C	594	600	606	mV
	V_{REF}	T_J = -40°C to 125°C	588	600	612	mV
VOUT	V_{OUT}=1.2V	T_J = 25°C	1188	1200	1212	mV
	V_{OUT}=1.2V	T_J = -40°C to 125°C	1182	1200	1218	mV
FB Current	I_{OUT}	V_{FB}=620mV		10	50	nA
EN Rising Threshold	V_{EN_Rise}		1.2	1.4	1.6	V
EN Hysteresis	V_{EN_HYS}			150		mV
EN Input Current	I_{EN}	V_{EN}=2V		2		μA
SYNC Frequency Range	f_{SYNC}		0.3		2	MHz
ADD High Level	V_{ADD_H}		2			V
ADD Low Level	V_{ADD_L}				0.4	V
VIN Under-Voltage Lockout Threshold-Rising	$INUV_{Vth}$		3.8	4	4.25	V
VIN Under-Voltage Lockout Threshold-Hysteresis	$INUV_{HYS}$			600		mV
VCC Regulator	V_{CC}			5		V
VCC Load Regulation		I_{CC}=5mA		1.5		%
Power Good Threshold Rising	PGVth-Hi	V_{REF}=600mV		0.9		VOUT
Power Good Threshold Falling	PGVth-Lo	V_{REF}=600mV		0.7		VOUT
Power Good Deglitch time (7)	PGTd			80		μs
Soft-Start Current	I_{SS}		6	12	18	μA
Thermal Shutdown (7)	T_{TSD}			160		°C
Thermal Hysteresis (7)	T_{TSD_HYS}			20		°C
DAC Resolution(7)	DAC			7		Bits

Notes:

7) Guaranteed by design and characterization test.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

I/O Level Characteristics

Parameter	Symbol	Condition	HS-Mode		LS-Mode		Units
			Min	Max	Min	Max	
Low-Level Input Voltage	V_{IL}		-0.5	$0.3V_{Bus}$	-0.5	$0.3V_{Bus}$	V
High-Level Input Voltage	V_{IH}		$0.7V_{Bus}$	V_{Bus}+0.5	$0.7V_{Bus}$	V_{Bus}+0.5	V
Hysteresis of Schmitt Trigger Inputs	V_{HYS}	V_{Bus}>2V	$0.05V_{Bus}$	-	$0.05V_{Bus}$	-	V
		V_{Bus}<2V	$0.1V_{Bus}$	-	$0.1V_{Bus}$	-	
Low-Level Output Voltage(Open drain) at 3mA Sink Current	V_{OL}	V_{Bus}>2V	0	0.4	0	0.4	V
		V_{Bus}<2V	0	$0.2V_{Bus}$	0	$0.2V_{Bus}$	
Low-Level Output Current	I_{OL}		-	3	-	3	mA
Transfer Gate On Resistance for Currents between SDA and SCAH, or SCL and SCLH	R_{onL}	VOL Level, IOL=3mA	-	50	-	50	Ω
Transfer Gate On Resistance between SDA and SCAH, or SCL and SCLH	R_{onH}	Both Signals (SDA and SDAH, or SCL and SCLH) at V_{Bus} Level	50	-	50	-	kΩ
Pull-Up Current of the SCLH Current Source	I_{cs}	SCLH Output Levels between $0.3V_{Bus}$ and $0.7V_{Bus}$	2	6	2	6	mA
Rise Time of the SCLH or SCL Signal	t_{rCL}	Output Rise Time (Current Source Enabled) with an External Pull-Up Current Source of 3mA					
		Capacitive Load from 10pF to 100pF	10	40			ns
		Capacitive Load of 400pF	20	80			ns
Fall Time of the SCLH or SCL Signal	t_{fCL}	Output Fall Time (Current Source Enabled) with an External Pull-Up Current Source of 3mA					
		Capacitive Load from 10pF to 100pF	10	40			ns
		Capacitive Load of 400pF	20	80	20	250	ns

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

I/O Level Characteristics *(continued)*

Parameter	Symbol	Condition	HS-Mode		LS-Mode		Units
			Min	Max	Min	Max	
Rise Time of SDAH Signal	t_{rDA}	Capacitive Load from 10pF to 100pF	10	80	-	-	ns
		Capacitive Load of 400pF	20	160	20	250	ns
Fall Time of SDAH Signal	t_{fDA}	Capacitive Load from 10pF to 100pF	10	80	-	-	ns
		Capacitive Load of 400pF	20	160	20	250	ns
Pulse Width of Spikes that must be Suppressed by the Input Filter	t_{SP}		0	10	0	50	ns
Input Current for each I/O Pin	I_i	Input Voltage between $0.1V_{Bus}$ and $0.9V_{Bus}$	-	10	-10	+10	µA
Capacitance for each I/O Pin	C_i		-	10	-	10	pF

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

I²C Port Signal Characteristics

Parameter	Symbol	Condition	Cb=100pF		Cb=400pF		Units
			Min	Max	Min	Max	
SCLH and SCL Clock Frequency	f_{SCHL}		0	3.4	0	0.4	MHz
Set-Up Time for a Repeated Start Condition	$T_{SU;STA}$		160	-	600	-	ns
Hold Time (repeated) Start Condition	$T_{HD;STA}$		160	-	600	-	ns
Low Period of the SCL Clock	t_{LOW}		160	-	1300	-	ns
High Period of the SCL Clock	t_{HIGH}		60	-	600	-	ns
Data Set-Up Time	$T_{SU:DAT}$		10	-	100	-	ns
Data Hold Time	$T_{HD;DAT}$		0	70	0	-	ns
Rise Time of SCLH Signal	t_{rCL}		10	40	20*0.1Cb	300	ns
Rise Time of SCLH Signal after a Repeated Start Condition and after an Acknowledge Bit	t_{fCL1}		10	80	20*0.1Cb	300	ns
Fall Time of SCLH Signal	T_{fCL}		10	40	20*0.1Cb	300	ns
Rise Time of SDAH Signal	t_{fDA}		10	80	20*0.1Cb	300	ns
Fall Time of SDAH Signal	T_{fDA}		10	80	20*0.1Cb	300	ns
Set-Up Time for Stop Condition	$T_{SU;STO}$		160	-	600	-	ns
Bus Free Time between a Stop and Start Condition	T_{BUF}		160	-	1300	-	ns
Data Valid Time	$T_{VD;DAT}$		-	16	-	90	ns
Data Valid Acknowledge Time	$T_{VD;ACK}$		-	160	-	900	ns
Capacitive Load for each Bus Line	C_b	SDAH and SCLH Line	-	100	-	400	pF
		SDAH+SDA Line and SCLH+SCL Line	-	400	-	400	pF
Noise Margin at the Low Level	C_i	For each Connected Device	-	$0.1V_{Bus}$	$0.1V_{Bus}$	-	V
Noise Margin at the High Level	V_{nH}	For each Connected Device	-	$0.2V_{Bus}$	$0.2V_{Bus}$	-	V

Notes:

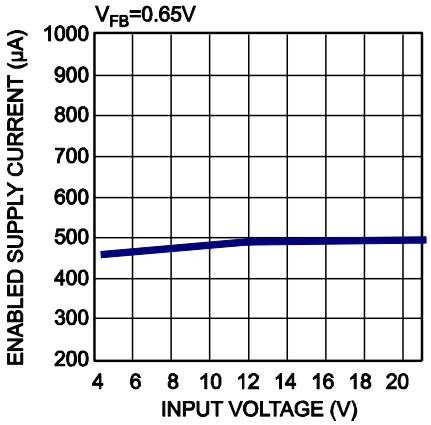
V_{Bus} is the I²C bus voltage, 3.0V to 3.6V range (3.3V typically).

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

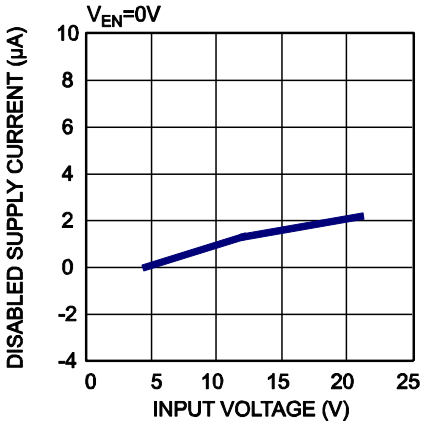
TYPICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.2V, L = 1µH, T_A = 25°C, unless otherwise noted.

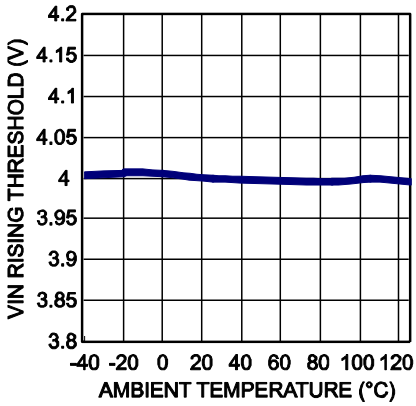
Enabled Supply Current vs. Input Voltage



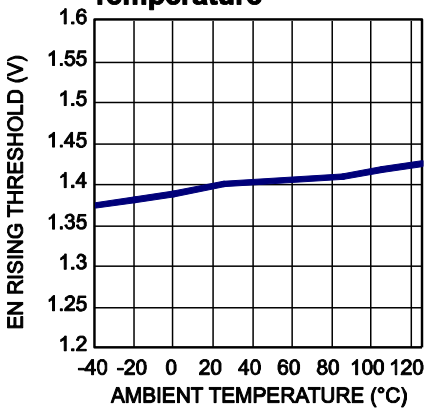
Disabled Supply Current vs. Input Voltage



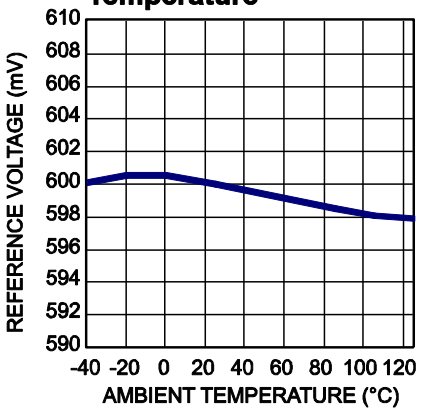
VIN UVLO Rising Threshold vs. Temperature



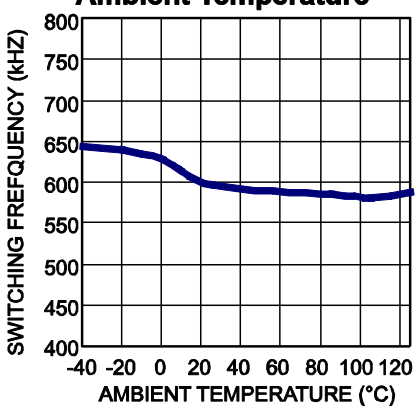
EN Rising Threshold vs. Temperature



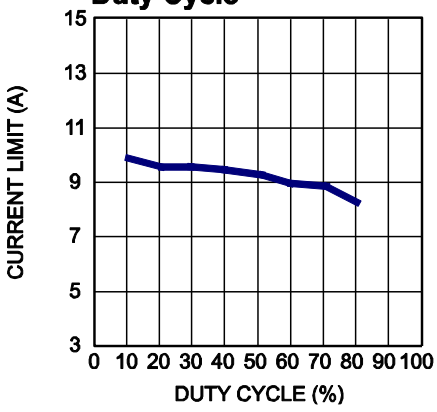
Reference Voltage vs. Temperature



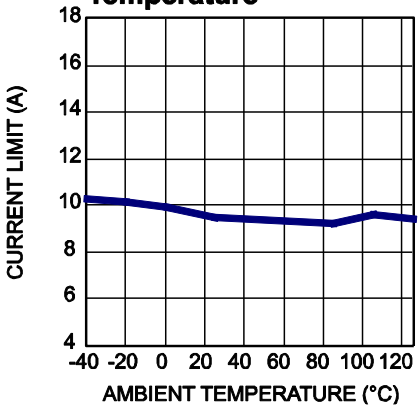
Switching Frequency vs. Ambient Temperature



Current Limit vs. Duty Cycle



Current Limit vs. Temperature

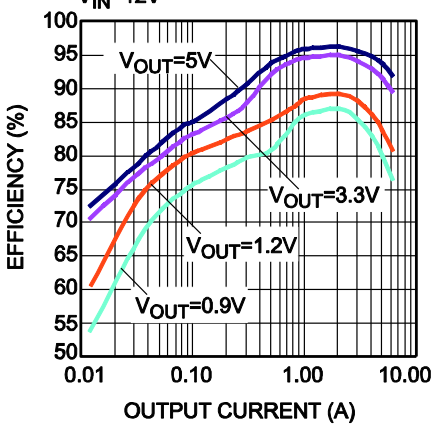


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

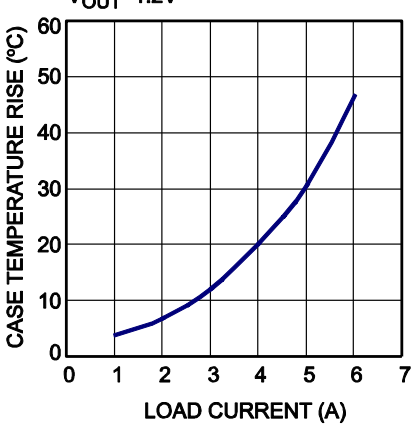
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1.2V, L = 1µH, T_A = 25°C, unless otherwise noted.

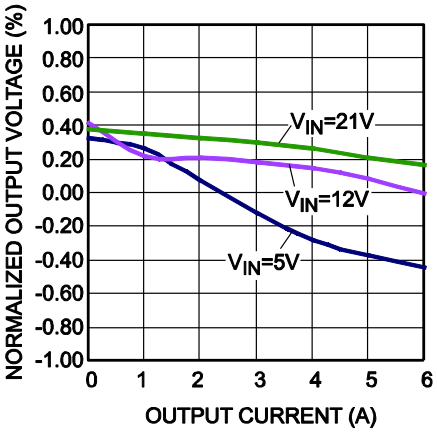
Efficiency vs. Output Current



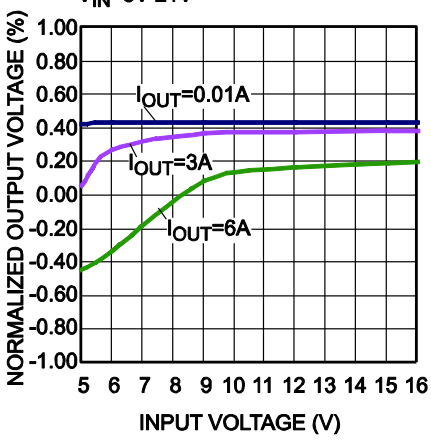
Case Temperature Rise vs. I_{OUT}



Load Regulation



Line Regulation

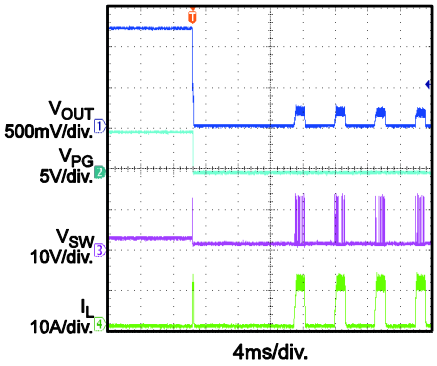


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

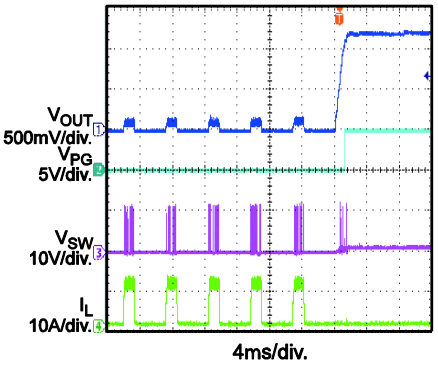
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1.2V, L = 1µH, T_A = 25°C, unless otherwise noted.

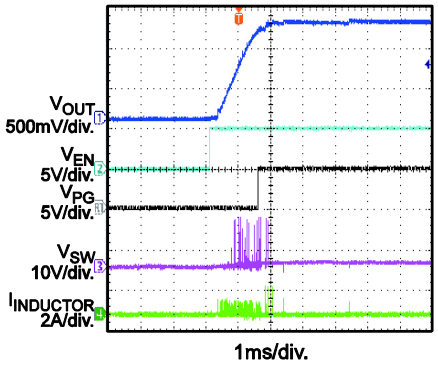
Short Entry
I_{OUT} = 0A



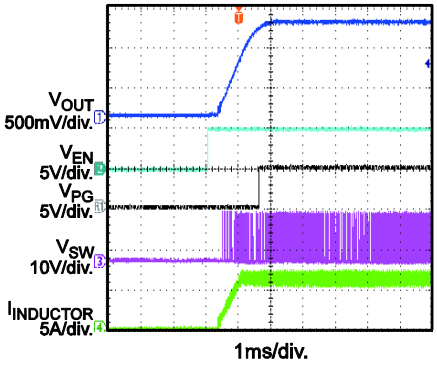
Short Recovery
I_{OUT} = 0A



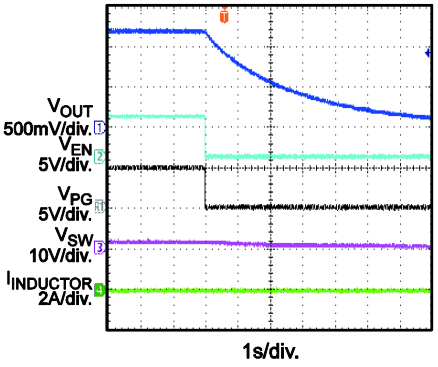
Start-Up through Enable
I_{OUT} = 0A



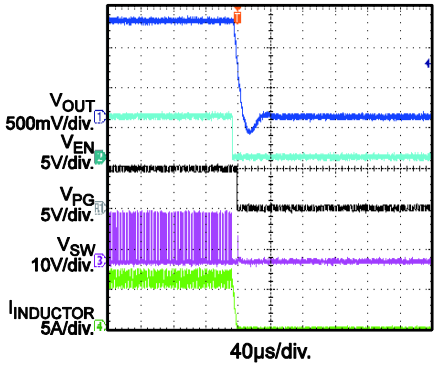
Start-Up through Enable
I_{OUT} = 6A



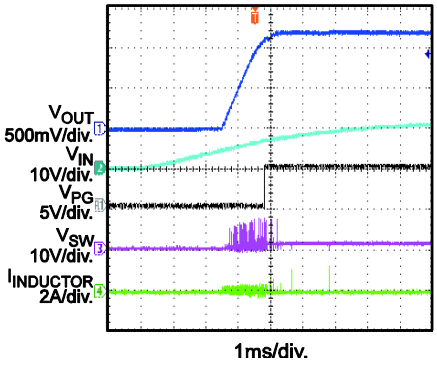
Shutdown through Enable
I_{OUT} = 0A



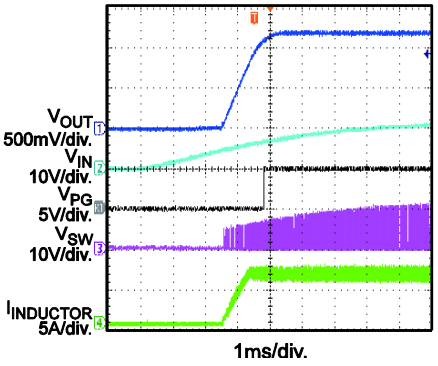
Shutdown through Enable
I_{OUT} = 6A



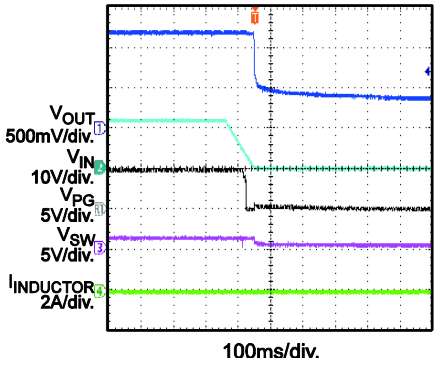
Start-Up through Input Voltage
I_{OUT} = 0A



Start-Up through Input Voltage
I_{OUT} = 6A



Shutdown through Input Voltage
I_{OUT} = 0A

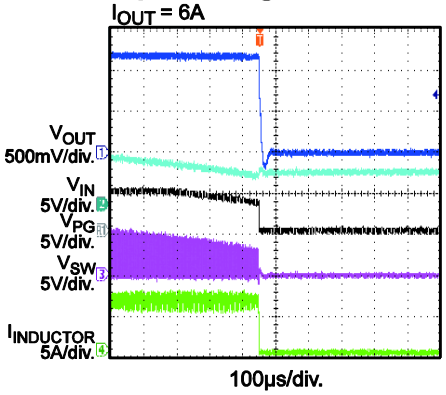


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

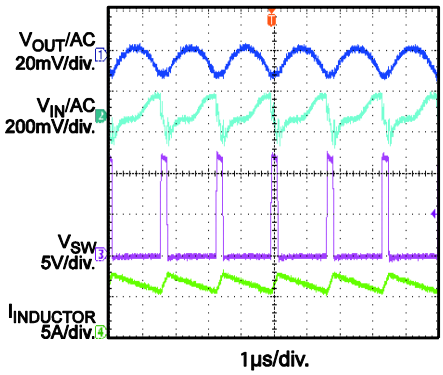
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1.2V, L = 1µH, T_A = 25°C, unless otherwise noted.

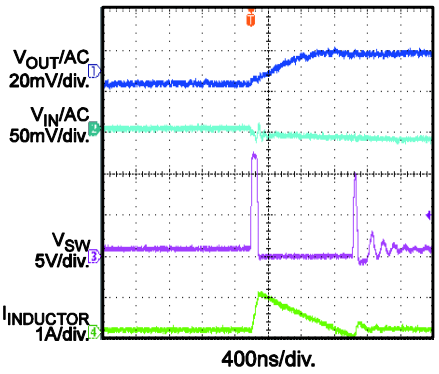
Shutdown through Input Voltage
I_{OUT} = 6A



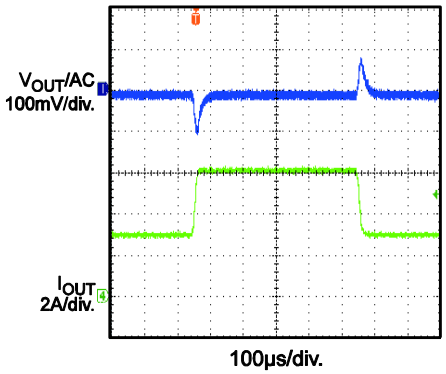
Input/Output Ripple
I_{OUT} = 6A



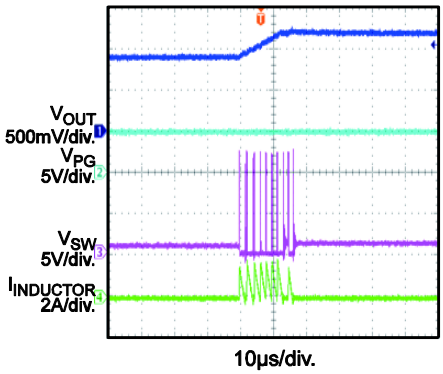
Input/Output Ripple
I_{OUT} = 0A



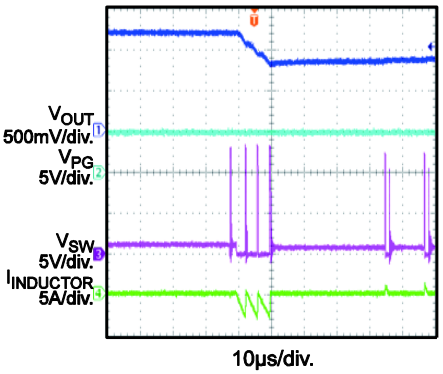
Load Transient Response
I_{OUT} = 3A to 6A



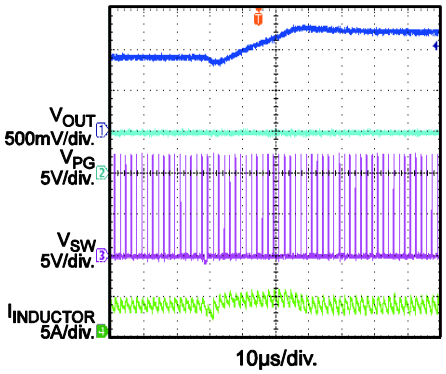
I²C Control Slew Rate
Slew rate=16mV/µs, I_{OUT} = 0A, from 0.9V to 1.2V



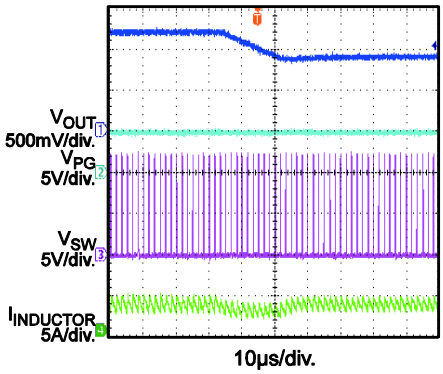
I²C Control Slew Rate
Slew rate=16mV/µs, I_{OUT} = 0A, from 1.2V to 0.9V



I²C Control Slew Rate
Slew rate=16mV/µs, I_{OUT} = 3A, from 0.9V to 1.2V



I²C Control Slew Rate
Slew rate=16mV/µs, I_{OUT} = 3A, from 1.2V to 0.9V



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	VIN	Supply Voltage. The MP8865 operates from a 4.5V to 21V input rail. VIN requires a ceramic capacitor to decouple the input rail. Connect using a wide PCB trace.
2, 8	PGND	System Ground. Reference ground of the regulated output voltage. PGND requires special consideration during PCB layout (see the “PCB Layout Guidelines” section on page 24). Connect PGND to GND with copper traces and vias.
3	EN/SYNC	Enable/Synchronize. EN=high to enable the MP8865. EN/SYNC has an internal 1MΩ pull-down resistor to ground.
4	PG	Power Good. Open-drain structure.
5	SDA	I^2C Serial Data.
6	SCL	I^2C Serial Clock.
7	ADD	I^2C Address Set. Floating ADD or pulling it to VCC sets *one* address. Pulling ADD to ground sets an additional addresses.
9	SW	Switch Output. Connect SW using a wide PCB trace.
10	BST	Bootstrap. BST requires a capacitor between SW and BST to form a floating supply across the high-side switch driver.
11	VOUT	Sense Input of Output Voltage in the I^2C Control Loop.
12	FB	Feedback. Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage in the FB control loop. Connecting FB to VCC sets the default output voltage at 0.9V.
13	SS	Soft-Start. Connecting a capacitor from SS to ground sets the soft-start time.
14	VCC	Internal 5V LDO Regulator Output. Decouple with a 0.22µF capacitor.
15	AGND	Signal Ground. AGND is NOT connected internally to system ground. Ensure AGND is connected to system ground in the PCB layout.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

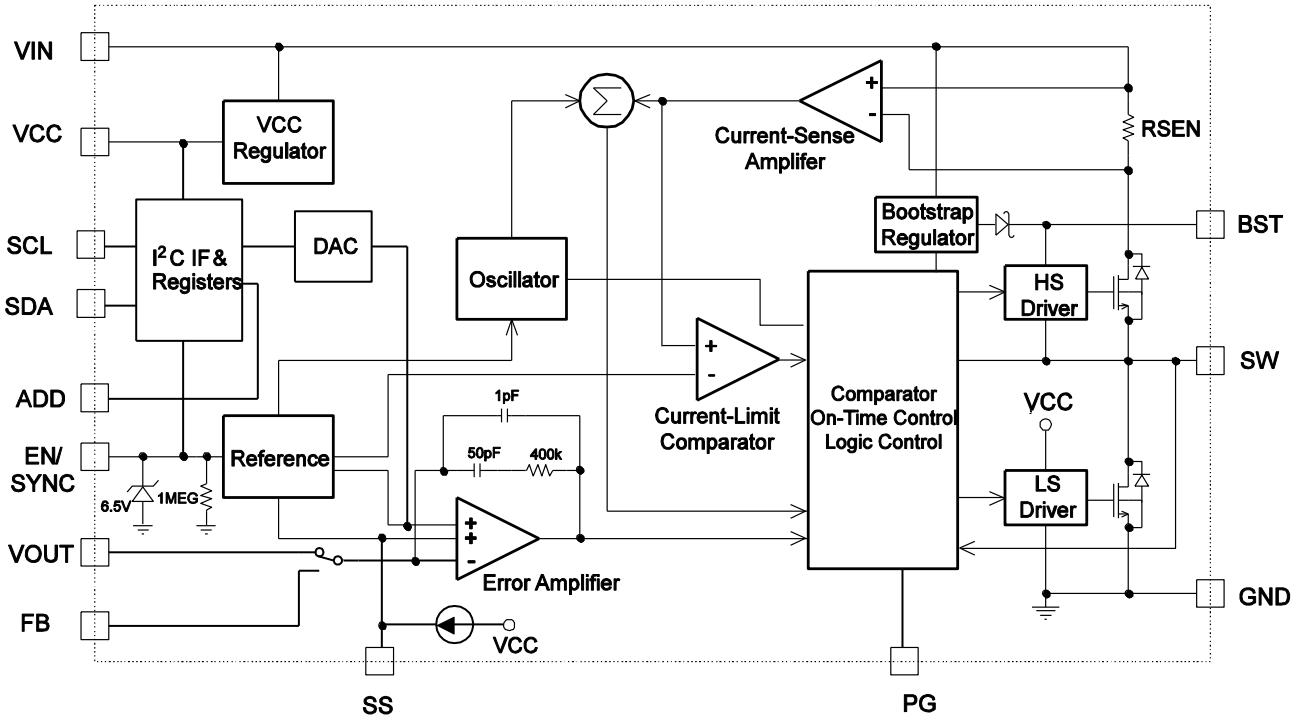


Figure 2. Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

OPERATION

The MP8865 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution that achieves a 6A continuous output current with excellent load and line regulation over a wide input-supply range.

The MP8865 has three working modes: advanced asynchronous modulation (AAM), discontinuous conduction mode (DCM), and continuous conduction mode (CCM). When the MODE bit in the I²C register is set to 1, the MP8865 works in CCM constantly.

AAM Control Operation

In a light-load condition, MP8865 works in AAM mode (see Fig. 3). The V_{AAM} is an internally fixed voltage when input and output voltages are fixed. V_{COMP} is the error amplifier output, which represents the peak inductor current information. When V_{COMP} is lower than V_{AAM}, the internal clock is blocked. This causes the MP8865 to skip pulses, achieving the light-load power save. For additional details, refer to AN032.

The internal clock re-sets every time V_{COMP} is higher than V_{AAM}. At the same time, the high-side MOSFET (HS-FET) turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}.

The light-load feature in this device is optimized for 12V input applications.

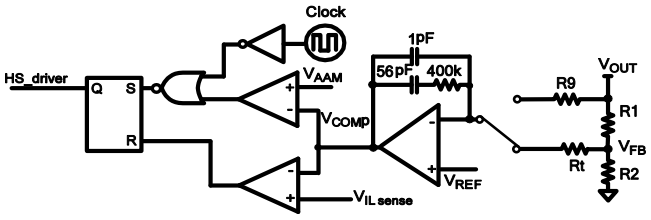


Figure 3. Simplified AAM Control Logic

DCM Control Operation

The V_{COMP} voltage ramps up as the output current increases. When its minimum value exceeds V_{AAM}, the device enters DCM. In this mode, the internal clock initiates the PWM cycle, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP} (after a period of dead time), and the low-side MOSFET(LS-FET) turns on and remains on until the inductor-current value decreases to zero. The device repeats the same operation in every clock cycle to regulate the output voltage (see Fig. 4).

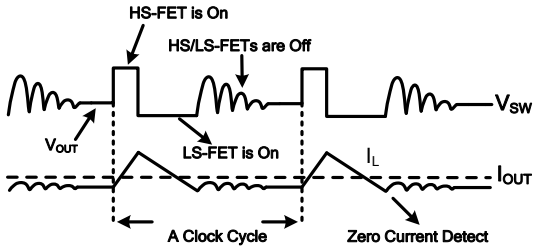


Figure 4. DCM Control Operation

CCM Control Operation

The device enters CCM from DCM once the inductor current no longer drops to zero in a clock cycle. In CCM, the internal clock initiates the PWM cycle, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP} (after a period of dead time), and the LS-FET turns on and remains on until the next clock cycle starts. The device repeats the same operation in every clock cycle to regulate the output voltage.

If $V_{ILsense}$ does not reach the value set by V_{COMP} within 95% (600kHz switching frequency) of one PWM period, the HS-FET is forced off.

Internal Regulator

A 5V internal regulator powers most of the internal circuitries. This regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} is greater than 5.0V, the output of the regulator is in full regulation. When V_{IN} is lower than 5.0V, the output voltage decreases. A 0.22μF ceramic capacitor is required for decoupling.

Error Amplifier (EA)

The error amplifier compares the FB voltage against the internal reference (REF) in the FB control loop and outputs the COMP voltage (which controls the power MOSFET current). In a I²C control loop, FB opens and VOUT is connected to the EA non-inverter input. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

Enable/SYNC Control

EN/SYNC is a digital control pin that turns the regulator, including the I²C block, on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. An internal 1MΩ resistor from EN to GND allows EN/SYNC to be floated to shut down the chip.

EN is clamped internally using a 6.5V series-Zener-diode (see Fig. **Error! Reference source not found.**5). Connecting the EN input through a pull-up resistor to the voltage on VIN limits the EN input current to less than 100μA.

Connecting EN directly to a voltage source without a pull-up resistor requires limiting the amplitude of the voltage source to <6V to prevent damage to the Zener diode.

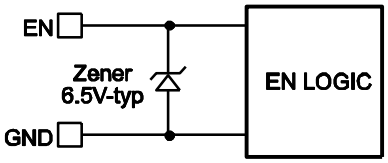


Figure 5. 6.5V Zener Diode Connection

The chip can be synchronized to an external clock range from 300kHz up to 2MHz through EN (as soon as an external clock is added); the internal clock rising edge is synchronized to the external clock rising edge. Select an external clock signal with a pulse width less than 80% of one internal clock cycle time.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP8865 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 4V while its falling threshold is 3.4V.

Soft-Start (SS)

The MP8865 employs a soft-start (SS) mechanism to ensure a smooth output during power-up. When EN becomes high, an internal current source (12μA) charges up the SS capacitor. The SS capacitor voltage takes over the V_{REF} voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once the SS voltage reaches the same level as the V_{REF} voltage, it keeps ramping up while V_{REF} takes over the PWM comparator. At this point, the soft-start is complete and the device enters steady-state operation.

The SS capacitor value can be determined as follows:

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)}$$

If the output capacitors have a large capacitance value, it is NOT recommended to set the SS time too small. Otherwise, it will be easy to hit the current limit during SS.

Pre-Bias Start-Up

The MP8865 has been designed for a monotonic start-up into a pre-biased output voltage. If the output is pre-biased to a certain voltage during start-up, the voltage on the soft-start capacitor will be charged. When the soft-start capacitor's voltage exceeds the sensed output voltage at FB**(8),** the part turns on the high-side and low-side power switches sequentially. Output voltage starts to ramp up following the soft-start slew rate.

Note:

8) FB voltage in the FB control loop or VOUT voltage in the I²C control loop.

Power Good (PG) Indicator

The MP8865 has a power good (PG) output used to indicate whether the output voltage of the module is ready. PG is an open-drain output. Connect PG to VCC (or another voltage source) through a pull-up resistor (e.g. 100kΩ). When the input voltage is applied, PG is pulled down to GND before the internal SS is ready (V_{SS}>1.15xV_{REF}). After SS is ready (when V_{FB}(8) is above 90% of V_{REF}), PG is pulled high (after a 80us delay). During normal operation, PG is pulled low when the V_{FB}(8) drops below 70% of V_{REF} (after a 80us delay).

When UVLO or OTP occurs, PG is pulled low immediately; when OC (over current) occurs, PG is pulled low when V_{FB}(8) drops below 70% of V_{REF} (after a 80us delay).

PG will NOT respond to an output over-voltage condition.

The PG bit in the I²C register has the same indication as the external PG.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

Output Over-Voltage Protection (OVP)

The MP8865 monitors the resistor divider V_{FB} (8) to detect over voltage. When V_{FB}(8) becomes higher than 115% of the target voltage, the LS-FET remains on until the LS current drops to -2.5A. This discharges the output and tries to keep it within the normal range. The device will exit this regulation period when V_{FB}(8) drops below 105% of the reference voltage.

Over-Current Protection (OCP) and Hiccup

The MP8865 has a cycle-by-cycle over-current limit control. When the inductor-current peak value exceeds the set current-limit threshold, the HS-FET turns off, and the LS-FET turns on and remains on until the inductor current falls below the internal "valley" current-limit threshold. The "valley" current-limit circuit is employed to decrease the operation frequency after the "peak" current-limit threshold is triggered. Meanwhile, the output voltage drops until V_{FB}(8) is below the under-voltage (UV) threshold (50% below the reference, typically). Once UV is triggered, the MP8865 enters hiccup mode to re-start the part periodically. This protection mode is useful when the output is dead-shorted to ground. The average short-circuit current is reduced greatly to alleviate thermal issues and protect the regulator. The MP8865 exits hiccup mode once the over-current condition is removed.

Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the die temperature exceeds 160°C, it shuts down the whole chip. When the temperature is less than its lower threshold (140°C, typically) the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C4, L1, and C_{OUT} (see Fig. 6). If (V_{BST}-V_{SW}) exceeds 5V, U1 regulates M1 to maintain a 5V BST voltage across C4. A 10Ω resistor placed between SW and the BST capacitor is recommended to reduce SW spike voltage.

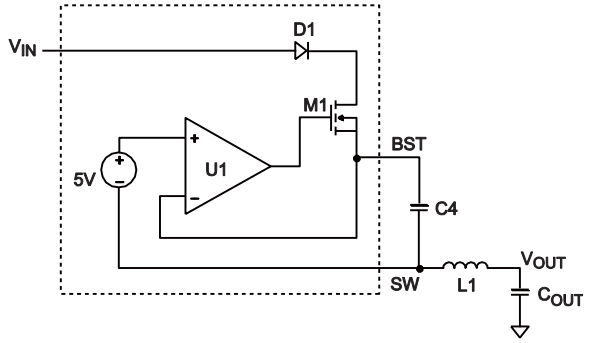


Figure 6. Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

I²C Control and Default Output Voltage

When the MP8865 is enabled (which means EN=high, and VIN>UVLO), the chip starts up to an output voltage set by the FB feedback resistors (with a programmed soft-start time). After the MP8865 is enabled, the I²C bus can communicate with the master. If the chip doesn't receive a I²C communication signal constantly, it works efficiently through FB feedback and performs behavior similar to a traditional non-I²C part.

Once the I²C receives a valid output reference and voltage scaling instruction (if V_BOOT="1"), the output voltage is determined by the resistor dividers R1, R2, and V_{REF} voltage. The V_{OUT} value can be calculated by the following equation (V_{REF} default value is 0.6V):

$$V_{OUT} = V_{REF} \times (1 + \frac{R1}{R2})$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

If V_BOOT="0," the output voltage is determined by the I²C control loop (output voltage is sensed through VOUT), and the FB feedback control loop is disabled.

If FB is pulled up to VCC, the chip starts up directly to the default 0.9V output voltage. In this case, the output voltage is determined by the I²C control loop.

The output reference voltage scaling is realized by adjusting the internal reference voltage (V_REF), which is the non-inverted input of the error amplifier. After the MP8865 receives a valid data byte of the output reference voltage setting, it searches the corresponding reference voltage from the truth table and then sends the command to adjust V_{REF} with a controlled slew rate. The slew rate is determined by 3-bits of another register, which can be *read* and *write* accordingly.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

I²C INTERFACE

I²C Serial Interface

The I²C is a 2-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are pulled externally to a bus voltage when they are “idle.” Connected to the line, a master device generates the SCL signal and addresses and arranges the communication sequence. The MP8865 interface is an I²C slave, which supports both fast mode (400kHz) and high-speed mode (3.4Mhz), adding flexibility to the power-supply solution. The output voltage, transition slew rate, and other parameters can be controlled instantaneously by the I²C interface.

Data Validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Fig. 7).

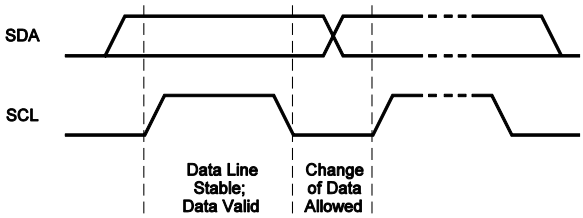


Figure 7. Bit Transfer on the I²C Bus

Start and Stop Conditions

The start and stop conditions are signaled by the master device, which signifies the beginning and the end of the I²C transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Fig. 8).

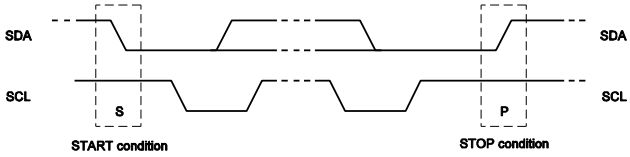


Figure 8. Start and Stop Conditions

Start and Stop conditions are generated always by the master. The bus is considered busy after the start condition. The bus is considered free again after a minimum of 4.7uS after the stop condition. The bus stays busy if a repeated start (Sr) is generated instead of a stop condition. The start (S) and repeated start (Sr) conditions are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8-bits long. Each byte must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (high) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse, so that it remains stable low during the high period of the clock pulse.

Data transfers follow the format shown in Fig. 8. After the start condition (S), a slave address is sent. This address is 7-bits long followed by an eighth bit, which is a data direction bit (R/W). A ‘0’ indicates a transmission (write), and a ‘1’ indicates a request for data (read). A data transfer is terminated always by a stop condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated start condition (Sr) and address another slave without first generating a stop condition.

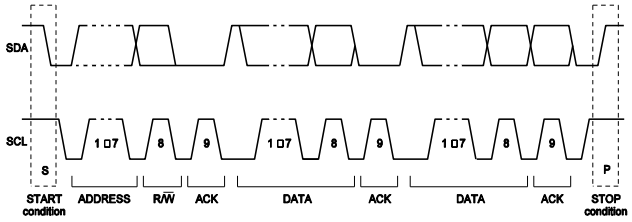


Figure 9. A Complete Data Transfer

The MP8865 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receipt of each byte, the MP8865 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP8865. The MP8865 performs an update on the falling edge of the LSB byte.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

MP8865 I²C Chip Address

ADD sets the MP8865 address. The default 7-bit address of the MP8865 is “68” (hex) or “1101000” (binary) if ADD is floated or pulled up to VCC. The other address of the MP8865 is “60” (hex) or “1100000” (binary) if ADD is pulled to ground. When the master sends the address as an 8-bit value, the 7-bit address should be followed by “0/1” to indicate write/read operation (see Table 1).

TABLE 1. MP8865 Address

ADD	Address (Hex)	Address (Binary)							
		A7	A6	A5	A4	A3	A2	A1	A0 (R/W)
Float or Connected to VCC	D0	1	1	0	1	0	0	0	0
	D1	1	1	0	1	0	0	0	1
Connected to GND	C0	1	1	0	0	0	0	0	0
	C1	1	1	0	0	0	0	0	1

MP8865 Register Address

The MP8865 contains four registers: register 00 to register 03. Register 00 sets the output voltage and decides whether the output voltage is controlled by the FB resistor divider or is set by I²C. Register 01 sets the MP8865 operating features. Register 02 and 03 are the only read registers. Register 03 indicates the MP8865 status. The register map is shown in next section.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

REGISER DESCRIPTION

Register Map

ADD	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	VSEL	R/W	V_BOOT	Output Reference						
01	SysCntlreg1	R/W	EN	GO_BIT	Slew Rate			Switching Frequency		Mode
02	ID1	R	Vendor ID				IC Revision			
03	Status	R	Reserved			VID_OK	OC	OTEW	OT	PG

Register Description

1. **Reg00 VSEL**

NAME	BITS	DEFAULT	DESCRIPTION
V_BOOT	D7	1	"FB" Control Loop Enable Bit. V_BOOT="1" means the output voltage is determined by the resistor divider connected to "FB" (FB control loop). V_BOOT="0" means the output voltage is controlled by I^2C through "VOUT" (I^2C control loop). This bit is helpful for the default output-voltage setting before the I^2C signal comes. If the I^2C is not used, the part works efficiently with "FB."
Output Reference	D[6:0]	0000000	Set the output reference voltage from 0.6V to 1.87V (see Table 1). The default value is 0.6V. If FB is connected to VCC, then the default value is 0.9V.

TABLE 2. Output Reference Voltage Chart

D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT
000 0000	0.60	010 0000	0.92	100 0000	1.24	110 0000	1.56
000 0001	0.61	010 0001	0.93	100 0001	1.25	110 0001	1.57
000 0010	0.62	010 0010	0.94	100 0010	1.26	110 0010	1.58
000 0011	0.63	010 0011	0.95	100 0011	1.27	110 0011	1.59
000 0100	0.64	010 0100	0.96	100 0100	1.28	110 0100	1.60
000 0101	0.65	010 0101	0.97	100 0101	1.29	110 0101	1.61
000 0110	0.66	010 0110	0.98	100 0110	1.30	110 0110	1.62
000 0111	0.67	010 0111	0.99	100 0111	1.31	110 0111	1.63
000 1000	0.68	010 1000	1.00	100 1000	1.32	110 1000	1.64
000 1001	0.69	010 1001	1.01	100 1001	1.33	110 1001	1.65
000 1010	0.70	010 1010	1.02	100 1010	1.34	110 1010	1.66
000 1011	0.71	010 1011	1.03	100 1011	1.35	110 1011	1.67
000 1100	0.72	010 1100	1.04	100 1100	1.36	110 1100	1.68
000 1101	0.73	010 1101	1.05	100 1101	1.37	110 1101	1.69
000 1110	0.74	010 1110	1.06	100 1110	1.38	110 1110	1.70
000 1111	0.75	010 1111	1.07	100 1111	1.39	110 1111	1.71
001 0000	0.76	011 0000	1.08	101 0000	1.40	111 0000	1.72
001 0001	0.77	011 0001	1.09	101 0001	1.41	111 0001	1.73
001 0010	0.78	011 0010	1.10	101 0010	1.42	111 0010	1.74
001 0011	0.79	011 0011	1.11	101 0011	1.43	111 0011	1.75
001 0100	0.80	011 0100	1.12	101 0100	1.44	111 0100	1.76
001 0101	0.81	011 0101	1.13	101 0101	1.45	111 0101	1.77
001 0110	0.82	011 0110	1.14	101 0110	1.46	111 0110	1.78
001 0111	0.83	011 0111	1.15	101 0111	1.47	111 0111	1.79
001 1000	0.84	011 1000	1.16	101 1000	1.48	111 1000	1.80
001 1001	0.85	011 1001	1.17	101 1001	1.49	111 1001	1.81
001 1010	0.86	011 1010	1.18	101 1010	1.50	111 1010	1.82
001 1011	0.87	011 1011	1.19	101 1011	1.51	111 1011	1.83
001 1100	0.88	011 1100	1.20	101 1100	1.52	111 1100	1.84

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT
001 1101	0.89	011 1101	1.21	101 1101	1.53	111 1101	1.85
001 1110	0.90	011 1110	1.22	101 1110	1.54	111 1110	1.86
001 1111	0.91	011 1111	1.23	101 1111	1.55	111 1111	1.87

2. Reg01 SysCntlreg1

NAME	BITS	DEFAULT	DESCRIPTION			
EN	D[7]	1	The I^2C turns the part on or off. When the external EN is low, the converter is off, and I^2C is shutdown. When EN is high, the EN bit will takes over. The default EN bit is "1."			
GO_BIT	D[6]	0	Switch Bit of I^2C Writing Authority for Output Reference Command Only. Set GO_BIT="1" to enable the I^2C authority of the writing output reference. When the command is finished, GO_BIT will auto re-set to "0" to prevent false operation of VOUT scaling. If the reference is adjusted within 50mV, GO_BIT will NOT auto re-set to "0." If this is the case, manually set GO_BIT to "0." Writing GO_BIT="1" first is suggested, then write the output reference voltage.			
Slew Rate	D[5:3]	100	D[5:3]	SLEW RATE	D[5:3]	SLEW RATE
			000	64 mV/uS	100	4 mV/uS
			001	32 mV/uS	101	2 mV/uS
			010	16 mV/uS	110	1 mV/uS
			011	8 mV/uS	111	0.5 mV/uS
Switching Frequency	D[2:1]	00	D[2:1]	Fs		
			00	600kHz		
			01	850kHz		
			10	1.1MHz		
			11	1.6MHz		
Mode	D0	0	"0" enables PFM mode; high disables PFM mode.			

3. Reg02 ID1

NAME	BITS	DESCRIPTION
Vendor ID	D[7:4]	1000
IC Revision	D[3:0]	IC Revision

4. Reg03 Status

NAME	BITS	DESCRIPTION
Reserved	D[7:5]	Reserved for Future Use. Always set at 0.
VID_OK	D[4]	I^2C Controlled Voltage Adjustment is Finished. The internal circuit compares DAC output with "VOUT" voltage. If "VOUT" is in the 90%-110% range of DAC output, the VID_OK bit is high (which means the voltage scaling is finished). Otherwise, VID_OK="0."
OC	D[3]	Output Over-Current Indication. When bit is high, the IC is in hiccup mode.
OTEW	D[2]	Die temperature early warning bit. When the bit is high, the die temperature is higher than 120˚C.
OT	D[1]	Over-Temperature Indication. When the bit is high, the IC is in thermal shutdown.
PG	D[0]	Output Power Good Indication. When the bit is high, the VOUT power is good. This means the VOUT is higher than 90% of the designed regulation voltage. See additional details in the "Power Good (PG) Indicator" section on page 15.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Output Voltage in the FB Control Loop

The reference voltage and the external resistor divider can set the output voltage through FB. Also, the feedback resistor R1 and R_T set the feedback loop bandwidth with the internal compensation capacitor. Choose the value of R1 first; R2 is then given by (9):

$$R2 = \frac{R1}{\frac{V_{OUT}}{V_{REF}} - 1}$$

Notes:

9) VREF is 0.6V when powering up or EN is on. After the MP8865 is enabled, VREF can be programmed through I²C. Set V_BOOT=1 to enable the FB control loop.

The T-type network (see Fig. 10) is recommended highly when V_{OUT} is low.

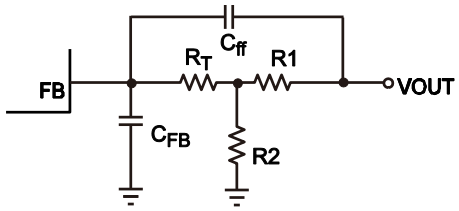


Figure 10. T-Type Network

Table 3 lists the recommended T-type resistor values for common output voltages.

TABLE 3. Resistor Selection for Common Output Voltages with default 0.6V V_{REF}(10)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R_T (kΩ)	Cff (pF)	C_{FB} (pF)	L (uH)
0.9	Connect FB to VCC					1
1	34(1%)	51(1%)	33(1%)	15	10	1
1.2	34(1%)	34(1%)	33(1%)	10	10	1
1.8	34(1%)	16.5(1%)	15(1%)	10	15	1.5
2.5	34(1%)	10.7(1%)	15(1%)	15	22	1.8
3.3	34(1%)	7.5(1%)	15(1%)	15	33	2.7
5	34(1%)	4.64(1%)	7.5(1%)	15	47	2.7

Note:

10) The recommended parameters are based on a 12V input voltage and a 22µFx2 output capacitor. A different input voltage and output capacitor value may affect the selection of R1, R2, RT, Cff, and CFB. For additional component parameters, please refer to the "Typical Application Circuits" section on page 26.

Setting the Output Voltage in the I²C Control Loop

In addition to setting the output voltage through the FB loop, the I²C loop can set the output voltage through VOUT by setting V_BOOT=0. In this case, the output voltage is the set reference voltage. Please refer to Table 2 on page 20 for additional details concerning the output voltage setting.

Output Voltage Dynamic Scale

To dynamic scale the output voltage during normal operation, refer to Fig. 11 and follow the steps below:

Step1: Write the GO_Bit (reg01[6]) to "1;"

Step2: Write reg00 to select the feedback loop by setting V_BOOT(reg00[7]). Set the reference voltage using the output reference (reg00[0:6]) simultaneously. If the reference adjustment is within 50mV, GO_BIT will NOT auto re-set to "0." If this is the case, manually set GO_BIT to "0."

Repeat the two steps above to dynamic scale to another voltage.

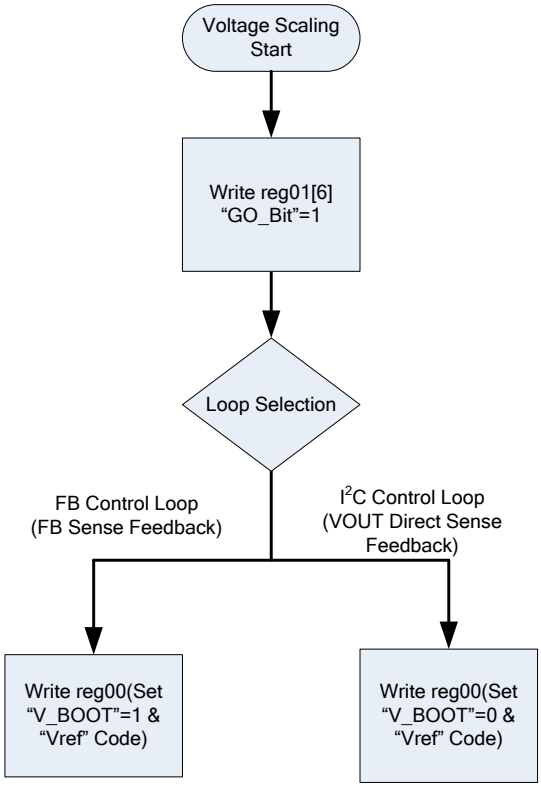


Figure 11. Output Voltage Dynamic Scale Flow Chart

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

Selecting the Inductor

For most applications, use a 1µH to 10µH inductor with a DC current rating at least 25% percent higher than the maximum load current. For highest efficiency, use an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value can be derived from the following equation:

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor-ripple current.

Choose the inductor-ripple current at approximately 30% of the maximum load current. The maximum inductor-peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Use a larger inductor for improved efficiency under light-load conditions—below 100mA.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore it requires a capacitor to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Use ceramic capacitors with X5R or X7R dielectrics for best results because of their low ESR and small temperature coefficients. For most applications, use a 44µF capacitor.

Since C1 absorbs the input-switching current, it requires an adequate ripple-current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge in order to prevent excessive voltage ripple at the input. The input-voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output-voltage ripple low. The output-voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output-voltage ripple. For simplification, the output-voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor affect the stability of the regulation system. The MP8865 can be optimized for a wide range of capacitance and ESR values.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

External Bootstrap Diode

An external bootstrap diode enhances the efficiency of the regulator given the following conditions:

- V_{OUT} is 5V or 3.3V
- The duty cycle is high: $D=\frac{V_{OUT}}{V_{IN}}>65\%$

In these cases, add an external BST diode from VCC to BST (see Fig. 12).

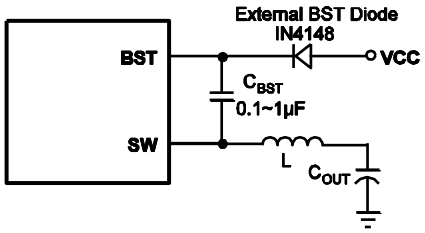


Figure 12. Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BST diode is IN4148, and the BST capacitor value is 0.1μF to 1μF.

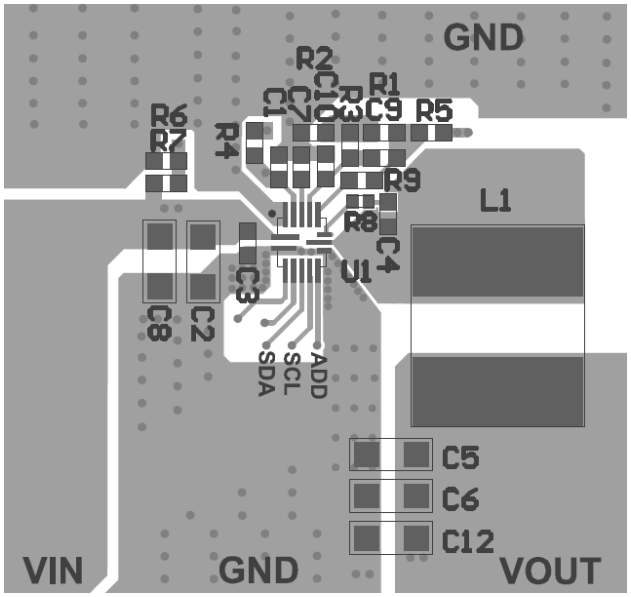
PCB Layout Guidelines[11]

Efficient PCB layout is critical to achieve stable operation, especially for VCC capacitor and input capacitor placement. For best results, refer to Fig. 13 and follow the guidelines below:

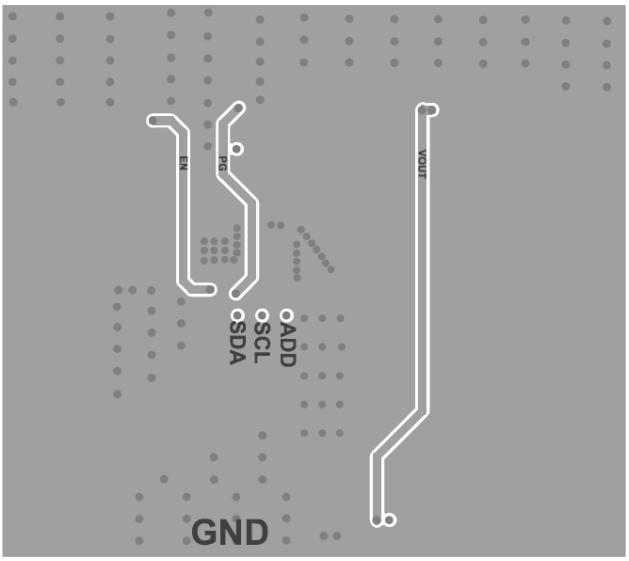
1) Use a large ground plane connected directly to GND. If bottom layer is ground plane, add vias near GND.
2) Place as close as possible the VCC capacitor to VCC and GND. Make the trace length of VCC to the VCC capacitor anode to the VCC capacitor cathode chip to GND as short as possible.
3) Place the ceramic input capacitor close to IN and GND. Keep the connection of the input capacitor and IN as short and wide as possible.
4) Route SW and BST away from sensitive analog areas (such as FB). It is NOT recommended to route SW and BST traces under the chip's bottom layer.
5) Place the T-type feedback resistor R3 close to the chip to ensure the trace (which connects to FB) is as short as possible.

Notes:

11) The recommended layout is based on Fig. 15 in the "Typical Application Circuits" section on page 26.



Top Layer



Bottom Layer

Figure 13. Recommended PCB Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

Design Example

Below is a design example following the application guidelines for the specifications:

TABLE 4. Design Example

V_{IN}	12V
V_{OUT}	1.2V
I_O	6A

The detailed application schematics are shown in Fig. 16. The typical performance and circuit waveforms have been shown in the “Typical Performance Characteristics” section. For more device applications, please refer to the related evaluation board datasheets.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUITS

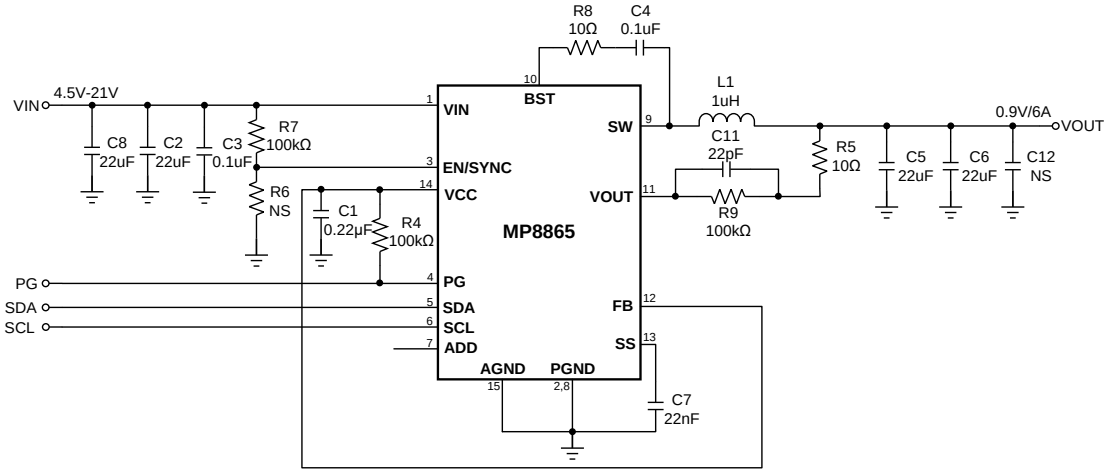


Figure 14. 12V Input-0.9V/6A Output

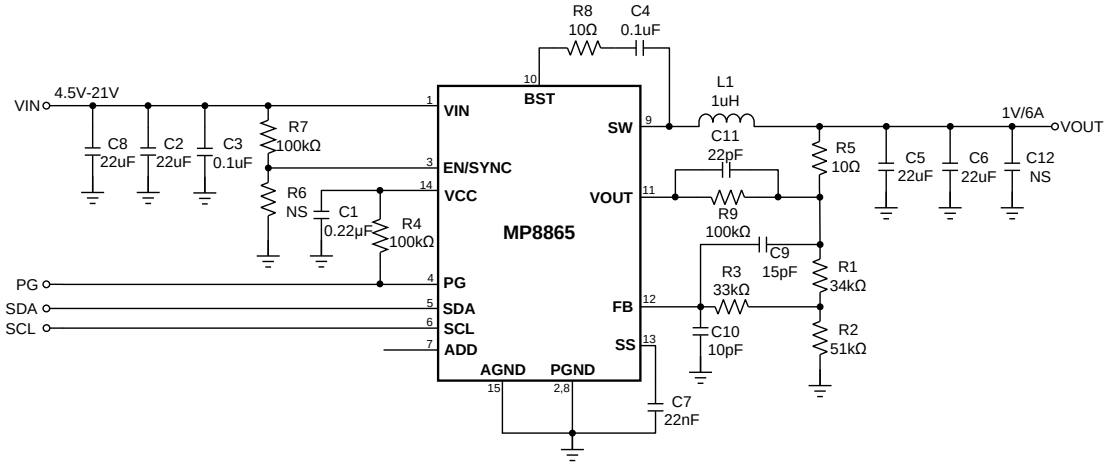


Figure 15. 12V Input-1V/6A Output

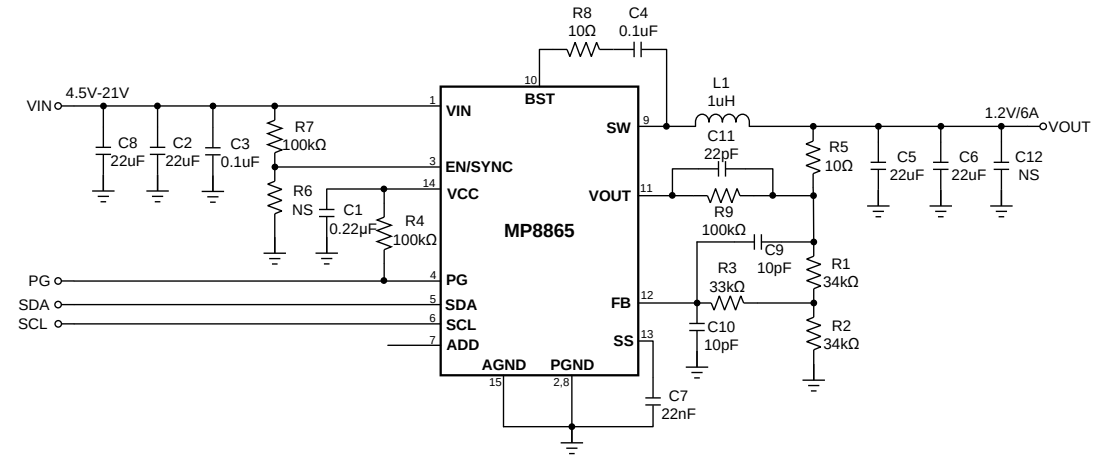


Figure 16. 12V Input-1.2V/6A Output

Notes:
12) Except for Fig. 13, the other circuits are based on a 0.6V default reference voltage.
13) R5 is used for loop test purposes. It is NOT needed if the test loop has a small signal.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

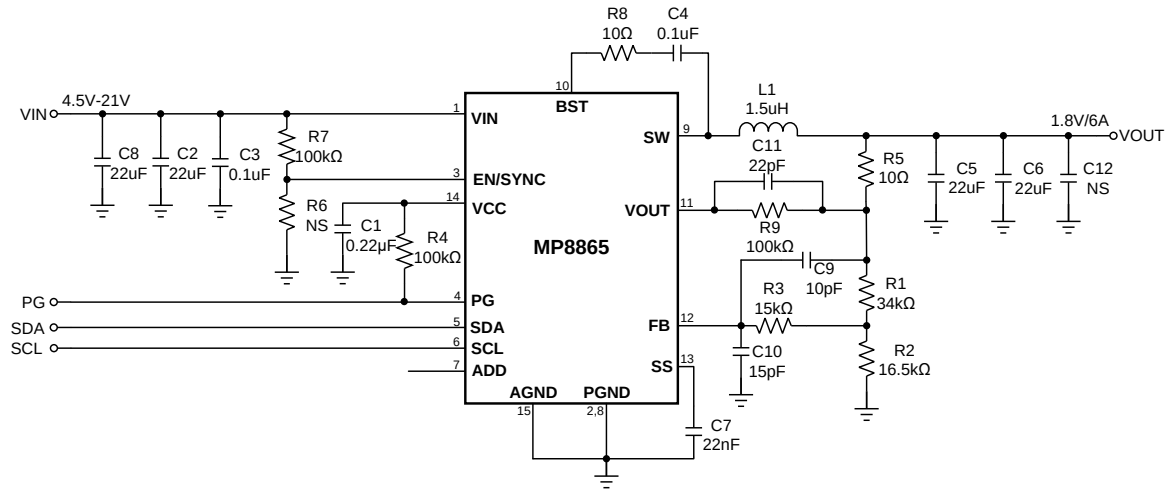


Figure 17. 12V Input-1.8V/6A Output

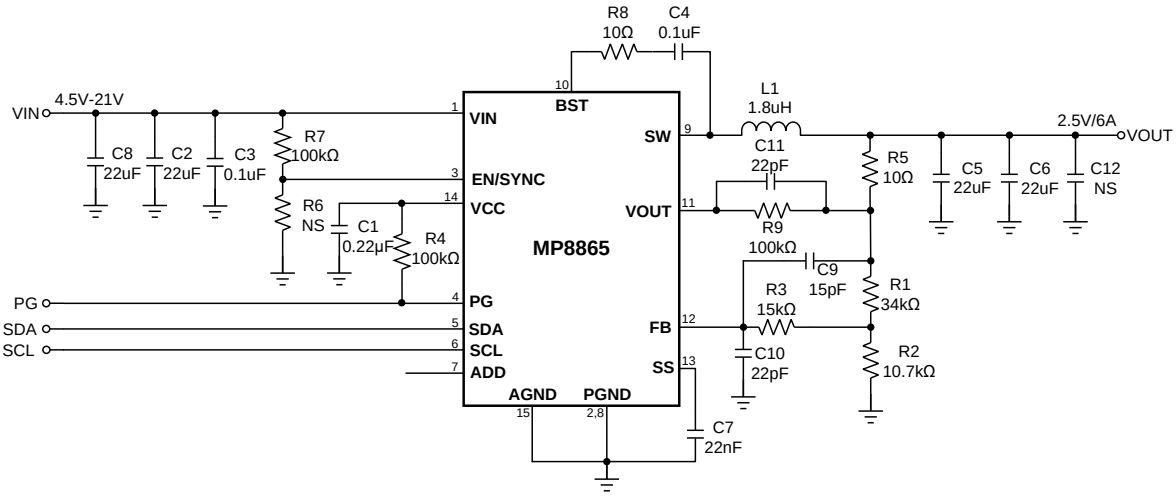


Figure 18. 12V Input-2.5V/6A Output

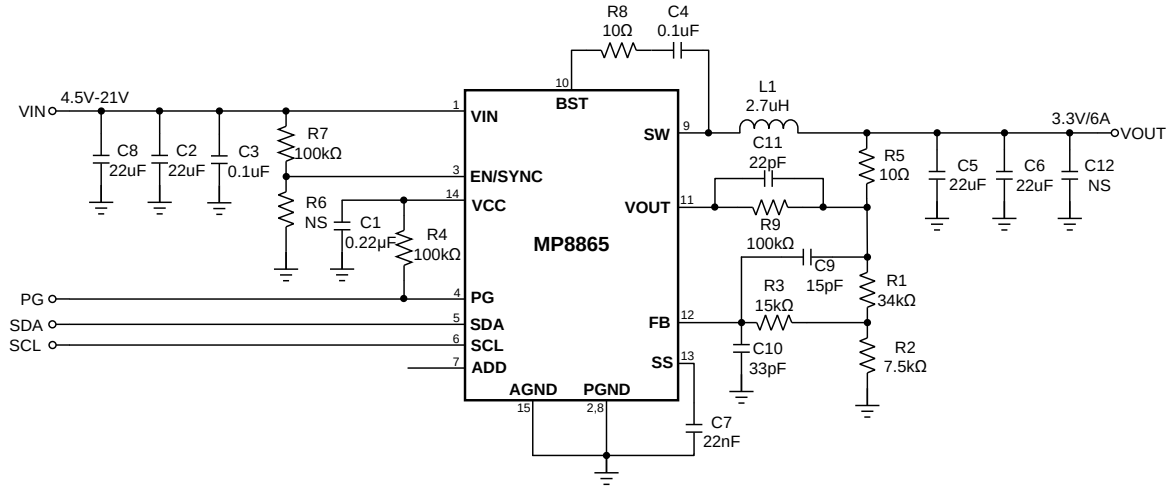


Figure 19. 12V Input-3.3V/6A Output

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

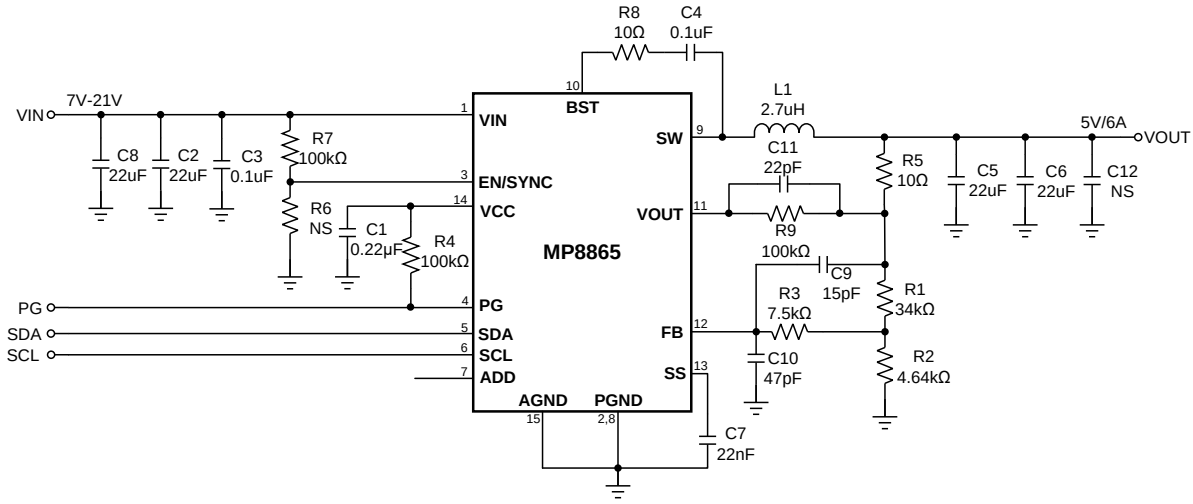
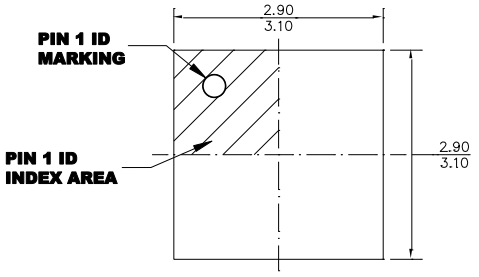


Figure 20. 12V Input-5V/6A Output

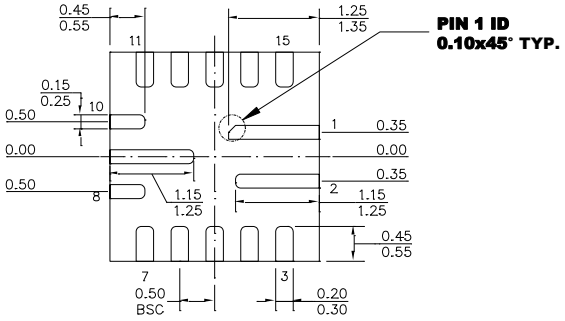
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.

PACKAGE INFORMATION

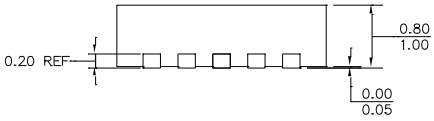
QFN-15 (3mmX3mm)



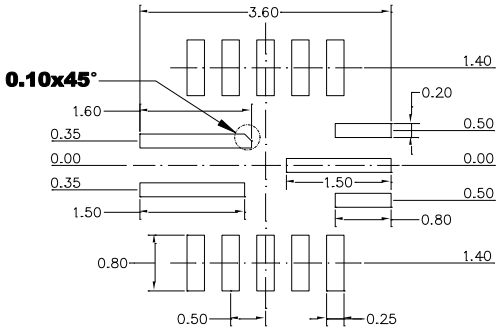
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Please contact MPS for current specifications. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2018 MPS. All Rights Reserved.