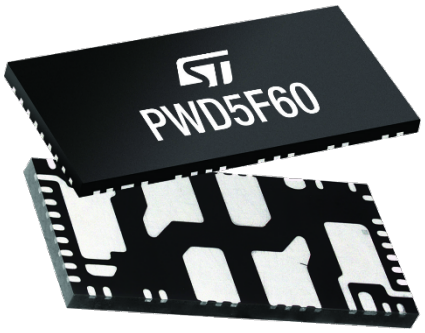
# PWD5F60

Datasheet

## High density power driver - high voltage full bridge with integrated comparators

VFQFPN 15 x 7 x 1 mm




| Product status link |
|---|
| PWD5F60 |

| Product summary | |
|---|---|
| Marking | PWD5F60 |
| Package | VFQFPN 15x7x1mm |
| Order codes | |
| PWD5F60 | Tray |
| PWD5F60TR | Tape and Reel |

## Features

- Power system-in-package integrating gate drivers and high-voltage power MOSFETs
  - $R_{DS(ON)}$ = 1.38 Ω
  - $BV_{DSS}$ = 600 V
- Suitable for operating as
  - full bridge
  - dual independent half bridges
- UVLO protection on low-side and high-side
- 3.3 V to 15 V compatible inputs with hysteresis and pull-down
- Internal bootstrap diode
- Uncommitted comparators
- Adjustable dead-time
- Bill of material reduction
- Very compact and simplified layout
- Flexible, easy and fast design

## Applications

- Industrial fans and pumps
- Cooking hoods and gas heaters
- Blowers
- Industrial drives and factory automation
- Power supply units

## Description

The PWD5F60 is an advanced power system-in package integrating gate drivers and four N-channel power MOSFETs in dual half-bridge configuration.

The integrated power MOSFETs have $R_{DS(ON)}$ of 1.38 Ω and 600 V drain-source breakdown voltage, while the embedded gate drivers high side can be easily supplied by the integrated bootstrap diode. The high integration of the device allows to efficiently drive loads in a tiny space.

The PWD5F60 accepts a supply voltage (VCC) extending over a wide range (10 V to 20 V) and also features UVLO protection on both the lower and upper driving sections, preventing the power switches from operating in low efficiency or dangerous conditions.

The input pins extended range allows easy interfacing with microcontrollers, DSP units or Hall effect sensors.

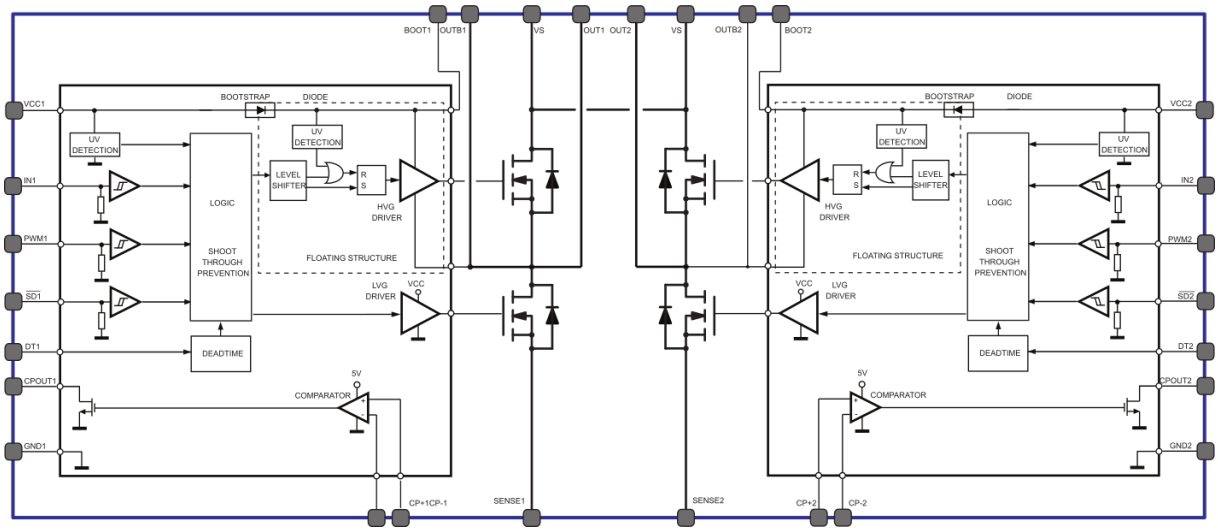
The PWD5F60 embeds two uncommitted comparators available for protections against overcurrent, overtemperature, etc.

The PWD5F60 operates in the industrial temperature range, -40 °C to 125 °C.

The device is available in a compact VFQFPN package.

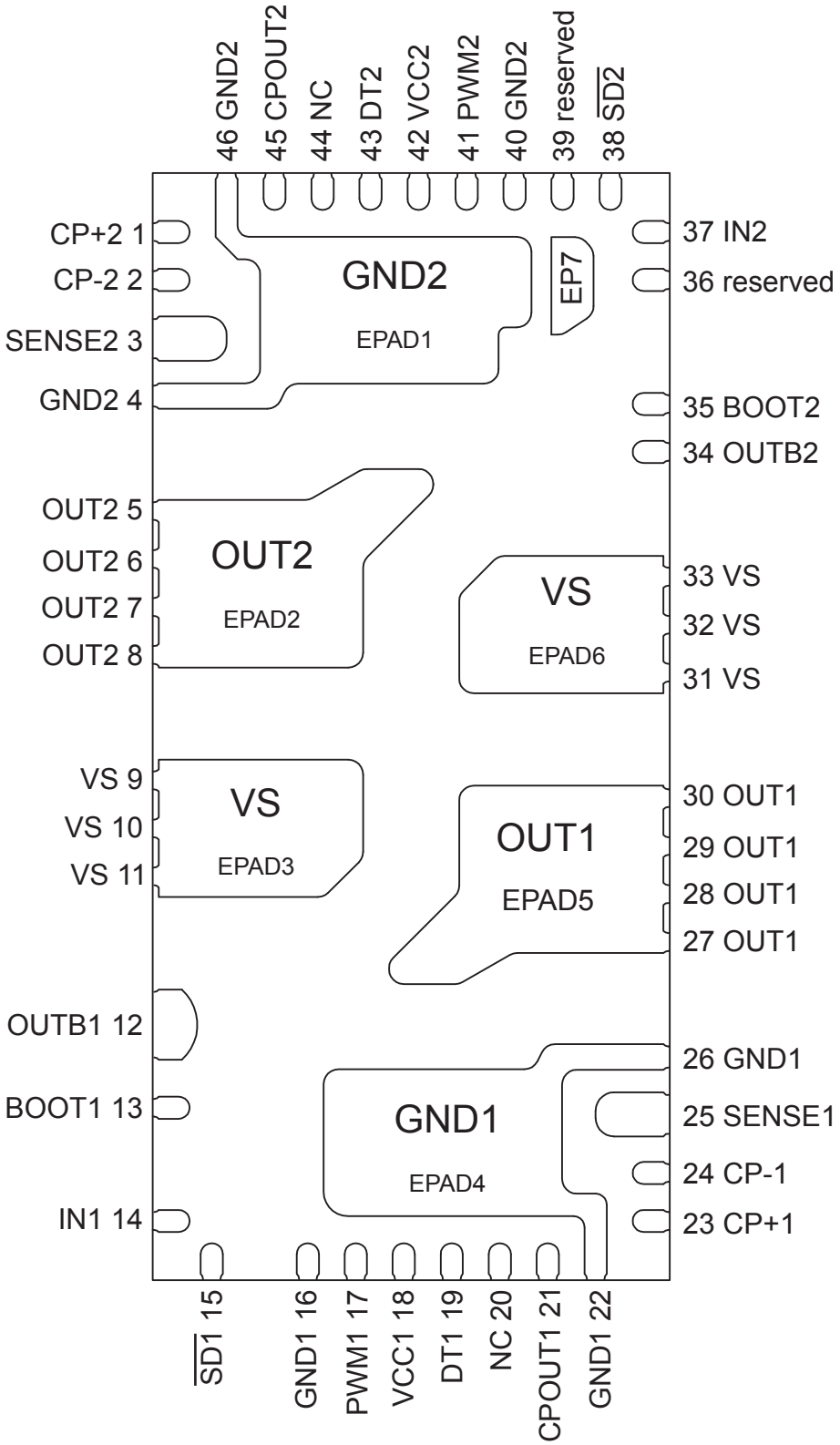
# 1 Block diagram

Figure 2. **Block diagram**



## 2 Pin description and connection diagram

Figure 3. **Pin connection (top view)**



## 2.1 Pin list

**Table 1. Pin description**

| Pin number | Pin name | Type | Function |
|---|---|---|---|
| 9, 10, 11, 31, 32, 33, EPAD3, EPAD6 | VS | Power Supply | High voltage supply (high-side MOSFET Drain)(1) |
| 27, 28, 29, 30, EPAD5 | OUT1 | Power Output | Half-bridge 1 output |
| 5, 6, 7, 8, EPAD2 | OUT2 | Power Output | Half-bridge 2 output |
| 12 | OUTB1 | Power supply | Half-bridge 1 output connection for high-side supply capacitor (2) |
| 34 | OUTB2 | Power supply | Half-bridge 2 output connection for high-side supply capacitor (3) |
| 25 | SENSE1 | Power Supply | Half-bridge 1 sense (low-side MOSFET Source) |
| 3 | SENSE2 | Power Supply | Half-bridge 2 sense (low-side MOSFET Source) |
| 13 | BOOT1 | Power Supply | Gate driver 1 high-side supply voltage |
| 35 | BOOT2 | Power Supply | Gate driver 2 high-side supply voltage |
| 18 | VCC1 | Power Supply | Gate driver 1 supply voltage |
| 42 | VCC2 | Power Supply | Gate driver 1 supply voltage |
| 16, 22, 26, EPAD4 | GND1 | Power Supply | Gate driver 1 ground |
| 4, 40, 46, EPAD1 | GND2 | Power Supply | Gate driver 2 ground |
| 14 | IN1 | Logic Input | Driver 1 logic input |
| 37 | IN2 | Logic Input | Driver 2 logic input |
| 15 | $\overline{SD1}$ | Logic Input | Driver 1 shut down input (active low) |
| 38 | $\overline{SD2}$ | Logic Input | Driver 2 shut down input (active low) |
| 17 | PWM1 | Logic Input | Driver 1 PWM input |
| 41 | PWM2 | Logic Input | Driver 2 PWM input |
| 19 | DT1 | Input | Driver 1 dead time setting |
| 43 | DT2 | Input | Driver 2 dead time setting |
| 21 | CPOUT1 | Output | Comparator 1 output (open drain) |
| 45 | CPOUT2 | Output | Comparator 2 output (open drain) |
| 23 | CP+1 | Input | Comparator 1 positive input |
| 1 | CP+2 | Input | Comparator 2 positive input |
| 24 | CP-1 | Input | Comparator 1 negative input |
| 2 | CP-2 | Input | Comparator 2 negative input |
| 36, 39, EPAD7 | reserved | Reserved | Not connected |
| 20, 44, | NC | Reserved | Not connected |

1. *EPAD3 is internally connected with EPAD6. No connection is required at PCB level.*
2. *Pin 12 is internally connected to OUT1. No connection is required at PCB level.*
3. *Pin 34 is internally connected to OUT2. No connection is required at the PCB level. Use pin 34 for bootstrap capacitor connection only.*

# 3 Electrical data

## 3.1 Absolute maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Test Condition | Value | Unit |
|---|---|---|---|---|
| $V_{DS}$ | MOSFET Drain-to-Source Voltage | $T_J$ = 25 °C | 600 | V |
| VCC1, VCC2 | Drivers supply voltage | - | -0.3 to 20 | V |
| VCCx-SENSEx | VCCx to SENSEx pin voltage | - | -0.3 to 25 | V |
| $V_{BOOTx}$ | Bootstrap voltage | - | GNDx-0.3 to 600 | V |
| $V_{BO1}$, $V_{BO2}$ | BOOTx to OUTx pin voltage | - | -0.3 to 20 | V |
| $V_{CP+x}$, $V_{CP-x}$ | Comparator input pin voltage | - | -0.3 to $V_{CCx}$+0.3 | V |
| $V_{CPOUTx}$ | Comparator open-drain output voltage | - | -0.3 to 15 | V |
| $I_D$ | Drain current (per MOSFET) | DC @ $T_{CB}$ = 25 °C (1) | 3.5 | A |
| | | DC @ $T_{CB}$ = 100 °C (1) (2) | 2 | A |
| | | Peak @ $T_{CB}$ = 25 °C (1) (2) (3) | 14 | A |
| $SR_{OUT}$ | Full-bridge outputs slew rate (10% - 90%) | (2) | 40 | V/ns |
| $V_i$ | Logic inputs voltage range | - | -0.3 to 15 | V |
| $T_J$ | Junction temperature | - | -40 to 150 | °C |
| $T_s$ | Storage temperature | - | -40 to 150 | °C |
| $P_{tot}$ | Total power dissipation (4) | $T_{CB}$ = 25 °C for each MOSFET | 43 | W |
| | | $T_{amb}$ = 25 °C, whole device, device mounted on an FR4 2s2p board as per JESD51-5,7. See Table 4.. (5) | 5 | W |
| ESD | Human body model | - | ±1500 | V |
| | Charged device model | - | ±500 | V |

1. *$T_{CB}$ is temperature of case bottom pad.*
2. *Characterized, not tested in production.*
3. *The value specified by design factor, pulse duration limited by max junction temperature and SOA.*
4. *Value calculated based on thermal resistance, power uniformly distributed over the four power MOSFETs, still air.*
5. *Actual applicative board max dissipation could be higher or lower depending on layout and cooling techniques.*

## 3.2 Recommended operating conditions

**Table 3. Recommended operating conditions**

| Symbol | Pin | Parameter | Test Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| VCC1, VCC2 | VCCx -GNDx | Driver Supply voltage | - | 10 | 20 | V |
| $V_{BO1}$, $V_{BO2}$ | BOOTx -OUTx | BOOTx to OUTx pin voltage | - | 9.8 | 20 | V |
| $V_{CP-x}$ | CP-x | Comparator negative input voltage | $V_{CP+}$ ≤ 2.5 V | - | $V_{CCx}$ (1) | V |

| Symbol | Pin | Parameter | Test Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CP+x}$ | CP+x | Comparator positive input voltage | $V_{CP-} \leq 2.5$ V | - | $V_{CCx}$ (1) | V |
| $T_J$ | - | Junction temperature | - | -40 | 125 | °C |

1. *At least one of the comparator inputs must be lower than 2.5 V to guarantee proper operation.*

## 3.3 Thermal data

**Table 4. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{th(J-CB)}$ | Thermal resistance junction to each MOSFET exposed pad, typical | 2.85 | °C/W |
| $R_{th(J-A)}$ | Thermal resistance junction-to-ambient (1) | 25 | °C/W |

1. *The junction to ambient thermal resistance is obtained simulating the device mounted on a 2s2p (4-layer) FR4 board as per JESD51-5,7 with 4 thermal vias for each MOSFET pad. Power dissipation is uniformly distributed over the four power MOSFETs.*

# 4 Electrical characteristics

## 4.1 Driver

VCCx = 15 V; $T_J$ = 25 °C, unless otherwise specified.

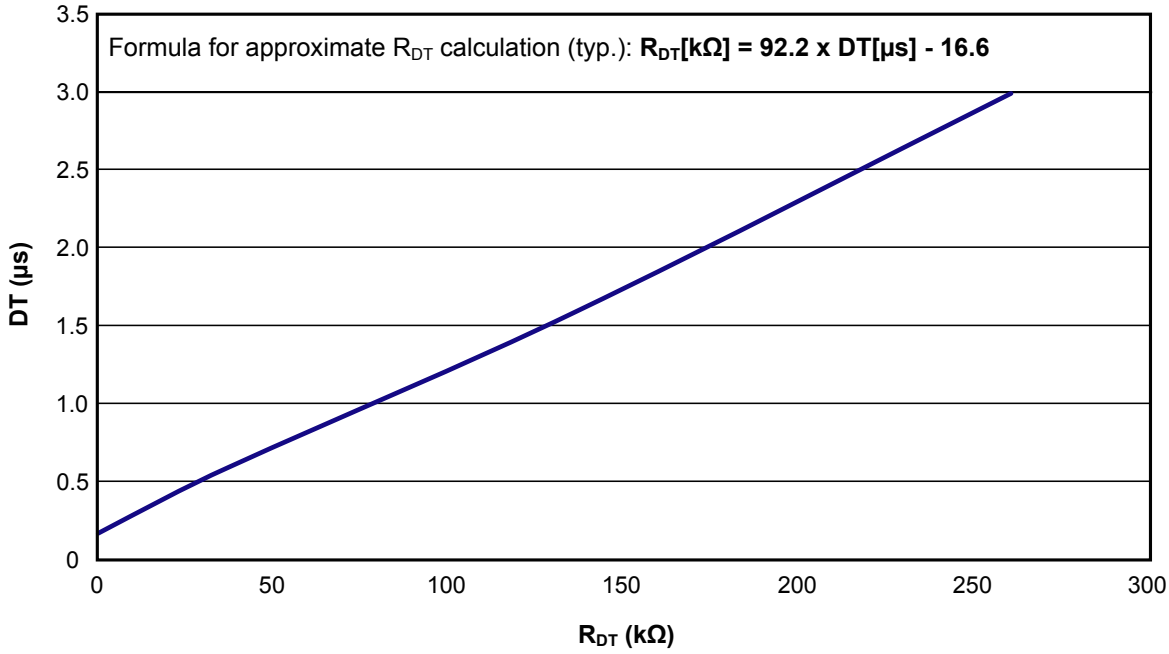
**Table 5. Driver electrical characteristics**

| Symbol | Pin | Parameter | Test condition | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Low supply voltage section** | | | | | | | |
| $VCC_{_hys}$ | VCCx vs. GNDx | VCC UV hysteresis | - | 1.2 | 1.5 | 1.8 | V |
| $VCC_{_thON}$ | | VCC UV turn ON threshold | - | 9 | 9.5 | 10 | V |
| $VCC_{_thOFF}$ | | VCC UV turn OFF threshold | - | 7.6 | 8 | 8.4 | V |
| $I_{qccu}$ | | Undervoltage quiescent supply current | VCC = 7 V; $\overline{SD}$ = 5 V; IN = PWM = GND; $R_{DT}$ = 0 Ω; CP+ = GND; CP- = 0.5 V | - | 110 | 150 | µA |
| $I_{qcc}$ | | Quiescent current | VCC = 15 V; $\overline{SD}$ = 5 V; IN = PWM = GND; $R_{DT}$ = 0 Ω; CP+ = GND; CP- = 0.5 V | - | 600 | 1000 | µA |
| **Bootstrapped supply voltage section** | | | | | | | |
| $V_{BO_hys}$ | BOOTx vs. OUTx | $V_{BO}$ UV hysteresis | - | 0.8 | 1.0 | 1.2 | V |
| $V_{BO_thON}$ | | $V_{BO}$ UV turn ON threshold | - | 8.2 | 9 | 9.8 | V |
| $V_{BO_thOFF}$ | | $V_{BO}$ UV turn OFF threshold | - | 7.3 | 8 | 8.7 | V |
| $I_{QBOU}$ | | Undervoltage $V_{BO}$ quiescent current | $V_{BO}$ = 7 V | - | 40 | 100 | µA |
| $I_{QBO}$ | | $V_{BO}$ quiescent current | $V_{BO}$ = 15 V IN = PWM = $\overline{SD}$ = 5 V; | - | 140 | 220 | µA |
| $R_{BD(on)}$ | VCCx vs. BOOTx | Bootstrap driver on resistance (1) | IN = GND; PWM = $\overline{SD}$ = 5 V; | - | 120 | - | Ω |
| **Logic inputs** | | | | | | | |
| $V_{il}$ | INx, PWMx, $\overline{SDx}$ | Logic level Low threshold voltage | - | 0.8 | - | 1.1 | V |
| $V_{ih}$ | | Logic level High threshold voltage | - | 1.9 | - | 2.3 | V |
| $I_{ih}$ | | Logic ‘1’ input bias current | IN = PWM = $\overline{SD}$ = 15 V | 10 | 40 | 100 | µA |
| $I_{il}$ | | Logic ‘0’ input bias current | IN = PWM = $\overline{SD}$ = GND | - | - | 1 | µA |
| $R_{in_pd}$ | | Logic Inputs pull-down resistor | IN = PWM = $\overline{SD}$ = 15 V | 0.18 | 0.37 | 1.5 | MΩ |
| **Comparator** | | | | | | | |
| $V_{io}$ | CP-x, CP+x vs. GNDx | Input offset voltage | $V_{CP-}$ = 0.5 V | -16 | - | +16 | mV |
| $I_{ib}$ | | Input bias current | $V_{CP+}$ = 1 V, $V_{CP-}$ = 1 V | - | - | 1 | µA |

| Symbol | Pin | Parameter | Test condition | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{d_comp}$ | CP+x to CPOUTx | Comparator delay | $R_{pu}$ = 100 kΩ to 5 V<br>$V_{CP-}$ = 0.5 V;<br>Voltage step on CP+ = 0 to 3.3 V;<br>50% CP+ to 90% CPOUT | - | 90 | 130 | ns |
| $I_{OD}$ | CPOUTx | Open-drain low level sink current | CPOUT = 400 mV,<br>$V_{CP+}$ = 1 V, $V_{CP-}$ = 0.5 V | 2.4 | - | - | mA |
| $I_{ODlk}$ | | Open-drain leakage current | CPOUT = 15 V,<br>$V_{CP+}$ = 0 V, $V_{CP-}$ = 0.5 V | - | - | 1 | µA |
| $SR_{CPOUT}$ | CPOUTx | Comparator output slew rate | $C_L$ = 180 pF<br>$R_{pu}$ = 5 kΩ to 5 V<br>CPOUT from 90% to 10% | - | 60 | - | V/µs |
| **Dead time** | | | | | | | |
| DT | DTx | Dead time setting range .(3) | $R_{DT}$ = 0 | 0.1 | 0.18 | 0.25 | µs |
| | | | $R_{DT}$ = 37 kΩ, $C_{DT}$ = 100 nF | 0.48 | 0.6 | 0.72 | |
| | | | $R_{DT}$ = 136 kΩ, $C_{DT}$ = 100 nF | 1.35 | 1.6 | 1.85 | |
| | | | $R_{DT}$ = 260 kΩ, $C_{DT}$ = 100 nF | 2.6 | 3.0 | 3.4 | |
| MDT | | Matching dead time (3) (4) | $R_{DT}$ = 0 | - | - | 80 | ns |
| | | | $R_{DT}$ = 37 kΩ, $C_{DT}$ = 100 nF | - | - | 120 | |
| | | | $R_{DT}$ = 136 kΩ, $C_{DT}$ = 100 nF | - | - | 250 | |
| | | | $R_{DT}$ = 260 kΩ, $C_{DT}$ = 100 nF | - | - | 400 | |

1. *$R_{BD(on)}$ is tested in the following way: $R_{BD(on)}$ = [(VCC - $V_{BOOTa}$) - (VCC - $V_{BOOTb}$)] / [Ia - Ib], where: Ia is BOOT pin current when $V_{BOOT}$ = $V_{BOOTa}$; Ib is BOOT pin current when $V_{BOOT}$ = $V_{BOOTb}$.*
2. *The comparator is disabled when VCC is in UVLO condition.*
3. *Tested at wafer level before packaging*
4. *MDT = | DTLH – DTHL |.*

Figure 4. **Typical dead time vs. $R_{DT}$ resistor value**




## 4.2 Power MOSFET

VCCx = 15 V; $T_J$ = 25 °C, unless otherwise specified.

Table 6. **Power MOSFET electrical characteristics**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **MOSFET on/off states** | | | | | | |
| $V_{(BR)DS}$ | Drain-source breakdown voltage | $I_D$ = 1 mA (1) | 600 | - | - | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{DS}$ = 600 V<br>$\overline{SD}$ = SENSE = GND | - | - | 1 | µA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA (1) | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $I_D$ = 1.75 A;<br>$V_{GS}$ = 10 V; | - | 1.38 | 1.75 | Ω |
| **MOSFET Avalanche** | | | | | | |
| $I_{AS}$ | Avalanche current, repetitive or not repetitive | pulse width limited by $T_J$ max (1) | - | - | 1 | A |
| $E_{AS}$ | Single pulse avalanche energy | Starting $T_J$ = 25 °C,<br>$I_D$ = $I_{AS}$, $V_{DD}$ = 50 V (1) | - | - | 132 | mJ |
| **Source-Drain diode** | | | | | | |
| $V_{SD}$ | Diode forward on voltage | $\overline{SD}$ = SENSE = GND<br>$I_{SD}$ = 3.5 A; | - | - | 1.6 | V |

1. *Tested at the wafer level before packaging.*

# 5 Device characterization values

Table 7., Table 8. and the electrical characteristics curves (from Figure 6. to Figure 15.) represent typical values based on characterization and simulation results and are not subject to production tests.

**Table 7. Power MOSFET characterization values**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **MOSFET Dynamic** | | | | | | |
| $Q_g$ | Total gate charge | $V_{GS}$ = 10 V, $T_J$ = 25 °C<br>$V_{DS}$ = 480 V, $I_D$ = 3.5 A | - | 5.3 | - | nC |
| **Source-Drain diode** | | | | | | |
| $t_{rr}$ | Diode reverse recovery time | $I_{SD}$ = 3.5 A, $T_J$ = 25 °C<br>di/dt = 100 A/µs,<br>$V_{DS}$ = 60 V | - | 58 | - | ns |
| $Q_{rr}$ | Diode reverse recovery charge | | - | 109 | - | µC |
| $I_{RRM}$ | Diode reverse recovery current | | - | 4 | - | A |
| $t_{rr}$ | Diode reverse recovery time | $I_{SD}$ = 3.5 A, $T_J$ = 150 °C<br>di/dt = 100 A/µs,<br>$V_{DS}$ = 60 V | - | 109 | - | ns |
| $Q_{rr}$ | Diode reverse recovery charge | | - | 309 | - | µC |
| $I_{RRM}$ | Diode reverse recovery current | | - | 5 | - | A |

**Table 8. Inductive load switching characteristics**

| Symbol | Parameter | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{(on)}$ (1) | Turn-on time | VS = 300 V,<br>VCC = $V_{BO}$ = 15 V,<br>$I_D$ = 1.75 A<br>See Figure 5. | - | 450 | - | ns |
| $t_{C(on)}$ (2) | Crossover time (on) | | - | 67 | - | ns |
| $t_{(off)}$ (1) | Turn-off time | | - | 171 | - | ns |
| $t_{C(off)}$ (2) | Crossover time (off) | | - | 25 | - | ns |
| $t_{SD}$ | Shutdown to high/low-side propagation delay | | - | 165 | - | ns |
| $E_{on}$ | Turn-on switching losses | | - | 51 | - | µJ |
| $E_{off}$ | Turn-off switching losses | | - | 3 | - | µJ |

1. *$t_{(on)}$ and $t_{(off)}$ include the propagation delay time of the internal driver*
2. *$t_{C(on)}$ and $t_{C(off)}$ are the switching times of MOSFET itself under the internally given gate driving conditions*

**Figure 5. Switching time definition**

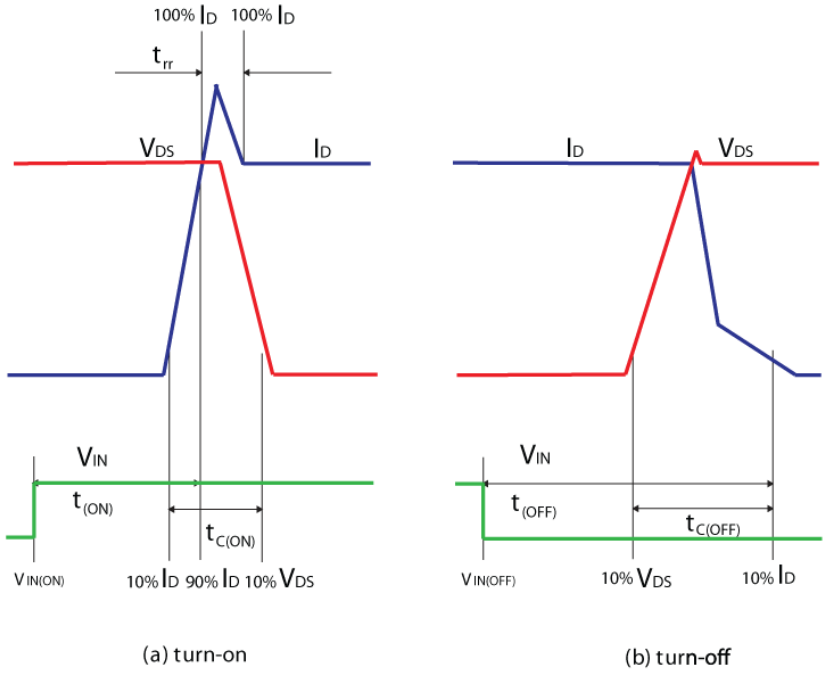



**Figure 6. Normalized gate threshold voltage vs temperature**

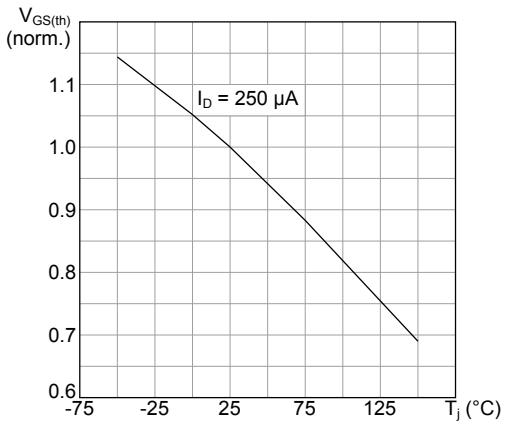



**Figure 7. Normalized drain-source breakdown voltage vs. temperature**

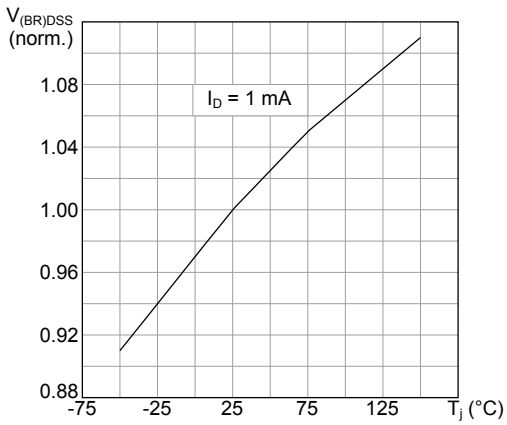


**Figure 8. Static drain-source on-resistance**

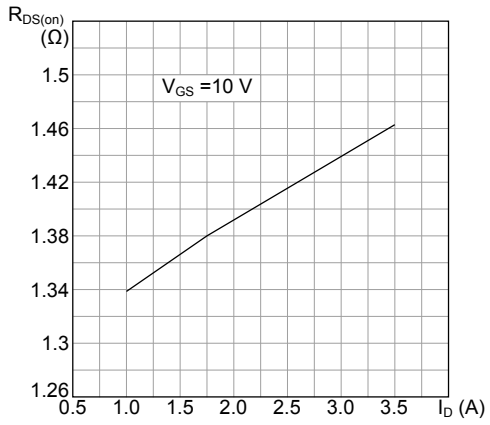



**Figure 9. Normalized on-resistance vs temperature**

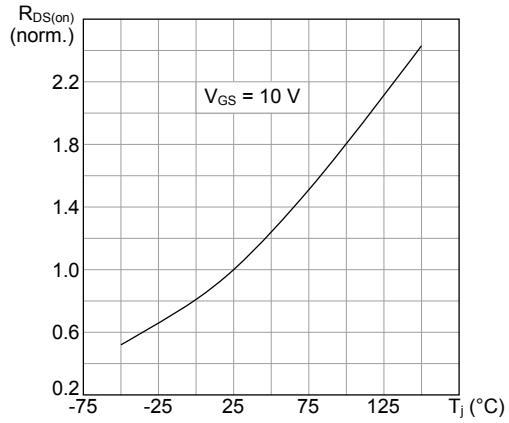



**Figure 10. Transfer characteristics**

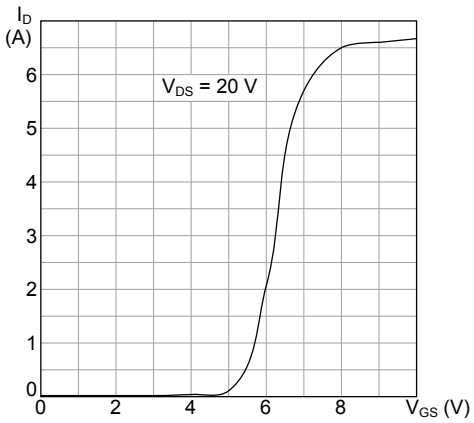



**Figure 11. Output characteristics**

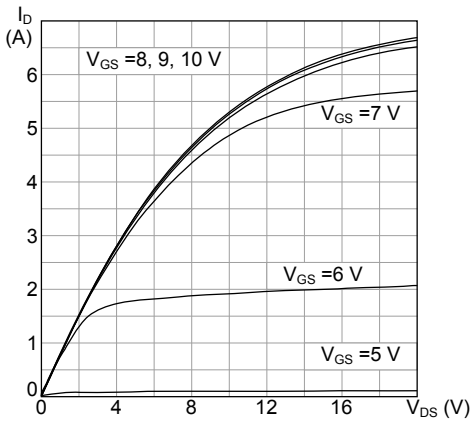



**Figure 12. Static source-drain diode forward characteristics**

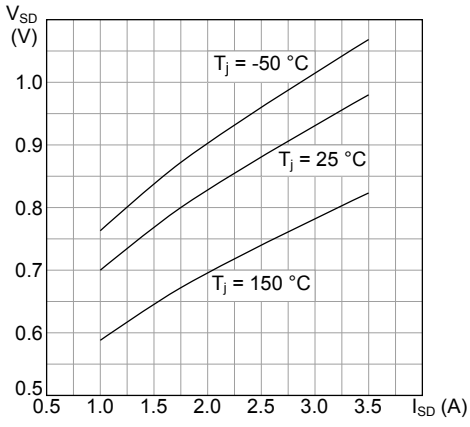



**Figure 13. Gate charge vs. gate-source voltage**

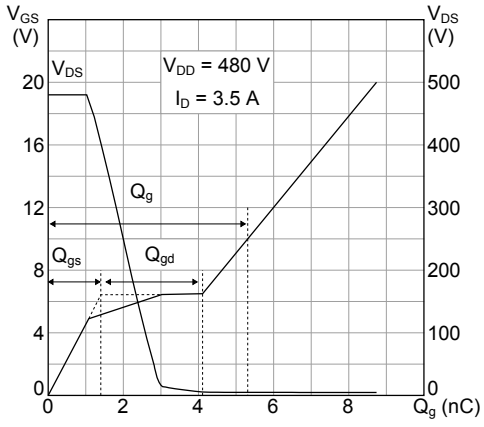


**Figure 14. MOSFET capicatance variations**

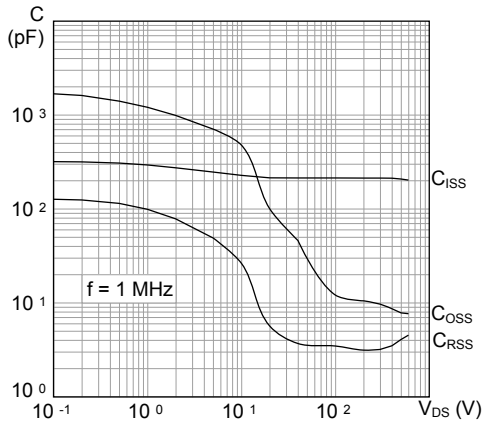
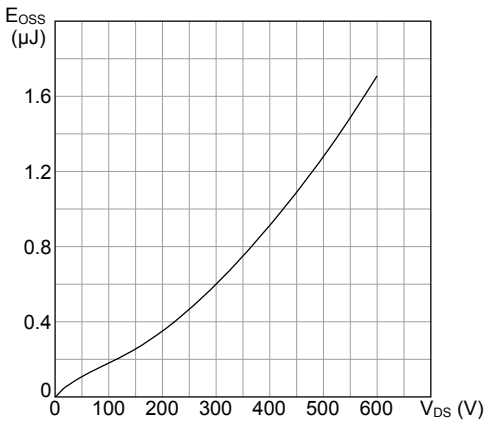



**Figure 15. MOSFET output capacitance stored energy**



# 6 Functional description

## 6.1 Logic inputs

The PWD5F60 full bridge features two identical half-bridge sections. Each section has three logic inputs to control the internal high-side and low-side MOSFETs.

**Table 9. Truth table**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| $\overline{SD}$ | IN | PWM | HS | LS |
| 0 | X | X | OFF | OFF |
| 1 | 0 | 0 | OFF | ON |
| 1 | 0 | 1 | OFF | ON |
| 1 | 1 | 0 | OFF | ON |
| 1 | 1 | 1 | ON | OFF |

The logic inputs have internal pull-down resistors. The purpose of these resistors is to set a defined logic level if, for example, there is an interruption on the logic lines or the controller outputs are in tri-state conditions.

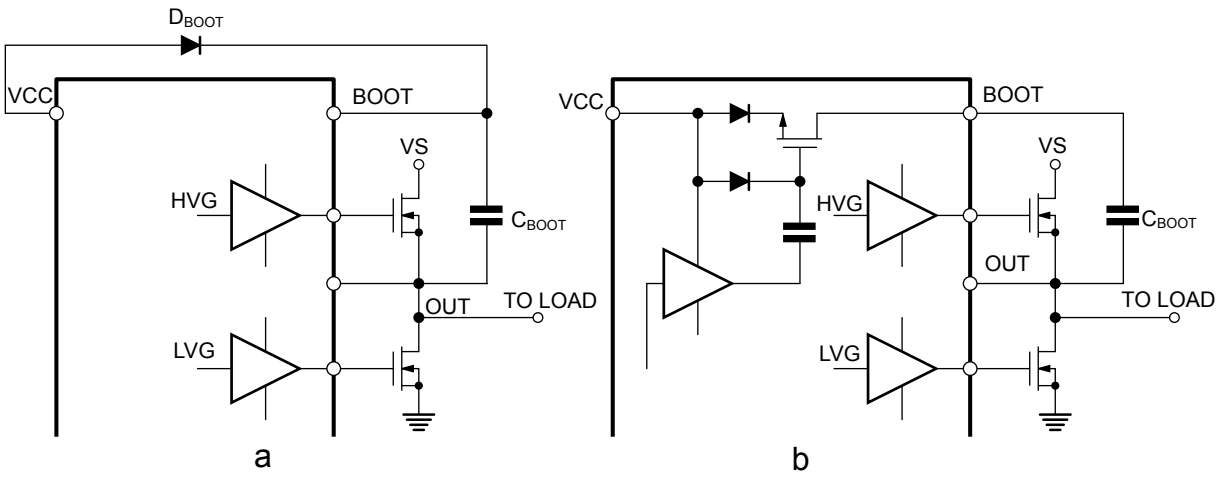
## 6.2 Bootstrap structure

Bootstrap circuitry is typically used to supply the high-voltage section. This function is normally accomplished with a high-voltage fast recovery diode, as shown in Figure 16. (side a).

In the PWD5F60, a patented integrated structure replaces the external diode. The structure consists of a series of low-voltage diodes and a high-voltage DMOS, driven synchronously by the low-side driver (LVG), as shown in Figure 16. (side b). An internal bootstrap provides the DMOS driving voltage. The integrated diode structure is actively turned on and guarantees best performance only when the low-side driver is on.

In applications where the control strategy requires recharging the bootstrap capacitor even when the low-side driver is off, the use of an external bootstrap diode in parallel to the integrated structure is possible.

**Figure 16. Bootstrap structure**



## 6.3 Supply pins and UVLO function

The VCCx supply pin supplies current to the low-side section of the gate driver and to the integrated bootstrap diode used to charge the bootstrap capacitor. During output commutations, the average current used to provide gate charge to the high-side and low-side MOSFETs flow through these pins.

The VCC1 and VCC2 pins separately supply power to the two drivers, even if they are usually connected together at the power supply in final applications.

The PWD5F60 VCCx supply voltage is continuously monitored by undervoltage lockout (UVLO) circuits that turn the high-side and low-side MOSFETs off when the supply voltage falls below the $VCC_{_thOFF}$ threshold. The VCCx UVLO circuitry turns on the high-side or low-side MOSFET according to the input status as soon as the supply voltage rises above the $VCC_{_thON}$ voltage. $VCC_{_hys}$ hysteresis is provided for noise rejection purposes.

Two separate UVLO circuits monitor VCC1 and VCC2 so that when a UVLO occurs on a single rail, only the corresponding half bridge MOSFETs are turned off.

The PWD5F60 $V_{BO}$ supply voltages are also continuously monitored by two dedicated $V_{BO}$ UVLO circuits that turn the corresponding high-side MOSFET off when the supply voltage falls below the $V_{BO_thOFF}$ threshold. The UVLO circuitry allows turning the high-side MOSFET on again, according to input edges, as soon as the $V_{BO}$ supply voltage rises above the $V_{BO_thON}$ voltage. A $V_{BO_hys}$ hysteresis is provided for noise rejection purposes.

## 6.4 Dead time

The PWD5F60 automatically inserts a DT dead time on each half bridge. This avoids shoot-through as a MOSFET gate discharges completely before charging starts on the other MOSFET gate.

The DT value is set by the resistor placed between the DTx pin and GNDx, as shown in Figure 4..

The minimum dead time value set with a 0 Ω resistor is normally sufficient to avoid shoot-through between high side and low side.

Some applications, like those operating with soft turn-on commutations at low current seeking maximum efficiency, might benefit from a longer dead time. The PWD5F60 lets you set the dead time for each half bridge for maximum flexibility.

# 7 Typical application diagrams

Figure 17. **Generic application**

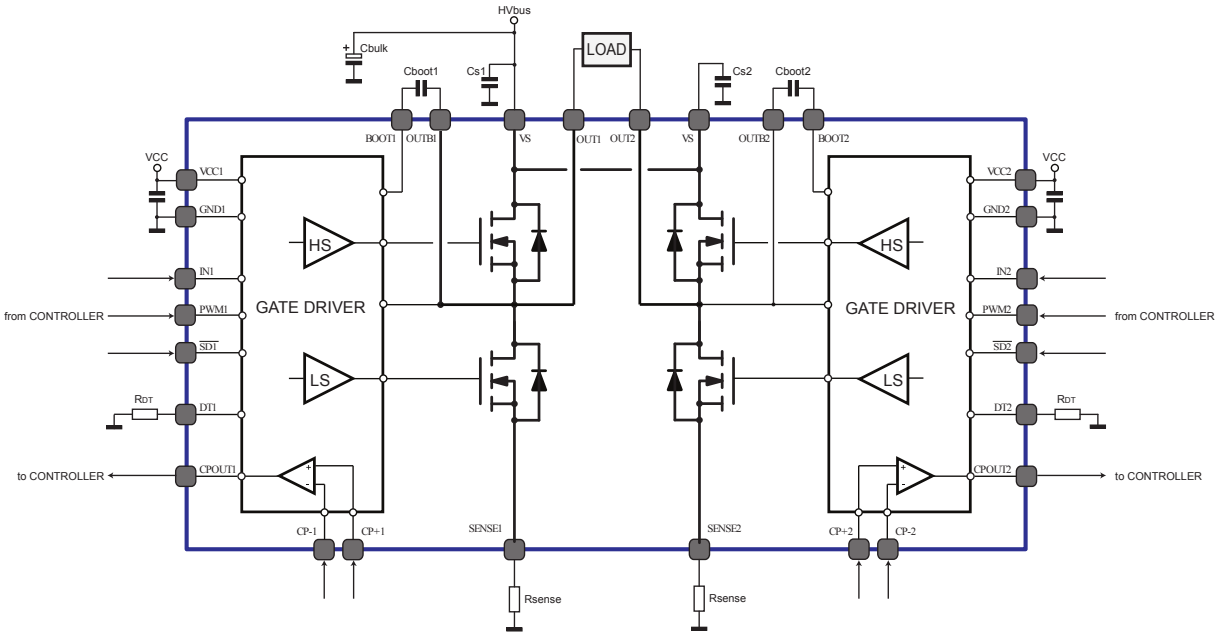
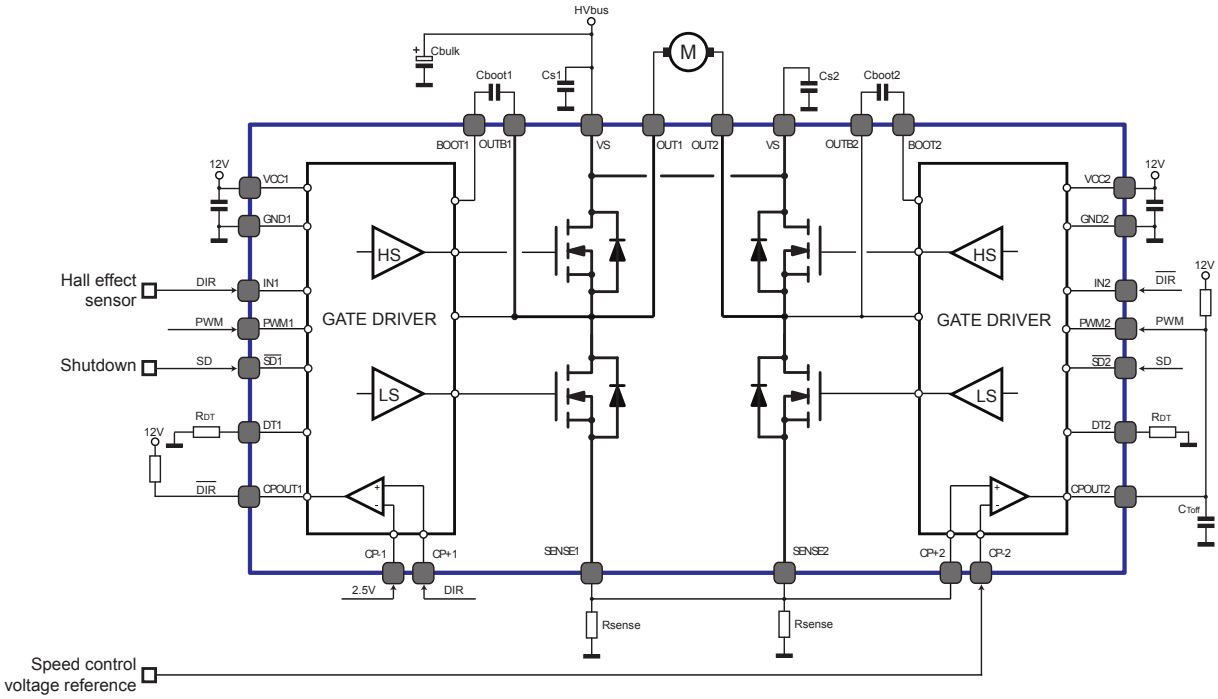



Figure 18. **Current mode motor control**



# 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

## 8.1 VFQFPN 15 x 7 x 1 mm package information

The package outline CAD file is available upon request.

**Figure 19. VFQFPN 15 x 7 x 1 mm package dimensions – drawing top and side view**

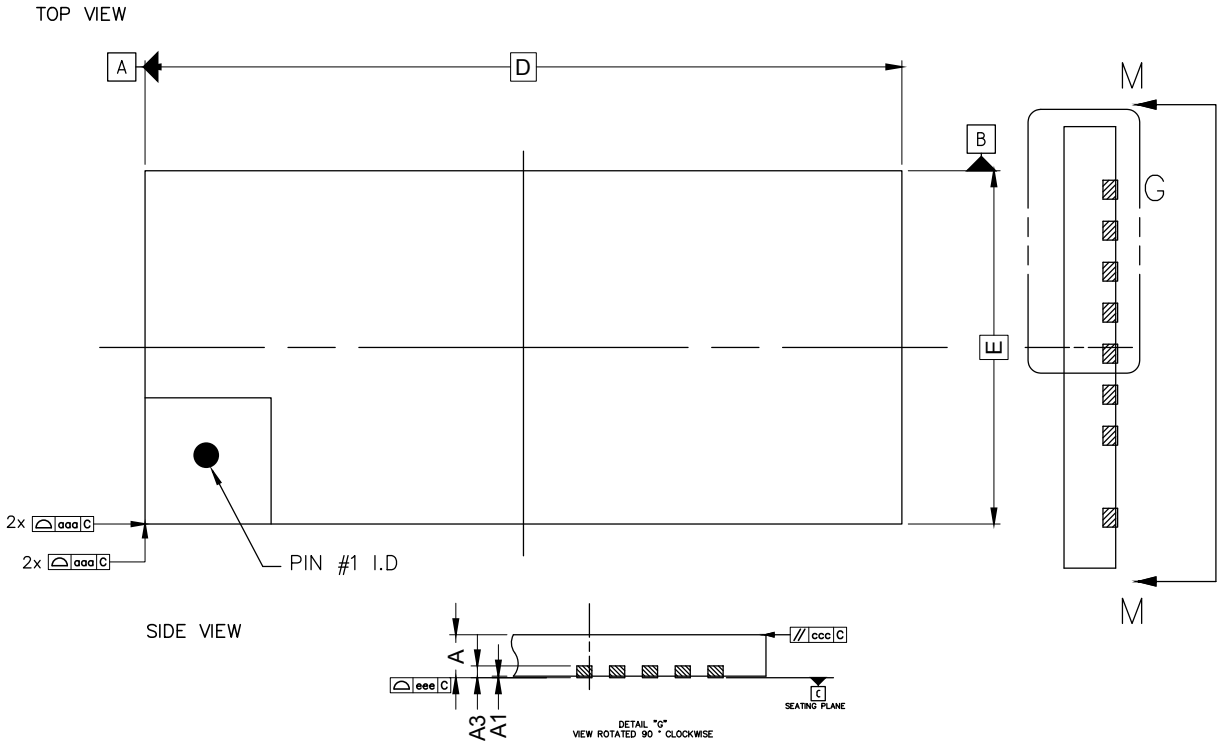


Figure 20. **VFQFPN 15 x 7 x 1 mm package dimensions – drawing bottom view**

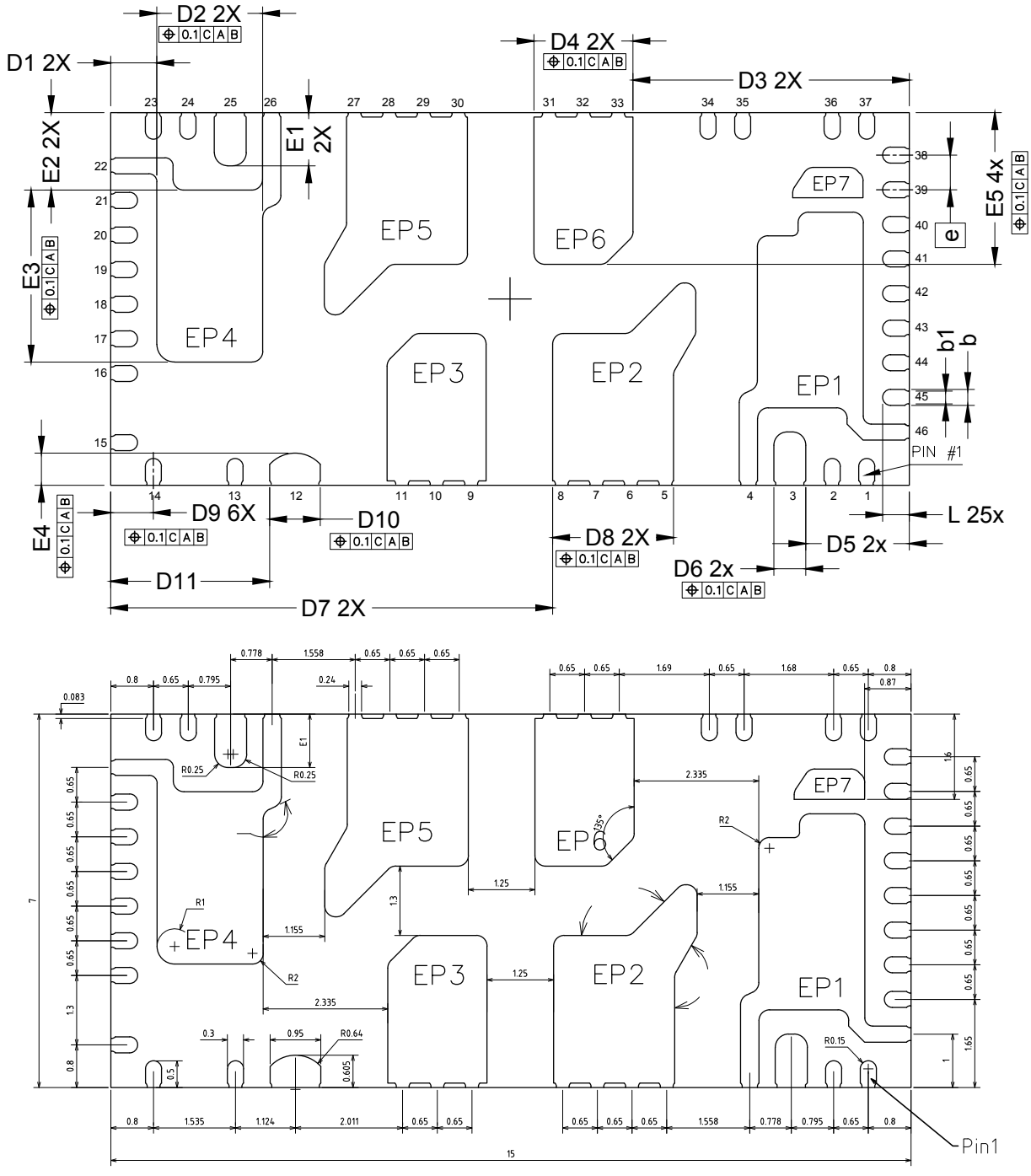


Figure 21. **VFQFPN 15 x 7 x 1 mm package dimensions – exposed pads details**

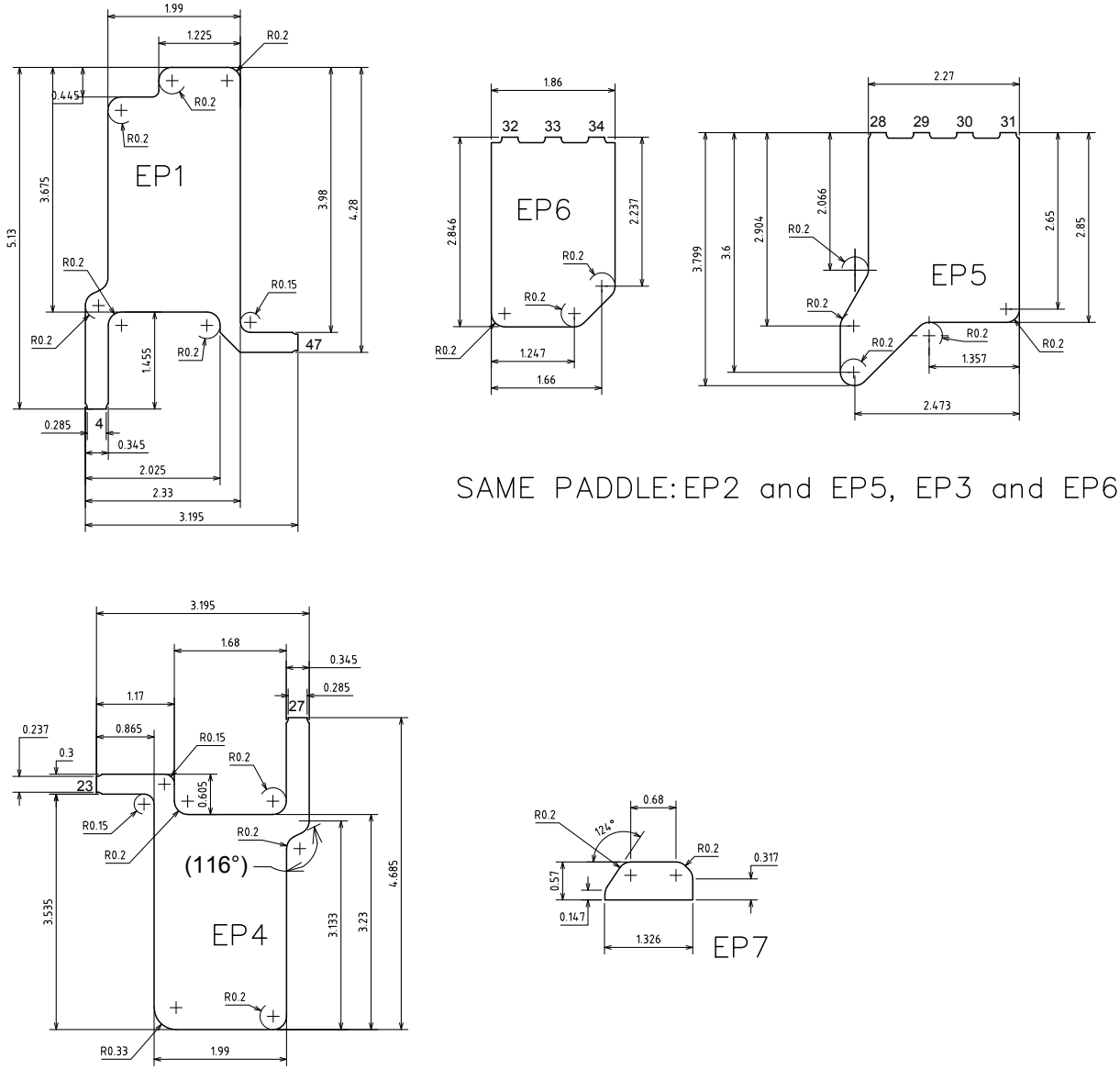



Table 10. **VFQFPN 15 x 7 x 1 mm package mechanical data**

| Symbol | Dimensions (mm) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | | 0.05 |
| A3 | | 0.20 | |
| b | 0.20 | 0.30 | 0.40 |
| b1 | 0.14 | 0.24 | 0.34 |
| D | 14.90 | 15.00 | 15.10 |
| E | 6.90 | 7.00 | 7.10 |
| D1 | | 0.865 | |

| Symbol | Dimensions (mm) | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| D2 | 1.89 | 1.99 | 2.09 |
| D3 | | 5.10 | |
| D4 | 1.70 | 1.86 | 1.90 |
| D5 | | 1.945 | |
| D6 | 0.50 | 0.60 | 0.70 |
| D7 | | 8.30 | |
| D8 | 2.17 | 2.27 | 2.37 |
| D9 | 0.70 | 0.80 | 0.90 |
| D10 | 0.85 | 0.95 | 1.05 |
| D11 | | 2.985 | |
| D12 | | 4.01 | |
| D13 | | 2.85 | |
| D14 | 0.20 | 0.345 | 0.40 |
| E1 | 0.90 | 1.00 | 1.10 |
| E2 | | 1.455 | |
| E3 | 3.13 | 3.23 | 3.33 |
| E4 | 0.505 | 0.605 | 0.705 |
| E5 | 2.75 | 2.85 | 2.95 |
| E6 | 3.70 | 3.80 | 3.90 |
| L | 0.40 | 0.50 | 0.60 |
| e | | 0.65 | |
| R1 | | 0.33 | |
| R2 | | 0.20 | |
| R3 | | 0.15 | |
| aaa | | 0.10 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |

*Note:*

- *VFQFPN stands for Thermally Enhanced Very thin Fine pitch Quad Flat Packages No lead.*
- *Dimensioning and tolerances comply with ASME Y14.5-2009.*
- *All dimensions are in millimetres.*
- *A variable pitch is applied on leads. Please refer to Figure 20. for lead position details.*
- *The leads size is comprehensive of the thickness of the leads finishing material.*
- *Dimensions do not include mold protrusion, not to exceed 0.15 mm.*
- *Package outline does not include eventual metal burr dimensions.*

# 9 Ordering information

Table 11. **Device summary**

| Order code | Package | Packaging |
|---|---|---|
| PWD5F60 | VFQFPN 15 x 7 x 1 mm | Tray |
| PWD5F60TR | VFQFPN 15 x 7 x 1 mm | Tape and Reel |

## Revision history

Table 12. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 03-Jul-2018 | 1 | Initial release. |

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